CHAPTER 7

Conclusions, Major Contributions and Scope of Future Work

7.1 Conclusions and Major Contributions

In this thesis Proposed, Analyzed and Designed wideband and narrowband LNAs for improve performance of RF receiver for fulfill need of future wireless communication. The performance parameters of the LNA, Input/output impedance matching, noise figure, gain and linearity have tradeoff among them. The proposed designs aim to relax tradeoff among different performance parameters and improve performance of the LNA to make it suitable for future RF receiver.

Chapter 4 presented the detail design of the LNAs for Bluetooth and GPS applications. The first LNA was designed using inductive degenerate topology for Bluetooth receiver and it’s achieved power gain ($S_{21}$), input reflection coefficient ($S_{11}$), NF and IIP3 is 22 dB, -21 dB, 3.6 dB and 1 dBm respectively. The LNA design consumed 10.8mW power from 1.8V supply. Bluetooth receiver LNA is also designed using current reuse LNA topology for portable low power devices. The proposed CRLNA design consuming only 5.4 mW power from 1.8V supply voltage which saved 50% power compare to simple inductive degenerate topology with the cost of larger silicon area. The 1.575 GHz narrowband LNA for GPS receiver is designed using inductive degenerate topology. The LNA for GPS receiver achieved Power gain, $S_{11}$, NF, IIP3 and power consumption are 20 dB, -20 dB, 3 dB, 1 dBm and 10.8 mW respectively. The proposed narrowband LNA designs will improve performance of future Bluetooth and GPS wireless communication.
Chapter 5 presented detailed design, analysis and simulation of high power gain 3.1- 10.6 GHz ultra wideband LNA for UWB system. The proposed UWB LNA design optimized for specifically high power gain for UWB RF frontend receiver. Due to FCC restriction, low power transmission for commercial UWB wireless applications require low noise high power gain receiver to amplify and process received weak signals. Common gate configuration of first stage of proposed design provided wideband input impedance matching in the multistage UWB LNA design. The CG has low power gain. The power gain has improved by using two cascade CS stages after CG in the proposed LNA design. NF and gain of the design have improved due to inductive load used instead of resistive in the design. Inductive load and next stage input capacitor are formed parallel tune circuit. Bandwidth of the design has improved by resonant each parallel tune circuit at different frequencies in interested band.

Simulated results of the UWB LNA design showed maximum power gain is 20-30 dB in interested band with low noise figure 2.8-6 dB. The achieved $S_{11}$ and IIP3 of the UWB LNA have -9 dB and -5.5 dBm respectively in interested band. Due to multi stage the proposed UWB LNA design has consumed slightly more power, 34 mW from 1.5V supply. Results of the high power gain UWB LNA shows the design has improved performance and makes it suitable for future UWB system and will open new frontier for UWB wireless communication users. FOM of proposed design shows UWB LNA achieved worthy overall performance with higher power gain compare to literature works.

In the chapter 6 highly linear 0.6-5.6 GHz wideband LNA designs for multi standards universal receiver are discussed. The proposed 0.6-5.6 GHz wideband matching, high linearity, high gain and low noise figure LNA design will support LTE and WiMAX 4G standards with existing GSM, CDMA, UMTS, Bluetooth, ZigBee and WLAN wireless standards for future RF receiver.

The first multi standard highly linear wideband LNA design is based on NMOS/PMOS inverter structure. The complementary characteristic of NMOS and PMOS transistors have improved linearity of the design by cancelling distortion. Resistive feedback NMOS/PMOS inverter structure is widely used in literature for linear wideband LNA design. Inverter structure of amplifier increased gain and reduced power consumption by current reusing but due to its higher input capacitance it reduced gain at higher frequency. Gate inductor based design has improved input impedance matching and gain at higher
frequency by cancelling capacitive effect. CD active feedback with resistive in NMOS/PMOS inverter structure has relaxed tradeoff among noise figure and input matching by providing one more degree of freedom to set input impedance matching and noise figure independently. The proposed highly linear wideband LNA has shunt and series inductive peaking CS next stage with CD active and resistive feedback NMOS/PMOS inverter structure.

Highly linear wideband LNA design achieved $S_{21}$, $S_{11}$, NF and average IIP3 were 16-20 dB, -10 dB, 3.2 dB and +4 dBm respectively. The design consumes 13.2 mW power including bias circuit. Stability simulation result showed that the design is unconditionally stable in interested band. Performance of the proposed highly linear wideband LNA makes it highly suitable for next generation 4G multi standards mobile terminal.

The next 0.6 – 5.6 GHz wideband LNA is designed for high power gain multi standards universal receiver. The high power gain multi standard wideband LNA is designed using CG with multi stage CS topology. The high power gain wideband LNA design achieved $S_{21}$, $S_{11}$, NF, IIP3 were >20 dB, <-8 dB, 4-6 dB and >-7 dBm respectively in interested 0.6-5.6 GHz band. Due to multistage the design consumed slightly high power, 26 mW including bias circuits. FOM shows proposed multi standards LNAs design achieved good overall performance compare to published wideband LNA designs.

All the LNAs were designed using TSMC 0.18µm RFCMOS technology. The proposed three novel wideband LNA topologies are relaxed tradeoff and improved performance of LNA. The high power gain with wideband matching and low noise figure UWB LNA design will improve performance of the UWB receiver. The highly linear and high power gain multi standard wideband LNA design will improve performance of future wireless communication.

### 7.2 Scope of Future Work

Here the work performed pre and post layout simulation to validate proposed LNAs design. In future, design will fabricate and validate for suitability for future wireless receiver.
The fabrication of passive inductor requires larger silicon area and it is not scalable as technology scale. Various active inductor design techniques are specified in literature. Active inductor based LNA design requires less silicon area and design is scalable but it adds more noise and consumes more power compared to passive inductor design. The NF and power consumption of active inductor based LNA can be reduce by using noise cancelling and low power LNA design.

RF frontend have three main analog blocks LNA, Mixer and Local oscillator. The work is expand by the design of mixer and local oscillator for multi standard universal receiver and integrate proposed LNA design with mixer and local to make complete RF frontend.