SIMULATION OF SINGLE LAYER ZnO CHANNEL THIN FILM TRANSISTOR
5.1 Zinc Oxide Thin Film Transistor

In last decades thin film transistors have shown an excessive expansion on prevailing technologies and continued the scope of potentially feasible applications in large-area and flexible devices. Presently, thin-film transistors (TFTs) using wide bandgap oxide semiconductors have attracted much attention for applications in flexible electronic devices.

High optical transparency and low cost with excellent switching performance drew the attention of researchers in using ZnO as a potential material for TFT device design. The electrical parameter extraction of ZnO channel thin film transistor using simulation is carried out in Sentaurus TCAD tool. The scope of the research is to analyze the performance of the device on the basis of parameters extracted from its transfer characteristics. The device has shown high field effect mobility and significant on-off current with improved $I_{ON}/I_{OFF}$ ratio of order of $\sim 10^5$, which makes the device reliable for the use in flexible electronics and flat panel displays.

5.2 Material Properties of ZnO

Zinc oxide is a wide bandgap ($E_g \sim 3.3$ eV) compound semiconductor of the II-VI semiconductor group. The Zn-O bond possesses very strong ionic character which lies on the borderline between covalent and ionic compound. It has a large exciton binding energy of 60 meV. Generally, ZnO crystallizes in three main types, wurtzite (B4), zinc blende (B3), and rocksalt (B1), the schematic of which are shown in Figure 5.1. Among those, the most stable phase of ZnO at ambient condition is wurtzite. The rocksalt structure (similar to NaCl) can be obtained at relatively high pressures, and the zinc-blende structure can grow on top of cubic substrates [Ozgur et al. (2003)].
Figure. 5.1 Schematic of ZnO crystal structures: (a) cubic rocksalt (B1), (b) cubic zinc blende (B3), and (c) hexagonal wurtzite (B4). The shaded gray and black spheres represent Zn and O atoms, respectively [Ozgur et al. (2003)].

Zinc oxide is typically an n-type semiconductor, due to the inherent nature of forming oxygen deficient films. Although experimental work indicates the feasibility of p-type doping of ZnO material, the prospect for achieving p-type doping in ZnO is quite difficult compared with n-type doping, due to the carrier compensation by native defects such as zinc interstitial and oxygen vacancies. It is known that poly-crystalline ZnO is inherently n-type. Compared with other n-type semiconductors, ZnO has predominant advantages. A list of the electrical properties of the competing n-type thin films is summarized in Table 5.1. The mobility of ZnO thin film can be achieved as high as 1.1×10² cm²/(V·s).

Table 5.1 Electrical Properties of competing thin film technologies [Siddiqui (2012)]

<table>
<thead>
<tr>
<th>Figure of merit</th>
<th>a-Si TFT</th>
<th>Organic TFT</th>
<th>a-IGZO</th>
<th>Zinc Tin Oxide (ZTO)</th>
<th>ZnO</th>
</tr>
</thead>
<tbody>
<tr>
<td>μ (cm²/V·s)</td>
<td>1.5</td>
<td>0.02</td>
<td>14</td>
<td>43</td>
<td>110</td>
</tr>
<tr>
<td>I_{ON}/I_{OFF}</td>
<td>~10⁸</td>
<td>~10⁸</td>
<td>&gt;10⁵</td>
<td>10⁷</td>
<td>10</td>
</tr>
<tr>
<td>I_{ON} (pA)</td>
<td>0.1</td>
<td>1</td>
<td>0.1</td>
<td>1</td>
<td>0.01</td>
</tr>
<tr>
<td>V_{TH} (V)</td>
<td>2</td>
<td>~ 0.7</td>
<td>2.3</td>
<td>1.4</td>
<td>2</td>
</tr>
<tr>
<td>S (mV/decade)</td>
<td>300</td>
<td>170</td>
<td>200</td>
<td>180</td>
<td>100</td>
</tr>
</tbody>
</table>
5.3 Device Structure and Design

The main aim of this chapter is to simulate the thin–film transistor using ZnO as an active channel layer. Figure 5.2 shows the structure of ZnO channel TFT device. The structure is bottom gate with ZnO active layer. The SiO$_2$ gate oxide layer is used with ITO as a gate material. The process involve the generation of the thin film based TFT structures using Sentaurus TCAD software. Simulations of the same to obtain the electrical characteristics and hence the extraction of electrical parameters like threshold voltage, mobility and current on-off ratio will enable in determining the functioning characteristics of the device.

![Figure. 5.2 Structure of ZnO channel TFT device.](image)

The uniqueness of the thin film transistor technology lies in the composing materials and structure with few parameters on the substrate material and size. $V_{TH}$ measured in Volts, $I_{ON}/I_{OFF}$, field effect mobility in cm$^2$/V.s and subtheshold slope in V/decade are the parameters which determine the electrical performance of a TFT device. These parameters can be extracted from the transfer characteristics of the device obtained from simulation using sentaurus TCAD.
5.4 Device Simulation

The experiment involves design of ZnO based TFT in TCAD. Figure 5.3 shows the process flow of simulation using Sentaurus TCAD. The design of the structure and sequential procedure is as below:

![Device Design Process Flow Chart]

Figure. 5.3 Device Design Process Flow Chart
5.4.1 Generation of Structure using Sentaurus TCAD

Using the Sentaurus Structure Editor the 2D structure of the TFT is drawn as shown in Figure 5.4. Graphical User interface of Structure editor opens a window after pressing command line. This window has its three part. The menu bar, toolbars, and lists are in the upper part of the main window; the view window is in the center; and the command-line window is in the lower part of the main window. Contacts can be defined to allow the constructed device to be connected to outside power sources. The contacts name, sets, properties, edge color, thickness are defined for the specific structure. Figure shows the designed structure of the TFT with ZnO as an active channel layer.

Figure. 5.4 Simulation of two dimensional structure of ZnO channel TFT
5.4.2 Defining Doping in the structure using Sentaurus TCAD

A constant boron background doping of $1 \times 10^{15}$ cm$^{-3}$ in the silicon material is introduced by appropriate selection in the constant profile placement with defining proper placement name, material, species, and concentration in the command file. The doping profile is chosen with $1e^{+15}$ concentration of arsenic active dopants by adding the constant doping profile into the substrate. The incorporation of dopants increases mobility in the dielectric semiconductor interface of the device. The doping concentration of the structure is shown in Figure 5.5.

![Figure 5.5 Definition of doping in the designed structure](image)
5.4.3 Meshing strategy of the structure and generation of Mesh

After the device is structured, contacts are set and doping profile has been selected. The next step is called meshing. Sentaurus Mesh is a modular 2D and 3D mesh generator that can create both axis-aligned and tensor meshes to be used in simulators that use the box discretization or finite-difference time-domain (FDTD) methods for spatial device discretization. The generated mesh of the designed ZnO channel TFT is saved and viewed in visual as shown in Figure 5.6.

![Figure 5.6 Meshing structure for two dimensional simulation of ZnO channel TFT using Sentaurus TCAD](image_url)
Sentaurus Mesh produces triangles in the case of 2D devices and tetrahedral in the case of 3D devices. Generated grids can be loaded into Sentaurus Device and Sentaurus Process. Depending on the mesh generator used, Sentaurus Mesh produces different output formats.

The axis-aligned mesh generator always produces a TDR unstructured mesh. In Sentaurus Structure Editor, the mesh generation process is performed in two steps. The first step defines the meshing strategy, which includes the maximum and minimum meshing step definition in each device dimensions as well as the mesh refinement strategies.

The second part links the defined strategy from the first step to a specific target, which is, in general, a material, or a device region, or a user-defined evaluation window. Note that different device regions have different roles in terms of determining the device performance, thereby the required meshing strategies for these regions are typically different. Figure 5.6 shows the successfully generated mesh structure and strategy adopted for the min-max element size of build mesh.

5.5 Simulation Results

From the simulation of the device the gate-drain transfer characteristics and drain characteristics have been obtained as shown in Section 5.5.1 and 5.5.2. From the results thin film transistor parameters including subthreshold swing (SS), $I_{ON}/I_{OFF}$ ratio, threshold voltage ($V_{TH}$), and gate leakage current ($I_G$) were calculated, and are summarized in Section 5.5.3.
5.5.1 Transfer Characteristics

There is a good gate controllability in the n-channel ZnO TFTs. From the simulation of the device, the gate and drain current-voltage characteristics are obtained. Experimental data [Hoffman et. al (2003)] and simulation characteristics are shown in Figure 5.7.

![Graph showing transfer characteristics of simulated ZnO channel TFT](image)

Figure 5.7 Transfer Characteristics of Simulated ZnO channel TFT.

5.5.2 Drain Characteristics

Figure 5.8 shows the (V<sub>DS</sub>-I<sub>D</sub>) drain characteristics obtained from the Inspect module of the TCAD tool. Keeping the V<sub>GS</sub> bias constant at values of -0.5V, -1.5V, -2.5V; and -3.5V, the drain current was recorded as a function of V<sub>DS</sub>.
5.5.3 Electrical Performance Parameters

The thin film transistor parameters including subthreshold swing (SS), $I_{ON}/I_{OFF}$ ratio, $V_{TH}$, and gate leakage current ($I_G$), were calculated.

Figure 5.8 Drain Characteristics of the Simulated ZnO channel TFT.
Table 5.2 Summary of the Electrical parameters of ZnO Channel TFT

<table>
<thead>
<tr>
<th>Parameters (in units)</th>
<th>Calculated Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>On current (A)</td>
<td>$5.22 \times 10^{-8}$</td>
</tr>
<tr>
<td>$I_G$ Off current (A)</td>
<td>$1.35 \times 10^{-11}$</td>
</tr>
<tr>
<td>On-off ratio</td>
<td>$\sim 10^4$</td>
</tr>
<tr>
<td>$V_{th}$ (V)</td>
<td>4.8</td>
</tr>
<tr>
<td>$\mu_{FE}$ (cm$^2$/V.s)</td>
<td>$1 \times 10^4$</td>
</tr>
</tbody>
</table>

The achieved $I_{ON}/I_{OFF}$ ratio was approximately $\sim 10^4$, and the $SS = (dV_{GS})/[d(\log I_{DS})]$ approximately 216 mV/decade. The parameters have been derived from the method as described in Section 1.3.2 of Chapter 1. Table 5.2 summarizes the calculated values of the parameters.