ABBREVIATIONS

SRAM	Static Random Access Memory
I/O	Input /Output
ICs	Integrated Circuits
SoC	System-on-Chip
CPU	Central Processing Unit
CMOS	Complementary MOSFET
FG	Floating Gate
FGMOSFET	Floating Gate MOSFET
POLY1	First Poly-silicon Layer
POLY 2	Second Poly-silicon Layer
CG	Control Gate
FGSRAM	Floating Gate SRAM
LCT	Leakage Control Transistor
FGSLSRAM	Floating Gate Sleepy SRAM
FGLECSRAM	Floating Gate Leakage Control Transistor SRAM
FGSLLEC SRAM	Floating Gate Sleepy-Lector SRAM
SNM	Static Noise Margin
VTC	Voltage Transfer Characteristics
VDD	Supply Voltage
VDS	Drain Source Voltage
Gnd	Ground
DC	Direct Current

DRAM	Dynamic Random Access Memory
PDA	Personal Digital Assistant
lVth	Low threshold voltage
hVth	High threshold voltage
DRC	Design Rule Check
LVS	Layout Versus Schematic
QRC	RC Extraction
WL	Word Line
BL	Bit line
BL_bar	Bitline_ bar
PR	Pull-up Ratio
CR	Cell-Ratio
TWA	Write Access Time
DRV	Data Retention Voltage
BTBT	Band-to-Band Tunnelling
DIBL	Drain-Induced Barrier Lowering
FN	Fowler-Nordheim
GIDL	Gate Induced Drain Leakage
MTCMOS	Multi Threshold Voltage CMOS
INV1	Inverter 1
INV 2	Inverter 2
IVC	Input Vector Control
VN	Node Voltage
SS	Slow-Slow

FF	Fast-Fast
SF	Slow-Fast
FS	Fast-Slow
TT	Typical-Typical
PDP	Power Delay Product
TSA	Sense Amplification Time
SAs	Sense Amplifiers
LV	Low-Voltage
LP	Low-Power