

CONTENTS

DECLARATION	i
CERTIFICATE	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT	iv
CONTENTS	vi
LIST OF FIGURES	x
LIST OF TABLES	xvii
ABBREVIATIONS	xix
Chapter 1: Introduction	1-10
1.1 Introduction	1
1.2 Motivation	5
1.3 Problem statement	7
1.4 Organization of the rest of the thesis	7
Chapter 2: Background and Literature Survey	11-60
2.1 4T SRAM cell	11
2.2 6T SRAM cell	12
2.2.1 Read operation of 6T SRAM cell	14
2.2.2 Cell-ratio	15
2.2.3 Read access time	15
2.3 Write operation of 6T SRAM cell	16
2.3.1 Pull-up ratio	17
2.3.2 Write access time	17
2.4 Hold or standby operation	18
2.5 Data retention voltage	18
2.6 Static noise margin	18
2.7 Leakage mechanism in CMOS transistor	19

2.7.1	PN Junction reverse bias leakage (I_1)	20
2.7.2	Band-To-Band tunneling current (I_2)	21
2.7.3	Subthreshold leakage current (I_3)	21
2.7.4	Gate oxide tunneling current (I_4)	21
2.7.5	Hot carrier injection (I_5)	22
2.7.6	Punch through (I_6)	22
2.7.7	Gate induced drain leakage current (I_7)	22
2.8	Power dissipation components in digital CMOS circuits	24
2.9	Architecture of an SRAM unit	25
2.10	Simulation circuit of 6T SRAM cell	25
2.11	Floating gate MOSFET(FGMOS)	31
2.12	Why FGMOS?	35
2.13	Schematic of FGSRAM cell	36
2.14	Simulation results of 6T SRAM cell and FGSRAM cell	42
2.15	Literature survey	45
2.16	Analytical summary of relevant works	50
2.17	Existing leakage reduction technique	53
2.17.1	Sleepy transistor technique	53
2.17.2	Forced Stack technique	54
2.17.3	Sleepy Stack technique	55
2.17.4	Lector technique	56
2.17.5	ABC-MTCMOS technique	57
2.17.6	Sleepy keeper technique	58
2.17.7	Zigzag approach	59
2.17.8	Input vector control (IVC) technique	59
2.17.9	Galeor technique	60

Chapter 3: FGSRAM Cell Using Sleepy Technique	61-73
3.1. Sleepy technique	61
3.2. Stack technique	63
3.3. FGSRAM cell using sleepy technique	64
3.4. Simulation results	70
Chapter 4: FGSRAM Cell Using Lector Technique	74-86
4.1. Lector technique	74
4.1.1 Lector based CMOS inverter	76
4.2 FGSRAM cell using lector technique	77
4.3. Simulation results	83
Chapter 5: FGSRAM Cell Using Sleepy and Lector Technique	87-98
5.1. FGSRAM cell using sleepy and lector technique	87
5.2. Simulation results	93
Chapter 6: Peripherals in SRAM Architecture	99-112
6.1 FGSLLLEC SRAM cell	100
6.2 Decoder	100
6.2.1 Row decoder	100
6.2.2 Column decoder	101
6.3 Write driver	103
6.4 Pre-charge circuit	106
6.5 Control logic	108
6.6 Sense amplifier	110
Chapter 7: FGSLLLEC SRAM Architecture	113-137
7.1 Basic SRAM architecture	113
7.2 Topologies of 8x8 SRAM architectures	115
7.2.1 8x8 FGSLLLEC SRAM architectures using 8 precharge circuit	116

7.2.2	8x8 FGSLLES SRAM architectures using 1 precharge circuit	117
7.2.3	Proposed 8x8 FGSLLEC SRAM architecture using control logic	119
7.3	Layout design of 8x8 FGSLLEC SRAM architecture	122
7.3.1	DRC Test of 8x8 FGSSLLEC SRAM architecture layout	122
7.3.2	LVS Test of 8x8 FGSLLES SRAM architecture layout	123
7.3.3	QRC Test of 8X8 FGSLLEC SRAM architecture layout	124
7.4	Simulation results	125
7.4.1	Power delay product(PDP)	128
7.4.2	PVT analysis	129
	7.4.2.1 Average power consumption (μW) vs Temperature ($^{\circ}\text{C}$)	129
	7.4.2.2 Delay (ns) vs temperature ($^{\circ}\text{C}$)	131
	7.4.2.3 Average Power consumption (μW) vs supply voltage (V)	132
	7.4.2.4 Delay (ns) vs supply voltage (V)	134
7.5	Corner analysis of FGSLLEC SRAM architecture	135
Chapter 8: Conclusions and Future Prospects		138-139
8.1	Conclusions	138
8.2	Future prospects	139