ABSTRACT

Low power static random access memory (SRAM) design is an important part of many applications. On-chip cache represents a substantial portion of the chip and SRAM used as cache memory in various kinds of portable devices/systems like mobile phones, microprocessors, microcontrollers, laptops and computers etc. because of its high speed, low cost and low power consumption. Future growth of SRAM is expected in both portable devices and high-performance processors. So, the rapid growth of battery operated handheld devices has increased the demand of low-power design a priority in recent years. Power dissipation has become a major design challenge to the VLSI designers as CMOS technology scaled to nanometer region. The leakage power becomes dominant due to the second order effects of the transistors in nanometer region. There are various sources of active and stand-by power consumption in SRAM. The active power consumption consists of the power consumed by decoders, bit lines, data lines, sense amplifier and other peripheral circuits. Energy consumption is the major concern in memory design. Low power SRAM is essential to achieve higher reliability and longer battery life for portable application. Power dissipation can be minimized by switching the circuit in off mode and by using low supply voltage.

This thesis focuses on the design of stable SRAM array using floating gate (FG) MOSFET and on three different low power techniques to achieve a low power and high speed SRAM. Three different low power SRAM cells namely FG sleepy, FG lector and FG sleepy lector have been designed and implemented on Cadence Virtuoso environment on 45 nm CMOS process technology. Complete memory architecture using proposed floating gate sleepy lector (FGSLLEC) SRAM cell and necessary peripheral circuits have been designed. A novel control logic circuit has been proposed in place of pre-charge circuit that reduces huge area and power dissipation. Pre-layout and post layout simulation of the architecture has been done. During layout of the SRAM design rule check (DRC), layout versus schematic (LVS) and RC extraction (QRC) have been done successfully. From the post layout simulation result of all architectures (architecture with 8 precharge, architecture with 1 precharge and architecture with control logic) it is observed that power delay

product in FGSLLEC SRAM architecture using control logic is decreased by 99.17% than 6T SRAM and 94.26% than FGSRAM architecture. As the power delay product of FGSLLEC SRAM cell is smaller than others, hence its quality and performance is better. From delay analysis it is observed that the delay also decreased in FGSLLEC SRAM architecture than 6T SRAM architecture and FGSRAM architecture using control logic circuit. In all proposed architectures and cells, the cell properties, i.e. read delay and static noise margin (SNM), are maintained. Also, to estimate the performance analysis of the architecture, PVT (process, voltage and temperature) analysis has been done.