Publications

Journals

[1] K. B. Ray, S. K. Mandal and B. S. Patro, "Low Power High speed Low Leakage Floating Gate SRAM Cell using Lector Technique“, Indian Journal of Science and Technology**,** vol.9, no.45, pp.1-6, (**Scopus**), Dec. 2016.

[2] K. B. Ray, S. K. Mandal and B. S. Patro, “Low Power FGSRAM Cell using Sleepy and Lector Technique“, Indonesian Journal of Electrical Engineering and Computer Science (**Scopus**) vol. 4, no. 2, pp.333-340, Nov. 2016.

[3] K. B. Ray, S. K. Mandal and B. S. Patro, "Low Power High Stability SRAM Cell with Combined Effect of Sleep- Stack and Diode Gated Technique “, which has been already communicated to the journal site "JESTR“ (**Scopus**), Nov. 2016.

[4] K. B. Ray and S. K. Mandal, “Low Power, High Speed 8×8 FGSLLEC SRAM Architecture Using Advanced Control Logic Circuit", to be communicated (**Scopus**), 2017.

[5] K. B. Ray, N. Ghosh, B. Chowdhury and S. K. Mandal, ‘'Low power 1 Bit SRAM Architecture Design Using GALEOR Technique'‘, International Journal of Engineering Research & Technology(IJERT) Conference Proc. Special Issue , pp.44-49, 2016.

[6] B. Chowdhury, K. B. Ray, N. Ghosh and S. K. Mandal, " Design and Analysis of Low Power, High Speed 3-2 Compressor Architectures in 45-nm Technology'‘, International Journal of Engineering Research & Technology(IJERT), Conference Proc. special issue, pp.24-28, 2016.

[7] A. Pattnaik and K. B. Ray " Leakage Power Minimization in Memory Design using an adaptive technique to optimize the Body Biasing Voltage“, International Journal of Scientific & Engineering Research, vol.5, no.3, pp.1253-1261, Mar. 2014.

Conferences

[1] B. Senapati, G. L. Kumar M and K. B. Ray, "High Resolution Reconfigurable Biopotential Processor for Portable Biomedical Application", 2nd International Conference on Devices for Integrated Circuit (DevIC), IEEE EDS, Mar. 2017.

[2] K. B. Ray, S. S. Das and S. K. Mandal, "Multi Threshold Floating Gate SRAM In 180nM Technology", National Conference on Devices and Circuits (NCDC - 2015), pp.138-141, Feb. 2015.

[3] K. B. Ray, P. P. Nanda and S. K. Mandal, "One Bit-Line Multi-Threshold SRAM Cell with High Read Stability", National Conference on Devices and Circuits (NCDC - 2015), pp.156-158, Feb. 2015.

[4] K. B Ray and S. K. Mandal, "Low Power SRAM Design", Participated in the poster competition held during "National Science Day" celebration, KIIT University, Bhubaneswar, Feb. 2014.

[5] S. S. Das, K. B. Ray and S. K. Mandal, "Low Power FGSRAM " Participated in the Poster Presentation in IEEE EDS Bhubaneswar Kolkata Mini-Colloquium on 'Advanced Electronic Devices and Circuits' jointly organized by IEEE EDS Calcutta Chapter, ED University of Calcutta Student Branch chapter, ED Heritage Institute of Technology Student Branch Chapter and School of Electronics Engineering, KIIT University, Dec. 2014.

[6] P. P. Panda, K. B. Ray and S. K. Mandal, "Low Power Single Bit-Line SRAM Design" Participated in the Poster Presentation in IEEE EDS Bhubaneswar Kolkata Mini-Colloquium on 'Advanced Electronic Devices and Circuits' jointly organized by IEEE EDS Calcutta Chapter, ED University of Calcutta Student Branch chapter, ED Heritage Institute of Technology Student Branch Chapter and School of Electronics Engineering, KIIT University, Dec. 2014.