CHAPTER 8

CONCLUSIONS AND FUTURE PROSPECTS

8.1 Conclusions

The broad focus of this dissertation is that of architectural solutions to inherent in modern VLSI transistor technology. To the belongings of severe supply voltage fluctuations lowering supply voltage makes chips more inclined, which can direct to errors. For years of technology development, density-scaling is always the first consider factor of semiconductor industries in order to increase speed, achieve better performance and reduce power consumption as much as possible. The important aspect of this thesis was to simulate results for an 8×8 FGSLLEC SRAM Architecture for a 1 V of power supply voltage. The area of concentration was for a relatively low power SRAM as compared to the SRAM available in market.

This thesis work focuses on low power high speed SRAM cell design using FG MOSFET. Three different SRAM cell namely FG Sleepy, FG Lector and FG Sleepy-Lector have been designed and implemented on Cadence Virtuoso on 45 nm CMOS process technology. Complete memory architecture with proposed SRAM cells has been designed. A novel control logic circuit has been proposed in place of pre-charge circuit which improved overall power consumption and other performances. From power and delay analysis it is observed that the both power and delay are decreased in FGSLLEC SRAM architecture than other architectures. Also from the post layout simulation result of all architectures it is observed that power delay product in FGSLLEC SRAM architecture using control logic has been decreased 99.17% than 6T SRAM and 95.56% than FGSRAM Architecture. As the power delay product of FGSLLEC SRAM Cell is smaller than others, hence its quality and performance is better.

8.2 Future Prospects

As the demand of low power memory is growing day-by-day for more portable devices, future aspect of this work is that the SRAM can be extended to a low power design using low voltage keeping the read and write speeds to the same level or with even better results. Also the designers may examine on the voltage reliability, the impact of other power management techniques. The size of the SRAM cells can be reduced with slight increase in the SA size so that we get better read data at the output. The existing techniques can be improved in future works in accordance with the advancing fabrication methodologies to obtain more improved performance of the memories and other operational circuits. Other leakage mechanisms like gate current due to hot-carrier injection, gate induced drain leakage, and channel punch will strongly contribute to the total leakage current. Designing a SRAM cell that can reduce the effect of all of these leakage mechanisms is a big challenge in 45nm the design could be extended to ultra-low-power SRAM using lower stronger design. Peripheral device like sense amplifier and decoder need to be revised to lower their power consumption. And to achieve a ultra-low-power design, new threshold SRAM cells could be used to make system could work at low supply voltage without at the cost of losing stability.