CHAPTER 6

PERIPHERALS IN SRAM ARCHITECTURE

An SRAM unit consists of several periphery blocks which facilitate access to the cells for the read or write operation. To achieve high speed of operation and electrical integrity the peripherals used in architecture are SRAM cell, decoders (column and row), write driver circuit, precharge circuit, control logic circuit and sense amplifier.

A decoder decodes the binary encoded input address to indicate the physical location of the addressed cell. To communicate with the cell during write and read operation, the bit-line and complement of the bit-line are interfaced by the write drivers and sense amplifiers (SAs) respectively. Appropriate timing signals are given for the active operation of the write driver, word line and sense amplifier throughout the write or read operation.

Figure 6.1 Block Diagram of SRAM Architecture with all Peripheral Circuits
6.1 FGSLLEC SRAM Cell

FGSLLEC SRAM cell is formed by a cross coupled floating gate MOS inverter combined with low power sleepy and lector technique. Two access transistors are connected to communicate with the bit-lines (BL and BL-bar). During hold operation, the access transistors are disconnected the SRAM cell from the BL and BL_bar and the data is latched within the inverters [108]. Two cross coupled inverters containing two bit lines complement to each other for communicating with outsides the cell. To stay away from accidently writing a '1' (one) into the cell [109] normally low W/L ratio is considered for all the cells. Moreover, watchful sizing is essential when designing a SRAM cell for proper read and write operation. The details of FGSLLEC SRAM cell used in SRAM architecture is explained in Chapter 5.

6.2 Decoder

Two types of decoders are used in SRAM architecture. Row decoder and Column decoder. Row decoders select the word line of the accessed cell. Column decoders select the bit lines of the accessed cell and connect it to the corresponding read and write circuit [110].

6.2.1 Row Decoder

Address decoders are known as row decoder. For one memory bank, the address is divided into two parts; the first part is used for the row decoder, while the second is used for column decoder. Read or write cycle time strongly depends on the row decoder. therefore, it is the critical path of the read/write cycle. Row address decoder is an essential element in an SRAM array. NAND and NOR gates were considered for the decoder design. Using delay and power consumption analysis, it was found that the NAND gate is faster than the NOR gate. In SRAM memory, two 3-to-8-line decoders are used named as row decoder and column decoder respectively. Depending on the row address inputs one of the input lines on the decoder goes low. All cells in that particular row are selected. The next task is to select one particular column. The column is selected from the column decoder. The columns pass transistors which gets inputs from the column decoder, which in turn receives input
from the column address lines and the output of the column decoder are passed to the gates of the pass transistors. This selects only one particular column. Thus, the combination of the row and the column decoder together selects one particular cell of SRAM at a time. The decoders are controlled by a clock because the SRAM is synchronous. The negative edge of a clock will allow the address to be read into the decoder, both column and row are enable the transistors used for precharging. The highest operation frequency that can be achieved by a memory array is strongly dependent on the speed of the row decoder. The row address and activation of one single row can be selected by the row selection circuit. The same row can be shared by the entire word line signals of the row. The row selection circuit is worked on a multiplexor logic. The other lines remain at high position when a single line is worked at low.

The required cell is selected by the column decoder and row decoder onto which the data will be read and the data will be written. In simulation, the input address is decoded by a row decoder and chose the word line. Just a single line is chosen of the row when performing a read or write operation. In the SRAM cell arrangement [111-112] the number of rows is the same to the number of word lines. A 3×8 decoder [98] is required with a view to plan an 8×8 SRAM architecture and the same is shown in the Figure 6.2. A 3-bit address has been given to the row decoder and a single row is selected by it. In row decoder design the inputs are taken as A, B and C.

6.2.2 Column Decoder

In the memory array a particular column is selected by the column decoder which is writing or reading the data of the particular memory cell. The column selector is worked on the similar principles as the row decoder. The data flows either from the data input signal to the cell (write cycle) or from the memory cell to the data output signal (read cycle) which is the major change [112]. The column decoder is also a 3-to-8-line decoder like row decoder, but the name of the input signals are D, E and F.
Figure 6.2 Simulation Circuit of 3-to-8 Line Decoder

Figure 6.3 Symbol of 3-to-8 Line Decoder
The simulation circuit, the symbol and the output wave form of the decoder circuit is shown in Figure 6.2 to Figure 6.4 respectively.

### 6.3 Write Driver

A horizontal word line is shared by a row of bit cells. For the write operation in the memory cell the component which is act as the main component of the total architecture is the write driver. One key factor is that when sense amplifier is on then write driver is in off state and when sense amplifier is off then write driver is in on state. This means simultaneously read and write operation is not done in the SRAM architecture.
Figure 6.5 Schematic of Write Driver Circuit

Figure 6.6 Simulation Circuit of Write Driver
The schematic diagram, simulation circuit, output waveform and symbol of write driver circuit are shown from Figure 6.5 to Figure 6.8 respectively. The write driver circuit is enabled by the active low WRITE_ENABLE signal shown in Figure 6.5.

Figure 6.8 shows when the WRITE_ENABLE signal is low the output of write driver (BL) is same as DATA_IN signal and the BL_bar is the complement of the DATA_IN signal.
6.4 Precharge Circuit

A precharge circuit is connected between the set of bit lines for each column. All the way through the precharge transistors and the equalizer the entire bit lines go back to their usual default situation at the stop of the write function and ready to read function. The most important component of dynamic power is due to precharging. The dynamic power overheads reduces by much more factor [108], [112] when precharge consumes no power.

![Figure 6.9 Schematic of Precharge Circuit](image)

The precharge circuit consists of three PMOS transistors (T1, T2 and T3), which are turned on and off by a shared enable signal PRE as shown in Figure 6.9.

![Figure 6.10 Simulation Circuit of Precharge Circuit](image)
The precharge simulation circuit and the symbol of the precharge circuit is shown in Figure 6.10 and Figure 6.11 respectively. PMOS transistors are normally used in pre-charge circuit as they pass VDD [113]. The PMOS transistor T3 between the two bit lines is essential to guarantee that there is no voltage difference between the two lines by the end of the precharge cycle. Otherwise, the read access time is longer to overcome any initial voltage variation among the bit lines. Prior to read operation the two bit lines BL-out and BL-bar-out are precharged to VDD by transistor 1 (T1) and transistor 2 (T2) when PRE_EN is active low. An extra equalizer transistor 3 (T3) is used which helps recharging bit lines and equalizes the voltages of the bit line pair during the precharge period. Perfect equalized voltages of BL_out and BL_bar_out are desirable before a read operation is initiated [114]. For write operation, precharging is not required but in high speed design, as the type of the access operation is not known the bit lines are precharged after each access operation to reduce the access time.
6.5 Control Logic

Two control logic circuits are used in this chapter to generate BL and BL_bar signals for SRAM cells.

The control logic circuit for BL and BL_bar is shown in Figure 6.12 (a) and Figure 6.12 (b) respectively. The circuit is designed in such a way that when EN = 0, CP1 and CP2 transistors turns on and makes both BL_out and BL_bar_out high. In this position, the proposed architecture does the read operation. When EN = 1, transistors CN1 and CN2 turns on and transistors CP1 and CP2 turns off. Hence, BL_in and BL_bar_in are coming out through BL_out and BL_bar_out lines of control logic circuit. During this period sense amplifier turns off and write operation takes place.
Figure 6.13 Simulation Circuit of Control Logic for BL and BL_bar

Figure 6.14 Symbol of Control Logic Circuit for BL and BL_bar

The simulation circuit of control logic circuit for BL and BL_bar is shown in Figure 6.13 (a) and 6.13 (b) respectively. The symbol of both BL and BL_bar control logic circuit is shown in Figure 6.14 (a) and 6.14 (b) respectively.
6.6 Sense Amplifier

In computer memory architecture, a sense amplifier is one of the components of the read/write circuitry. The memory cells are weak due to their small size, and hence cannot discharge the bit lines fast enough [115]. To sense the levels of the logic from a bit line which represents a data bit (1 or 0) placed in a memory cell on the chip is the main function of a sense amplifier. It is mainly used to convert a small voltage swing signal (difference of bit line voltages) to a full voltage swing [109], [116] to identify the levels of the logic, so properly the data will be interpreted at the memory chip's output terminal. The performance of sense amplifier strongly affects the power consumption and speed of whole SRAM design hence the memory performance is better by dropping both power dissipation and sensing delay. The data reading operation from the SRAM cell is performed by the sense amplifier. In addition by sensing a small variation in voltage on the bit lines [117] on the whole SRAM chip sense amplifier helps to decrease the delay times, reduces the power consumption and restore the imaginative signal. To accomplish performance, functionality and reliability of memory chips a vital job is played by sense amplifiers.

A sense amplifier needs to satisfy a few electrical requirements for proper operation in the SRAM unit. First, the required minimum differential voltage swing at the input of sense amplifier should be smaller than the minimum differential voltage that is developed over the bit lines by the SRAM cell. Second, the sense amplifier should be able to provide the output within the sense amplification time (TSA) once it exercises minimum input differential voltage. The sensing threshold voltage, power consumption and reliability are major concerns in sense amplifier design. Sensing threshold voltage is the required minimum read bit line voltage drop that can be successfully detected by the sense amplifier. Sense amplifiers that have lower sensing threshold voltages offer higher data access speed and lower power consumption. Variation of sensing threshold voltage due to parameter fluctuations may cause read failure in an SRAM array.

Sense amplifiers of differential type are used to read the data quickly and are designed in this chapter. The advantage of this circuit is to get better speed and noise immunity
of the circuit. The sense amplifier of differential voltage type can amplify and attenuates common-mode noise signals. When difference is created between the bit lines, sense amplifier senses it and amplifies it to give the output [109].

Figure 6.15 Schematic of Sense Amplifier Circuit

The Figure 6.15 shows the schematic of sense amplifier circuit. In this Figure 6.15, when SE_EN = 0, it makes SP1 and SP2 as in on position and other transistors (acts like differential amplifier) to calculate the difference of bit line (BL) and bit line bar (BL_bar).

Figure 6.16 Simulation Circuit of Sense Amplifier
Figure 6.16 shows the simulation circuit of sense amplifier. The symbol and the output waveform of the sense amplifier is shown in Figure 6.17 and Figure 6.18 respectively. In Figure 6.18, BL and BL_bar are the inputs to the sense amplifier and OUT and OUT_bar are the outputs of the sense amplifier.