CHAPTER 3

FGSRAM CELL USING SLEEPY TECHNIQUE

Due to technology scaling the device size shrinks to nanometer range. In this nanometer technology era static power of CMOS circuits has become major concern of the designer. Supply voltage is reduced and device parameters such as gate oxide thickness, channel length and threshold voltage is decreased with scaled technology. The drawbacks here is subthreshold leakage current which increases exponentially with decrease in threshold voltage and also performance can be degraded. This chapter presents sleepy technique which is used for static power reduction. This technique generally reduces subthreshold leakage current.

3.1 Sleepy Technique

Threshold and supply voltages are shrinking with the CMOS technology scaling. The subthreshold leakage current increases exponentially with decreasing threshold voltages (Vth). In nanometer technology era, more than 40% of the whole power dissipation of ICs is due to leakage currents. Due to higher integration of transistors on a single die, the total power consumption of ICs will be dominated soon by the leakage currents. Researchers are trying to find new techniques to reduce leakage current. The sleepy technique is the most widely used technique for leakage current reduction. It is also known as gated-Gnd and gated-VDD technique [91] or “power gating” technique.

![Figure 3.1 Circuit Diagram of Sleepy Technique](image-url)
The sleepy technique is also known as multi threshold voltage CMOS (MTCMOS) technique and proposed by Motoh et al. In this MTCMOS technique two different threshold voltages are used in the circuit. Here, both sleepy transistors PMOS and NMOS (S and \(\overline{s}\)) are positioned between pull up network and VDD and Gnd and pull down network respectively \([91-92]\) which is shown in Figure 3.1.

Sleepy transistors are high threshold voltage (hVth) transistors connected in series with low threshold voltage (lVth) logic \([93]\) and are used to control the subthreshold leakage current. The leakage power consumption can be minimized by using various high threshold transistors. Due to the non-zero interconnect delay, different memory cells have different write and read delays for fast access. Major advantages of high threshold voltage transistors includes no hardware overhead, no delay overhead, no significant change in the design flow of SRAM and static noise margin (SNM) improvement.

When the logic circuits are inactive the sleepy transistors are turned off. MTCMOS is used to reduce leakage current during inactive mode and to achieve high speed in active mode. The low threshold voltage (lVth) transistors are used to realize the logic. During inactive mode to minimize leakage dissipation \([94]\) high threshold voltage (hVth) transistors are used to cut off the low threshold voltage (lVth) transistors from ground and supply voltage. The circuit is turned off by the sleepy transistors (PMOS and NMOS) where the power rails are cut off. In this technique the reduction of leakage power is due to two reasons, first transistor stacking and second low subthreshold leakage current of high threshold voltage transistor (hVth) transistors. As the sleepy transistors are connected in series with the pull up and pull down transistor of the network, hence this technique acts like transistor stacking.
3.2 Stack Technique

Figure 3.2 shows the stack technique. When two or more transistors are tied up in series and all are in sleepy mode, the subthreshold leakage current decreases. This technique is called stacking technique [92], [95]. The stacking technique describes that the circuit consumes less leakage current if two or more transistors are connected in series and all are in sleep mode [96-97]. In Figure 3.2 when both NMOS (N₁ and N₂) transistors are in sleep mode, due to little positive drain current the intermediate node ('N') voltage (VN) is positive. This positive intermediate voltage results three effects [92], [95].

- The gate to source voltage ($V_{GS1}$) of N₁ suppresses as a consequence of positive voltage at node N.

- In a consequence of 'N' node's positive voltage, the body to source voltage ($V_{BS1}$) of N₁ drops down to negative, developing in a rise in the threshold voltage (extra body effect) of N₁ transistor and therefore suppressing the sub-threshold leakage current.

- Because of node voltage ('VN') is positive, the drain to source voltage (VDS) of N₁ transistor suppresses. Hence the sub-threshold voltage rises (small amount of DIBL effect) which shows to suppressing the sub-threshold leakage current.
Both high threshold voltage (hVth) and low threshold voltage (lVth) transistors are used in above technique to suppress leakage current [82]. The leakage current can be suppressed by using high threshold voltage transistors and better performance can be achieved by low threshold voltage transistors. When more than two stacked transistors are turned off, the leakage power consumption is reduced than that of a single transistor due to stacking effect [94].

### 3.3 FGSRAM Cell using Sleepy Technique

Sleepy transistor technique explained in Section 3.1 has been used for FGSRAM cell design. Using sleepy transistors, the gated-VDD FGSRAM cell blocks pull-up networks from the VDD rail and/or blocks pull-down networks from the Gnd rail [92]. Low-leakage power consumption can be achieved by the gated-VDD SRAM cell from both the high threshold voltage (hVth) sleepy transistors and stacking effect.

![Figure 3.3 Schematic of FGSRAM Cell](image)

The Figure 3.3 shows the schematic diagram of floating gate SRAM cell using sleepy transistors (FGSLSRAM cell). As the floating gate SRAM cell contains two inverters, two PMOS transistors (M7 & M8) and two NMOS transistors (M9 & M10) are applied here as sleepy transistors. All sleep transistors used in the circuit are hVth
transistors. High threshold transistors are used to achieve lower subthreshold current and low threshold transistors are used to improve the delay. M3 and M4 are the two access transistors. So, low threshold transistors are applied in the SRAM cell and because of these thin channel devices, switching time will be reduced which provides fast access of the cell [27].

Figure 3.4 Simulation Circuit of FGSLSRAM Cell

The simulation circuit of FGSLSRAM cell is shown in Figure 3.4. Here, the width of the pull-up transistors (M5, M6, M7 and M8 in Figure 3.3) and pull down transistors (M1, M2, M9 and M10 in Figure 3.3) are taken as 145 nm and 250 nm respectively. The sizes of the sleepy transistors are taken as 145 nm (M7 and M8) and 250 nm (M9 and M10) respectively. The size of the access transistors (M3 and M4) are 200 nm each. The length of each transistor is taken as 45 nm. The supply voltage and wordline voltage is given as 1 V and 750 mV respectively. For write '0' operation the voltage at BL is given as zero and BL-bar is given as one. It is given just reverse for write '1' operation. During Write '0' operation the transistors M1, M6, M8 and M9 turn on and during write '1' operation the transistors M2, M5, M7 and M10 of the
SRAM cell turn on. During read operation sense amplifier is enabled and output is taken from OUT and OUT_bar of sense amplifier.

Figure 3.5 DC Analysis of FGSLSRAM Cell

DC analysis of FGSLSRAM Cell is shown in Figure 3.5. In this figure V1 is the output voltage at node "1" and V2 is the output voltage at node "2". Node 1 and Node 2 is shown in schematic Figure 3.3.

Figure 3.6 Transient Analysis of FGSLSRAM Cell
Figure 3.6 shows the transient analysis of FGSLSRAM cell. This analysis shows the output voltage of two inverters vs time. Here, it is observed that the voltage swing is 100% which indicates better stability and good performance of the cell. In Figure 3.6 V1 and V2 are the node voltages of the SRAM cell.

![Power Consumption Curve of FGSLSRAM Cell](image1)

**Figure 3.7 Power Consumption Curve of FGSLSRAM Cell**

Figure 3.7 shows the power consumption of FGSLSRAM cell. It illustrates that with the increase in supply voltage the power consumption increases.

![Write '0' Leakage Current Curve of FGSLSRAM Cell](image2)

**Figure 3.8 Write '0' Leakage Current Curve of FGSLSRAM Cell**
Figure 3.8 and 3.9 shows the write '0' and write '1' leakage current curve of FGSRAM cell. Taking this two curves write '0' and write '1' leakage power is calculated.

Figure 3.10 Write SNM Curve of FGSLSRAM Cell
Figure 3.11 Simulation Circuit of FGSLSRAM Cell for Read Operation

Figure 3.12 Read SNM Curve of FGSLSRAM Cell

The write SNM curve, the read simulation circuit and the read SNM curve is shown from Figure 3.10 to Figure 3.12. In the SNM curve voltage 1 is the output voltage of inverter 1 and voltage 2 is the output voltage of inverter 2.
3.4 Simulation Results

From simulation results it is observed that the leakage current is reduced in FGSLSRAM cell than FGSRAM cell both due to sleepy and stacking effect explained in sec 3.1 and 3.2. The simulation results for write and read operation of FGSRAM and FGSLSRAM cell are represented in Table 3.1 to Table 3.4.

Table 3.1: Write '0' Operation of FGSRAM Cell and FGSLSRAM Cell

<table>
<thead>
<tr>
<th>SRAM Cell</th>
<th>Leakage Power</th>
<th>Delay</th>
<th>Power Consumption</th>
<th>SNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>FGSRAM</td>
<td>3.4 nW</td>
<td>296.9 ps</td>
<td>228.5 nW</td>
<td>424.2 mV</td>
</tr>
<tr>
<td>FGSLSRAM</td>
<td>1.2 pW</td>
<td>210.7 ps</td>
<td>102.6 nW</td>
<td>636.3 mV</td>
</tr>
</tbody>
</table>

Table 3.1 shows the leakage power, delay, power consumption and SNM for write '0' operation of FGSRAM cell and FGSLSRAM cell. It is observed that leakage power in FGSLSRAM cell is reduced 99.9% and delay is reduced 29% than FGSRAM cell.

Table 3.2: Write '1' Operation of FGSRAM Cell and FGSLSRAM Cell

<table>
<thead>
<tr>
<th>SRAM Cell</th>
<th>Leakage Power</th>
<th>Delay</th>
<th>Power Consumption</th>
<th>SNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>FGSRAM</td>
<td>3.7 nW</td>
<td>152.6 ps</td>
<td>228.5 nW</td>
<td>424.2 mV</td>
</tr>
<tr>
<td>FGSLSRAM</td>
<td>1.7 pW</td>
<td>95.5 ps</td>
<td>102.6 nW</td>
<td>636.3 mV</td>
</tr>
</tbody>
</table>

Table 3.2 shows the leakage power, delay, power consumption and SNM for write '1' operation of FGSRAM cell and FGSLSRAM cell. It is observed that leakage power in FGSLSRAM cell is reduced 99.9% and delay is reduced 37% than FGSRAM cell.

Again from Table 3.1 and Table 3.2 it is concluded that power consumption decreases 55% and SNM improves 32% both for write '0' and write '1' operation.
Table 3.3: Read '0' Operation of FGSRAM Cell and FGSLSRAM Cell

<table>
<thead>
<tr>
<th>SRAM Cell</th>
<th>Leakage Power</th>
<th>Delay</th>
<th>Power Consumption</th>
<th>SNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>FGSRAM</td>
<td>3.4 nW</td>
<td>297.6 ps</td>
<td>4.0 µW</td>
<td>247.4 mV</td>
</tr>
<tr>
<td>FGSLSRAM</td>
<td>1.2 pW</td>
<td>211.3 ps</td>
<td>3.8 µW</td>
<td>707.1 mV</td>
</tr>
</tbody>
</table>

Table 3.3 shows the leakage power, delay, power consumption and SNM for Read '0' operation of FGSRAM cell and FGSLSRAM cell. It is observed that leakage power in FGSLSRAM cell is reduced 99.9% and delay is reduced 29% than FGSRAM cell.

Table 3.4: Read '1' Operation of FGSRAM Cell and FGSLSRAM Cell

<table>
<thead>
<tr>
<th>SRAM Cell</th>
<th>Leakage Power</th>
<th>Delay</th>
<th>Power Consumption</th>
<th>SNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>FGSRAM</td>
<td>3.4 nW</td>
<td>153.2 ps</td>
<td>4.0 µW</td>
<td>247.4 mV</td>
</tr>
<tr>
<td>FGSLSRAM</td>
<td>1.7 pW</td>
<td>95.9 ps</td>
<td>3.8 µW</td>
<td>707.1 mV</td>
</tr>
</tbody>
</table>

Table 3.4 shows the leakage power, delay, power consumption and SNM for read '1' operation of FGSRAM cell and FGSLSRAM cell. Here, it is observed that leakage power in FGSLSRAM cell is reduced 99.9% and delay is reduced 37% than FGSRAM cell.

Further, from Table 3.3 and Table 3.4 it is concluded that power consumption decreases 5% and SNM improves 65% both for read '0' and read '1' operation.

Hence, from Table 3.1 to Table 3.4, it is concluded that FGSLSRAM cell achieves better performance than FGSRAM cell.
Figure 3.13 Power Consumption Comparison of FGSRAM Cell and FGSLSRAM Cell

Figure 3.14 Delay Comparison for Write and Read operation of FGSRAM Cell and FGSLSRAM Cell

Figure 3.15 SNM Comparisons for Write and Read Operation of FGSRAM and FGSLSRAM Cell
Table 3.5: Hold Operation of FGSRAM Cell and FGSLSRAM Cell

<table>
<thead>
<tr>
<th>SRAM Cell</th>
<th>Leakage Power</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>FGSRAM</td>
<td>24.8 nW</td>
<td>24.8 nW</td>
</tr>
<tr>
<td>FGSLSRAM</td>
<td>1.7 nW</td>
<td>1.7 nW</td>
</tr>
</tbody>
</table>

Table 3.5 shows the hold operation of FGSRAM cell and FGSLSRAM cell. It shows that both leakage power and power consumption decreases 93% respectively.

Sleepy technique is applied with FGSRAM cell as shown in Figure 3.3. Multi threshold voltages are used in this technique. Normal SRAM cells have lower threshold voltages and the higher threshold voltages are sleep transistors which operates as a combined effect of sleep and stack [76], [98]. The SRAM cell has been designed and simulated in the Cadence Virtuoso environment on 45 nm standard CMOS technology. The results obtained for different operations are given in the comparison table from Table 3.1 to Table 3.5. From the tables it is observed that the power consumption is reduced significantly than conventional FGSRAM cell both for read, write and hold operation. Leakage power is reduced and stability of the cell also improved. But power consumption for read operation is not satisfactory which is only 4% and write stability is not so good as read stability.

However, the area is increased by extra sleepy transistors. Again the limitation to this technique is the floating output in sleep mode. So, the result of the technique is a floating output voltage and damage of the state. Using sleep transistors the state-destructive techniques cut off transistor (pull-down, pull-up or both) networks from ground (Gnd) or supply voltage (VDD). Moreover, the pull-down and the pull-up networks will be floating values. Therefore, the networks will be unable to find state for the period of sleep mode. These floating values considerably bang the wake up time and power of the sleep technique owing to the necessity to refresh transistors which missing state through sleep.

So, a new low power technique named lector with FGSRAM called FGSLSRAM cell and is presented in the next chapter.