CHAPTER 1
INTRODUCTION

1.1 Introduction

In present days due to the high demand for hand-held devices like laptops, notebooks, toys, automobiles, digital devices and memory cards, static random access memories (SRAMs) have gained a quick progress of low-voltage, low-power memory design. SRAM is used in high capacity memory design because of its less complex structure and higher density.

SRAM is one of the major blocks of embedded cache memory and occupies 90% of the die area [1]. It has become the major data storage space. The basic function of the SRAM is to store data, hold it and then output the data on the input/output (I/O) lines. Mobile device normally operates in the inactive mode. So, the device battery life is highly affected by the standby leakage power. Major part of the active mode energy consumed in current high performance integrated circuits (ICs) is due to leakage current. In system-on-chip (SoC) and high-performance processors, SRAM block is the major source of leakage current. To achieve better system performance, reliability and efficiency, reduction of area and power consumption of memories are extremely essential since memories are important part of most of the digital devices. Therefore, many researchers have focused on the design of low leakage SRAM.

SRAM is preferred in “on-chip memories” due to its high speed. On-chip memories contribute to a large part of power consumption of SoCs. The energy loss in memories is due to bit lines, word lines, address decoders and peripheral circuits. Power dissipation is the major design concern of SoC due its high speed and increased integration [2]. Reduction in power dissipation of SRAM will not only reduce the overall system power consumption, but also increase the yield and improve the SoC reliability [3]. This thesis focuses on reduction of power consumption mainly the leakage power and delay of SRAM design. Also, this thesis carefully examines various low power circuit techniques which are used combinely to achieve low power

operation, although process [4-5] and supply [6-11] scaling stay the largest drivers of high speed low power design.

The main challenge in SRAM cell design is its stability. This stability identifies change in memory during operating conditions and process variation. The objective is, even if in the presence of noise, the memory should operate perfectly. In the existence of DC noise, static noise margin (SNM) gives the stability of SRAM cell and can be measured from the voltage transfer characteristic (VTC) of two cross coupled inverters of the SRAM cell. The minimum amount of DC noise voltage required to change the state of the SRAM cell is known as SNM [12].

SRAM is used in most portable and battery-operated devices which requires low power consumption and less area. It is also used in processors which requires less write and read timing. It has been observed that stability of SRAM cell is affected with decrease in supply voltage (VDD) [13]. So, these goals can be achieved by optimizing the cell ratio and modifying the pre-charge circuit.

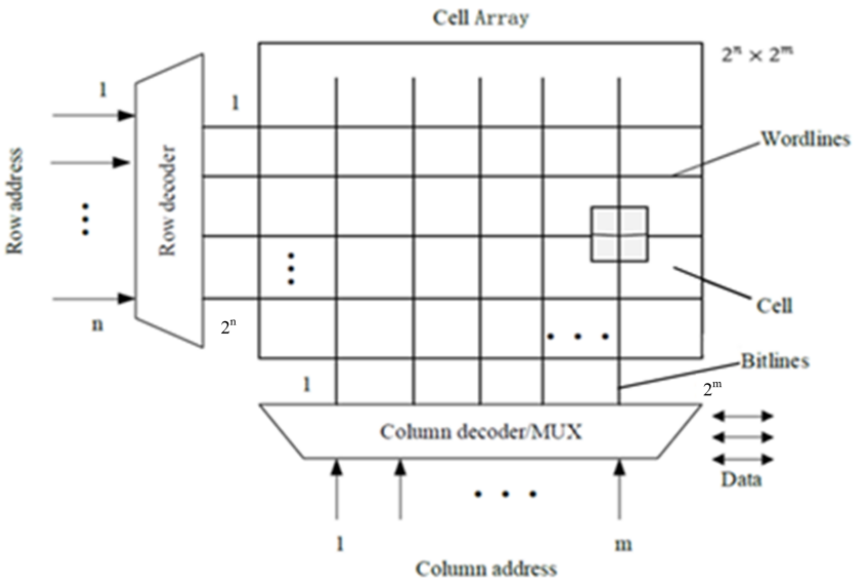

Figure 1.1 Block Diagram of Basic SRAM Memory Array

The block diagram of basic SRAM memory array is shown in Figure 1.1. SRAM array contains a matrix of memory cells of 2^m rows and 2^n columns. Each memory cell

consists of two cross coupled inverters. The inverters are connected to bit line (BL) and complement of bit line (BL_bar) through two NMOS access transistors which provides differential write and read access. Moreover, an SRAM array contains row and column circuit to access the memory cells. Out of 2^m word lines, one line is activated by the row decoder and the particular bit lines are connected by the memory cells to facilitate row.

A couple of column switches are sets by the column decoder and one bit line column out of 2^n bit line columns are connected to the peripheral circuits. The columns have pass transistors (not shown) which gets inputs from the column decoder, which in turn receives input from the column address lines and the output of the column decoder are passed to the gates of the pass transistors. This selects only one particular column. Thus, the combination of the row and the column decoder together selects one particular cell of SRAM at a time. The output of the columns that is the bit lines is connected to the I/O lines.

The two bit lines are pre-charged to a value close to VDD (positive supply voltage) during read operation. The NMOS access transistors connected to the cell node storing a '0' begin to discharge the bit line whereas the complementary bit line stays in its pre-charged state when word line is connected to high and a differential voltage is developed across two bit lines (BL and BL_bar). SRAM cells are optimized to reduce the cell area and their cell currents are small which results a slow bit line discharge speed. The small bit line signals are amplified by the sense amplifiers to accelerate the access of SRAM and finally push it to the outside world. The write data is shifted to the required columns in a write operation by moving the data onto the bit line and complement of the bit line. This is done by connecting either of the bit line pairs to ground. If the cell data and the write data are not same then the node "1" is discharged as the NMOS access transistor connects node to the discharged bit line. As a result the cell is loaded through the bit line value.

In this thesis, SRAM cell has been effectively considered and seem to be how to place the cells equally well. To reduce the usual time to access memory, SRAM (cache) is used in the central processing unit (CPU) of a computer. The cache is a less

significant and faster memory that stores the data copying from the most commonly used head memory locations. The techniques to reduce the average time and leakage current as well as area and power of the SRAM are mainly focused in this thesis work.

To reduce leakage power consumption a common technique known as the sleep transistor technique is used which cuts off transistors connection from VDD and/or Gnd. But, while transistors are allocated to hang, a system may have to stay a long period to constantly re-establish lost state and so, may show seriously degraded performance. Therefore, retaining state is crucial for a system that requires fast response even while in an inactive state.

Floating gate SRAM (FGSRAM) cell is designed using another leakage reduction technique called lector technique which decreases the leakage current substantially without increasing the dynamic power dissipation. This is a very efficient technique. In this technique, inside the logic gate two leakage control transistors are used. The gate terminal of each leakage control transistor (lector) is controlled through the source of the other transistor. In this technique, for every input arrangement one of the leakage control transistor is always close to its cut off voltage and the path resistance increases from VDD to ground (Gnd) which decreases the leakage currents. In addition, this technique also overcomes the restrictions created by previous existing methods for reduction of leakage.

In this thesis, a new SRAM cell combining floating gate MOSFET (FGMOSFET) with sleepy and lector technique has been proposed. The sleepy lector technique combines the advantages the sleepy transistor technique and the lector technique. This combined technique is focused on reduction of subthreshold leakage power consumption. The proposed cell can memorize multiple signals per memory cell and effective to use it as SRAM cell worth a multi-valued logic system. In low power-supply voltage, the purposed floating gate sleepy lector SRAM (FGSLLECSRAM) cell can protect a stable noise margin.

The peripheral circuits like write driver circuit, decoder (row and column), pre-charge circuit and sense amplifier are part of the architecture. So, all the peripheral circuits

are carefully designed with proper sizing of the transistors to minimize the power consumption. This thesis work proposes three types of architecture topologies. First applying 8 pre-charge circuits then applying 1 pre-charge circuit and finally by replacing pre-charge with control logic. All topologies are designed using 6T SRAM cell, FGSRAM cell and FGSLLEC SRAM cell. When compared it is found that the parameters like delay of FGSLLEC SRAM architecture is less than 6T SRAM and FGSRAM architecture in each case (8 pre-charge, 1 pre-charge and using control logic). The FGSLLEC SRAM architecture delay is reduced by 13% than the 6T SRAM and 31 % than the FGSRAM architecture. Also, power consumption of FGSLLEC SRAM architecture is less than 6T SRAM and FGSRAM architecture in each case (8 pre-charge, 1 pre-charge and using control logic). In FGSLLEC SRAM architecture using control logic power consumption is reduced by 98.9% than the 6T SRAM and 93.6% than the FGSRAM architecture in post layout simulation.

From the result analysis, it is found that the architecture using control logic circuit with FGSLLEC SRAM cell is more advantageous than other two architectures. The thesis work proposes novel low power techniques that realize leakage power consumption though keeping logic state. Also, it can be used for a system with extended stationary times.

1.2 Motivation

Growing demand for handheld devices such as cellular phones has motivated the semiconductor industry into a novel low energy and low power frontier. To increase the battery life period for as extensive as possible, a restricted quantity of energy stored in undersized battery needs wide power management techniques. Again, capacity of the battery has been developed at the modest rate (two to three times over the last 30 years). Embedded SRAM occupies more than 65% of the video decoder's core area of a chip [14] and adds to in excess of 30% of mobile device power consumption [15-18].

In everyday life since additional microelectronics are being used, the requirement on power has been increased sharply. As of the environmental point of view, the lesser the dissipation of energy of electronic devices, the lower the electricity consumed into

the rooms and so the worse the impact on worldwide environment, a reduced amount of the office noise due to removal of a fan from the desktop, and a reduced amount of stringent the office power /environment release or heat elimination requirements. As in standard CMOS SoCs one of the major challenges is leakage current [19], hence the lesser the consumption of power, the smaller the heat produced and thus the lower the price required for more cooling systems in home and offices. This energy efficient design makes possible reasonable ratio of cost-to-performance of the electronic equipment. For permanent supply devices the growing power dissipation is more or less equally challenging. As the technology is scaling down, transistors number is increased and extra power is dissipated. According to Moore's law, the transistors number is multiplied by four times every two to three years duration. Before 2020 on a single chip one hundred billion transistors are proposed. For wasting such large power produced from that huge number of transistors costly packaging techniques are required. Moreover, increased power dissipation has a harmful impact on consistency of the device. Every 10°C raise in working temperature doubles the failure rate of component. Several silicon failure mechanisms can be caused due to the rising temperature [20-21]. Since, chip power increases, gradually more expensive packaging and cooling policies are essential [22-23].

SRAM is faster as compared to dynamic random access memory (DRAM) but consumes more power. These issues are main aspects of motivation of this thesis work. Though the designs are already made on low power memory devices, the motive is to design 6T SRAM circuit which will consume less power and will have SNM using a low power consuming devices. Various techniques like temperature variation, stacking, multi threshold voltage are used to reduce the leakage power VLSI circuits.

As technology shrinks SRAM cell designers meet many challenges. It has become gradually more complicated to keep a tolerable SNM in a SRAM cell while scaling supply voltage and the minimum size. As a consequence, to organize the process parameters becomes extremely difficult, for the reason that the improved process variations are interpreted into a wider sharing of transistor and circuit characteristics.

Secondly, it is watched that in the SRAM bit-cell a lot of inconsistency problems by the side of a transistor level are there. For example, Data Retention or Read/Write/Access fails as the operating voltage is decreased. With this other failures relating to inconsistency in the sense amplifier circuit of SRAM cell are there. The raise in the power consumption marks in smaller battery life span for portable devices such as cell phones, laptops and personal digital assistants (PDAs) which are battery-operated [24]. Therefore, while meeting the performance requires the major objective for designing low-power of battery-operated portable electronic device is to expand the battery life. It is identified that just a 30% progress in battery performance is accomplished within five years. For that reason, the ability of upcoming portable devices will be severely restricted by the size and weight of the batteries essential for a suitable service period, if power optimization methods are useful at unlike stages of granularity [4]. Alternatively, in high presentation desktop systems the power consistency and packaging cost problems related with high power expenditure also has prepared the small power design a chief design goal. Due to the fall in swing voltage [25], permanence of the SRAM has also degraded.

1.3 Problem Statement

The problem to be solved in this research work is:

Design of low power high speed SRAM cell using floating gate MOSFET and different leakage minimization technique design of complete SRAM architecture with modified peripheral circuits to achieve better performance with variation of voltage and temperature without introducing much performance cost.

1.4 Organization of the Rest of the Thesis

The thesis discusses about the design of the SRAM cell and floating gate concept with leakage reduction techniques namely sleepy, lector and combined hybrid technique sleepy-lector. All the peripheral circuits and complete 8×8 FGSLLEC SRAM architecture with pre-charge circuit and proposed control logic circuit achieve overall low power consumption and low leakage power as well as improve the speed. The rest of the thesis work is organized as follows.

Chapter 2: Background and Literature Survey

This chapter briefly explains the basic operation of a SRAM cell which includes read operation, write operation and hold operation. Brief description of different leakage current components in CMOS process is presented here. It reviews current state-of-the-art techniques to reduce leakage current. It also presents, the SNM and comparison of simulation result of SRAM cell and FGSRAM cell. Research work reported in the literature on leakage power minimization of SRAM cell and other peripheral circuitry are summarized to provide an idea about latest development in this field.

Chapter 3: Floating Gate SRAM Cell using Sleepy Technique

This chapter presents the sleepy technique and design metrics for modified FGSRAM with sleepy transistors for leakage power minimization. The sleepy-stack technique is applied to generic logic circuits as a remedy for static power consumption. In this technique two sleepy transistors are used. One PMOS transistor is connected between pull-up network and VDD, the other one is connected between pull-down network and Gnd. Sleepy transistors use high threshold voltage (hVth) transistors. To prevent leakage power dissipation the transistors having lower threshold voltage (lVth) from supply and ground during standby (sleep) mode are isolated by the transistors having high threshold voltage . This technique provides less leakage by using high threshold voltage sleep transistors and high speed using low threshold voltage transistors in SRAM logic. Simulation results are presented and compared to the initial results with modified result.

Chapter 4: Floating Gate SRAM Cell using Lector Technique

This chapter explains how the LECTOR (LEakage Control TransistOR) technique is applied with FGSRAM cell. This approach introduces 4-transistors (two PMOS and two NMOS) in the FGSRAM cell. In this technique, between the pull-down and pull-up network of each inverter of FGSRAM cell two transistors are introduced. These two transistors are called leakage control transistors which are connected to the internal load lines of the cell, so that the gate terminal of each transistor is controlled

by the source terminal of the other transistor. Connecting in this way the effect is for any input arrangement; one of the leakage control transistors is always "near its cut-off voltage". This increases the resistance of the path from VDD to ground leading to significant decrease in leakage currents. Here, simulation results like power consumption, leakage power, read-write delay and SNM is calculated and compared with previous FGSRAM cell.

Chapter 5: Floating Gate SRAM Cell using Sleepy and Lector Technique

This chapter presents the modified SRAM cell i.e., FGSRAM by using both sleepy and lector techniques, which reduces more power consumption than individual technique. After analysing the results of sleepy and lector both the techniques are combined to capture the merits of individuals. Simulated results of 6T SRAM, FGSRAM, sleepy FGSRAM(FGSLSRM), lector FGSRAM (FGLECSRAM) and FGSLLEC SRAM cell are presented here. From simulation result of all designed cells it is observed that FGSLLEC SRAM cell is more advantageous than others. The proposed 8×8 SRAM architecture has been designed using this hybrid FGSLLEC SRAM cell.

Chapter 6: Peripheral Circuits in SRAM Architecture

This chapter presents the total peripheral circuits used in the complete SRAM architecture such as write driver, control logic circuit, address (row and column) decoders, pre-charge circuit and sense amplifier. Simulated outputs of all peripheral circuits are presented here.

Chapter 7: FGSLLEC SRAM Architecture

This chapter describes three architecture approaches i.e using 8 pre-charge, single pre-charge and finally using control logic circuit with 6T SRAM, FGSRAM and FGSLLEC SRAM. Analysis of simulation results and comparison of various SRAM architecture topologies are presented. From the simulated result it is found that the FGSLLEC SRAM architecture using control logic has better performance than other architectures. The layout diagram of all the architectures and the test report of design

rule check (DRC), layout vs schematic (LVS) and RC extraction(QRC) are presented here. Also process variation and corner have been analyzed for the proposed FGLSLEC SRAM architecture.

Chapter 8: Conclusion and Future prospects

This chapter presents the conclusions gained from research work as well as presents future research directions.