Chapter 7

Conclusion

7.1 Conclusions

While working on my thesis, many new ideas are explored. Furthermore, I gained a lot of experience in using the Xilinx ISE simulation and synthesis tools. The design of the 16-bit RISC processor, carried out at Electronics and Telecommunication Engineering Department, is very rewarding indeed. The results are almost satisfactory. The main objective of this thesis work is to design a 16-bit RISC processor and implement it into XC3S1000-5FT256 Spartan FPGA device, which is fulfilled to the almost satisfaction.

The proposed 16 bit RISC processor [104] is coded with VHDL. Using Xilinx ISE 10.1 software the code is tested and checked for error. When there is no error, the code is synthesized and simulated using Xilinx ISE 10.1 software. The synthesis and simulation results are same as the expected results, which is very attractive. The proposed processor has the capability for handling large applications due to flexibility provided in the memory. The proposed idea may be useful for rapid implementation and testing. This also facilitates to build the complete system on inexpensive FPGA.

Before the start of simulation, the memory is loaded by writing the instructions and data into the memory. The proposed processor with memory is tested for addition, subtraction, multiplication, and division program. First the VHDL code is 100% synthesized. Then the code is downloaded to the Spartan FPGA device. After downloading the code, the functionality of 16 bit RISC processor is found correct. The simulated output results have been compared with the expected results. The minimum clock period of proposed 16 bit RISC processor implemented in Spartan XC3S1000-5FT256 FPGA is 13.568 ns, which translate to a maximum operating frequency of 73.702MHz.

The Booth multiplier unit is tested and the functionality is found correct. Similarly, the functionality of restoring division circuit is tested and found correct.
The 4x4 Vedic multiplier sub module of the proposed 8x8 Vedic multiplier architecture [103] proved to show improved efficiency in terms of speed and area compared to the multiplier architecture proposed in [71]. The 8x8 Vedic multiplier is found to be better than 8x8 fast Booth multiplier in terms of both speed and area. The carry save adder based design investigated in this thesis seems to be more useful for the implementation of processor.

Further, the carry save adder based Vedic multiplier resulted in high performance of the proposed multiply accumulate unit [102]. The multiply accumulate module architecture proved to show improved efficiency in terms of speed compared to the corresponding optimized Vedic multiplier architecture presented in [72]. Our approach for the design of MAC unit is better than the earlier method proposed in [72].

The Vedic multiplier architecture using ‘Nikhilam’ Sutra investigated in this thesis [103] has speed improvements compared to Vedic multiplier architecture presented in [56], [69] and [100]. The 16x16 Vedic multiplier using ‘Nikhilam’ Sutra found to be better than 16x16 Vedic multiplier using ‘Urdhva Tiryagbhyam’ Sutra in terms of both speed and area. Hence, the Vedic multiplier introduced in this thesis may be useful for high performance processors.

7.2 Future work

For further work on the thesis, I recommend my successors to continue the following tasks:

- The 4 bit function field of instruction set architecture is not used. The function field can add sixteen numbers of additional operations in the design of the processor.
- The 32x32 and 64x64 bit Vedic multiplier using ‘Urdhva Tiryagbhyam’ Sutra can be implemented to test for time delay.
- The Vedic multiplier architecture using ‘Nikhilam’ Sutra can be implemented for data size 32x32 and 64x64 bits for reduction of time delay.
- The functionality of the proposed 16-bit RISC processor can be tested by any other sample program.
- A new method for data transfer from I/O into memory can be investigated.