A Low-Noise Four-Stage Voltage-Controlled Ring Oscillator in Deep-Submicrometer CMOS Technology

Joo-Myoung Kim, Student Member, IEEE, Seungjin Kim, In-Young Lee, Student Member, IEEE, Seok-Kyun Han, and Sang-Gug Lee, Member, IEEE

Abstract—This brief presents a low-voltage and low-noise ring voltage-controlled oscillator (VCO) where the phase noise performance is improved by reducing the total channel thermal noise injected into the output node of the VCO during the transition period of the output voltage swing. Implemented in a 65-nm CMOS technology, the proposed ring VCO operates from 485.7 to 1011.6 MHz. At 645 MHz, the measured phase noise is $-110.8$ dBc/Hz at an offset of 1 MHz while dissipating 10 mW from a 1-V supply.

Index Terms—Phase noise, ring oscillator, transition period, voltage-controlled oscillator (VCO).

I. INTRODUCTION

C MOS TECHNOLOGIES continue to be scaled down in order to lower costs, increase speeds, and achieve a higher level of integration. As a result, CMOS has flourished in wireless communication applications [1]. However, transceiver building blocks must now accommodate the shrinking supply voltage of deep-submicrometer technologies.

LC voltage-controlled oscillators (VCOs) (LC VCOs) are typically utilized in wireless transceivers due to their good phase noise performance [2]. However, LC VCOs exhibit a relatively narrow tuning range, which further decreases with the supply voltage. Furthermore, these designs also occupy a large chip area, regardless of scaling. In contrast, ring VCOs offer a wide tuning range and occupy a small chip area, and their power consumption substantially decreases with scaling. Owing to these attributes, ring VCOs are a popular candidate for implementation in scaled CMOS. Unfortunately, they exhibit poor phase noise performance. Thus, the phase noise of ring VCOs is the key issue compared to LC VCOs.

Extensive research has been carried out to analyze and improve the phase noise of ring oscillators [3]–[7]. From these works, it has been reported that the phase noise is degraded by the reduced output voltage swing and the increased channel thermal noise of the transistor in accordance with the development of CMOS technology [4]. The phase noise of the ring oscillator can be improved by maximizing the output voltage swing and minimizing the amount of noise injected during output voltage transitions [4]. The VCOs reported in [6] and [7] facilitate rail-to-rail voltage swings to achieve low phase noise. However, the noise performance of the design in [6] is limited by the delay cells, which inject a substantial amount of noise during the transition periods of the VCO. A ring VCO with good phase noise was reported in [7]. However, it suffers from an extremely narrow tuning range due to the reduced supply voltages of scaled-down CMOS technology [8]. In [8], this problem is mitigated by adopting a transmission gate. Despite an increased tuning range, the noise current injected by the transmission gate during the transition periods translates to a significant amount of phase noise. This brief focuses on reducing the amount of injected channel thermal noise of transistors during output voltage transitions while maintaining an acceptable frequency tuning range for low supply voltages.

This brief is organized as follows. Section II describes the phase noise of the ring oscillator. Section III presents the structure and the operation principles of the proposed VCO shown in Fig. 1. Section IV gives the measurement results. Section V discusses the performance of the proposed VCO in comparison with other ring VCOs in accordance with technology development. Finally, conclusions are provided in Section VI.

II. PHASE NOISE OF RING OSCILLATOR

Hajimiri et al. [3], [4] reported that the phase noise of the ring oscillator is affected by the amount of noise injected during the transition period of the oscillator output signal, and the single-sideband phase noise spectrum due to a white-noise current source is given by

$$L(f_{\text{off}}) = \frac{\Gamma^2_{\text{rms}}}{8\pi^2 f_{\text{off}}^2} \cdot \frac{i_n^2}{\Delta f}$$  \hspace{1cm} (1)$$

where $\Gamma^2_{\text{rms}}$ is the rms value of the impulse sensitivity function (ISF); an approximate ISF for the ring oscillator is shown in Fig. 2 [4]. $i_n^2/\Delta f$ is the single-sideband power spectral density of the noise current source and $f_{\text{off}}$ is the frequency offset from the carrier. In the case of multiple noise sources injected into the same node of the delay cell, $i_n^2/\Delta f$ represents the total current noise due to all sources and is given by the sum of individual

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PMOS input transistors \((M_5, M_6)\), and the PMOS control transistors \((M_{cont1}, M_{cont2})\) that are adopted to change the oscillation frequency by varying the control voltage \(V_{cont}\).

Fig. 1(b) shows the proposed four-stage ring VCO, which provides eight different phases \((0^\circ, 45^\circ, 90^\circ, 135^\circ, 180^\circ, 225^\circ, 270^\circ,\) and \(315^\circ\)). \(V_{IN1+}\) and \(V_{IN1-}\) represent the differential voltage that is applied to the NMOS input transistors \(M_1\) and \(M_2\), and \(V_{OUT-}\) and \(V_{OUT+}\) constitute the differential output voltage of the delay cell. Due to the oscillation condition of the four-stage structure, the phase difference between the input \((V_{IN1+}, V_{IN1-})\) and output \((V_{OUT-}, V_{OUT+})\) is \(225^\circ\). \(V_{IN2-}\) and \(V_{IN2+}\) are applied to the PMOS input transistors \(M_5\) and \(M_6\), respectively. As \(V_{IN2-}\) and \(V_{IN2+}\) are taken from a delay cell that is two stages away from the corresponding delay cell, \(V_{IN2-}\) and \(V_{IN2+}\) come \(45^\circ\) earlier in phase than \(V_{IN1+}\) and \(V_{IN1-}\) [7]. The proposed VCO adopts the negative skewed delay scheme reported in [7] for fast transition as a method to improve the phase noise.

To illustrate how the phase noise is reduced in the proposed design, the time-domain operation of the proposed ring oscillator is now analyzed. Since each stage is identical, it is sufficient to examine a single delay cell over one oscillation period. The analysis is further simplified by only considering the half circuit of the proposed delay cell. This is easily justified since the goal of the analysis is to show the reduced conduction time during the transition periods of the oscillator, and both halves of the circuit ideally behave in the same manner.

Fig. 3 depicts the half-circuit waveforms of a single delay cell in the proposed design. Fig. 3(a) shows the input voltage \(V_{IN1+}\), while \(V_{OUT-}\), \(V_{IN2-}\), and \(V_{OUT+}\) are given in Fig. 3(b). Fig. 3(c) shows the current \(i_{pc1}\) flowing through \(M_{cont1}\) in the proposed delay cell. Fig. 3(d) illustrates the behavior of the proposed delay cell through one oscillation period. Consequently, the delay circuit exhibits three regions of operation, which are now considered in detail.

In region I, \(V_{IN1+}\) and \(V_{OUT+}\) are low while \(V_{OUT-}\) remains high. This region of operation continues until a low–high transition of \(V_{IN2-}\) occurs, thereby changing \(V_{IN2-}\) to approximately \(V_{DD-}[V_{th,p}]\). As illustrated in Fig. 3(d), \(M_5\) is in the OFF state while all the PMOS transistors \((M_3, M_5, M_{cont1})\) are on. In this region, the device noise power spectral density is given by

\[
\frac{\tilde{v}_n^2}{\Delta f} = 4kT\gamma(g_{mp3} + g_{mpcont1})
\]  

where \(g_{mp3}\) and \(g_{mpcont1}\) are the transconductances of transistors \(M_3\) and \(M_{cont1}\), respectively. \(\gamma\) is the noise multiplication factor, which is more significant for a short-channel transistor. In this region, the phase noise is negligible since the output voltage remains near the supply rail [4].

In region II, \(V_{IN1+}\) and \(V_{OUT+}\) experience a low–high transition while \(V_{OUT-}\) undergoes a high–low transition. During the transition of \(V_{OUT-}\), the phase noise is affected by the noise current of only two transistors, \(M_1\) and \(M_3\). In the proposed delay cell, \(i_{pc1}\) flowing through \(M_5\) and \(M_{cont1}\) can be eliminated by turning off \(M_5\) since \(V_{IN2-}\) is higher than \(V_{DD-}[V_{th,p}]\) in this region. During the high–low transition of
the output voltage $V_{OUT-}$, the device noise power spectral density is given by

$$\bar{i}^2 = 4KT\gamma(g_{mp3} + g_{m1})$$  \hspace{1cm} (3)$$

where $g_{m1}$ is the transconductance of transistor $M_1$. In (3), there is no noise current from $M_{cont1}$ since the transistor is off during the high–low transition of $V_{OUT-}$. As a result, the phase noise does not suffer from noise current by $M_{cont1}$ at the output in this region.

In region III, $V_{IN1+}$ and $V_{OUT+}$ change from high to low while $V_{OUT-}$ undergoes a low–high transition. In this region, $V_{IN2-}$ is at a lower voltage than $V_{DD} + |V_{th,n}|$, and thus, both $M_5$ and $M_{cont1}$ turn on; hence, $i_{pc1}$ and the accompanying channel noise are observed. However, $i_{pc1}$ is terminated as soon as $V_{OUT-}$ reaches $V_{DD}$. During the low–high transition of $V_{OUT-}$, the device noise power spectral density is given by

$$\bar{i}^2 = 4KT\gamma(g_{mp3} + g_{mpcont1} + g_{m1})$$  \hspace{1cm} (4)$$

Thus, the phase noise is dominantly affected during the low–high transition of $V_{OUT-}$, which occurs in region III, because all noise sources appear in this region. The same operation can be applied to the other half circuit.

In summary, the proposed ring oscillator can alleviate much of the phase noise contributed by the channel thermal noise of $M_{cont1}$ by turning off $M_5$ and $M_{cont1}$ in region II. Fig. 3(c) shows $i_{pc1}$, which corresponds to the current through the frequency control transistors of the design reported in [6], plotted against $i_{pc1}$ of the proposed oscillator. As can be seen in Fig. 3(c), $i_{pc2}$ of [6] appeared over the entire two transitions (low–high and high–low), but the frequency control current of the proposed delay cell ($i_{pc1}$) only appeared during one transition period (low–high). As a result, the phase noise performance is improved in the proposed architecture. Fig. 4 represents the simulation results of the proposed structure to verify the discussed waveforms ($V_{IN1+}$, $V_{OUT-}$, $V_{IN2-}$, and $i_{pc1}$) in Fig. 3. The simulation results shown in Fig. 4 are similar to that in Fig. 3, and $i_{pc1}$ is eliminated during the high–low transition of the output voltage. Thus, the phase noise of the proposed VCO is improved by eliminating the noise current of $M_{cont1,2}$ during the high–low transition as well as by achieving the fast transition by a negative skewed delay scheme [7] and PMOS latch.

Fig. 5 shows the simulated phase noise performance in comparison with other ring VCO architectures reported in [6], [7], and [10] for the same process, supply voltage, center frequency (645 MHz), and power dissipation (11 mW). The proposed VCO achieves the lowest phase noise performance among the simulated VCOs; the phase noise of the proposed VCO is 6.6,
The oscillation frequency is tuned by \( i_{pe1} \), which is changed according to the control voltage \( (V_{cont}) \), because the charging time of the output capacitor is affected by \( i_{pe1} \). If the gate voltage \( V_{cont} \) of \( M_{cont1} \) is increased, the current \( i_{pe1} \) is decreased, and the output capacitor is charged slowly. Thus, the charging time is increased, and the oscillation frequency is decreased. Therefore, the oscillation frequency can be changed by \( V_{cont} \). Furthermore, the proposed VCO achieves a wider frequency tuning range than [6] because higher oscillation frequency is achieved by adopting the dual-delay scheme of [7]. The proposed ring oscillator is limited by the characteristic that the delay cell can be used as a four-stage oscillator in order to maximize the effect of the phase noise improvement. This may not, however, be a critical issue, as a four-stage ring oscillator has been widely used.

**IV. MEASUREMENT RESULTS**

The proposed ring VCO is fabricated in a 65-nm CMOS technology. The oscillation frequency range is measured from 485.7 to 1011.6 MHz over a control voltage from 0.8 to 0 V, as shown in Fig. 6. Fig. 7 shows the measured phase noise and the output spectrum. The measured phase noise is \(-110.8 \text{ dBc/Hz}\) at a 1-MHz offset while oscillating at 645 MHz and dissipating 10 mA at a 1-V supply. An approximately 0-dBm output power is measured at the buffer output. The open-drain common-source topology using the off-chip inductor is adopted as the output buffer of the proposed ring VCO. Fig. 8 shows a microphotograph of the fabricated VCO. The chip area without the pads is \( 230 \times 98 \mu \text{m}^2 \).

Table I summarizes the measurement results of the proposed VCO and prior works. In order to provide a fair comparison with other reported works at different center frequencies and power consumptions, a Figure-of-Merit (FoM), as defined hereinafter, is used:

\[
\text{FoM} = L\{f_{off}\} - 20 \log \left( \frac{f_{osc}}{f_{off}} \right) + 10 \log \left( \frac{P_{diss}}{1 \text{ mW}} \right)
\]

where \( L\{f_{off}\} \) is the phase noise from the oscillation frequency \( (f_{osc}) \) at the offset of \( f_{off} \) and \( P_{diss} \) is the power consumption of the VCO.

**V. DISCUSSION**

As shown in Table I, [6]–[9] and [11] were implemented in 500-, 600-, 180-, 180-, and 180-nm CMOS technologies, respectively. The delay cells of [7] was used in [9] and [11] as well. Eken and Uyemura [11] report a high oscillation frequency of 5.9 GHz with good phase noise performance. However, the FoM cannot be estimated to compare with other
ring VCOs in Table I because the power dissipation was not reported. In Table I, it can be seen that the FoMs of [6] and [7] are better than those of [8] and [9] because the phase noise of the short-channel oscillator is larger than that of the long-channel case at the same center frequency and power consumption due to the larger $\gamma$ of the short-channel transistor as reported in [4]. Although the channel lengths of [8] and [9] are the same, the FoM of [9] is better than that of [8] because the delay cell of [9] was used with the low-noise delay cell of [7]. As discussed in Section I, however, the delay cell of [7] suffers from a narrow tuning range at a low supply voltage. In the case of [9], the frequency tuning range is only 8.13% under a tuning voltage of 1.6 V. If the supply voltage continues to be reduced with the development of CMOS technology, the frequency tuning range would be narrower, and the delay cell of [7] will be difficult to be used in wideband applications. Thus, new low-noise delay cells are required for an acceptable frequency tuning range at a low supply voltage. In spite of the low supply voltage and the short-channel technology whose phase noise performance is inferior, the proposed VCO shows a frequency tuning range of about 70% with a FoM of $-157$ dBc/Hz, which is similar to that of [6] and is 6.4 and 0.7 dB better than those of [8] and [9], respectively. Therefore, the proposed VCO can be used as a low-noise ring VCO for low supply voltage and scaled-down technology.

### VI. Conclusion

A low-noise ring VCO is proposed as a suitable structure in deep-submicrometer CMOS technology. The phase noise is improved by eliminating the noise currents that are added for frequency tuning during the output high–low transition. The VCO is implemented in a 65-nm CMOS technology. The measured frequency tuning range is from 485.7 to 1011.6 MHz (about 70%). At 645 MHz, the measured phase noise is $-110.8$ dBc/Hz at a 1-MHz offset frequency while dissipating 10 mA at a 1-V supply. The FoM of the proposed VCO is $-157$ dBc/Hz. The proposed VCO can be used as a low-noise ring VCO for low supply voltage and scaled-down technology.

### References

A Multiobjective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO
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Abstract—This paper presents a novel design methodology for design of optimal and robust current starved voltage controlled oscillator (CSVCO) circuit. A recently developed multiobjective optimization technique infeasibility driven evolutionary algorithm is used to minimize the power and the phase noise of the circuit at its schematic and physical level. The multiobjective optimization is carried out by taking into account the extracted parasitics that would be present in the physical integrated circuit and the random variations of parameters during fabrication in foundry. This method helps the designer in semiconductor industry by effectively reducing several time consuming design iterations to a single iteration ensuring the near optimal performance of the CSVCO. The performance of the circuit is validated by carrying out simulations for transient and noise analysis in Cadence tools using 90 nm 1P9 M CMOS process.

Index Terms—Industrial Design Optimization, Multi-objective optimization, Infeasibility Driven Evolutionary Algorithm (IDEA), Current Starved Voltage Controlled Oscillator (CSVCO).

I. INTRODUCTION

The voltage controlled oscillator (VCO) is a very widely used block in wireless transceivers and many other electronic systems. The reception quality of the signals in any wireless standard [1], [2] depends on the noise performance of the VCO. The VCO [3] is built as a part of a high density integrated circuit system like transceiver and phase locked loops [4], [5]. The parasitic components are undesired but unavoidable in integrated circuits. They have a significant effect on the performance of radio frequency integrated circuits (RFIC) particularly in the submicron regime. This can be overcome by taking these into account during the initial design phase. When parasitic effects are considered, the complete circuit becomes too much complex to be analyzed by hand. Hence finding design parameters manually for optimal circuit performance by the designer in semiconductor industry is almost impossible. The complexity of the problem is further elevated when there is a necessity to optimize multiple competing performance indices. A designer in semiconductor industry accomplishes this task by many design iterations which is time consuming, yet with no guarantee on the optimal performance. Apart from this, the study of the effect of variations in process parameters on different performance indices is vital because of the high sensitivity of nanoscale RFIC to any parameter. Optimization methodologies find wide scope for performance improvement in integrated circuits design industry. Optimization of parameters in RF circuits [6] has been an active area of research in present times. Optimization of design parameters for efficient Analog integrated circuit design is another important area which has attracted attention of many researchers. In [7], Mandal and Visvanathan have presented a novel scheme of CMOS operational amplifier design using geometric programming. Another such work on opamp design has been carried out in [8]. However reliance on gradient based optimization methods make them prone to possible trapping at local optima. Employment of global optimization techniques such as genetic algorithm (GA) [6], [9], [10], swarm intelligence [11]–[14], bacterial foraging optimization [10] and many others mitigate this problem. Thus, the evolutionary optimization techniques have been widely applied for analog integrated circuits design [15], [16]. But, in normal parasitic aware analog circuit designs the parasitics are generated from an initial circuit which may not be yielding optimal performance and hence the parasitics considered for further circuit optimization may not be proper in their value. Again for good performance of integrated circuits multiple design goals need to be optimized. In such a scenario, all these techniques that have the limitation of optimizing single objective function fail. And, there is a need for optimizing multiple objective functions in a multimodal design landscape [17], [18]. In [19] conjugate gradient optimization and in [20], [21] polynomial regression based genetic algorithm is used for design of a voltage controlled oscillator which has very wide scope for performance improvement by use of multi-objective optimization. Multiobjective evolutionary optimization techniques like the Non-dominated Sorting Genetic Algorithm-II (NSGA-II) [22] have found wide applications in various practical problems where more than one competing objectives need to be optimized. The recently proposed infeasibility driven evolutionary algorithm (IDEA) is an efficient multi-objective optimization technique that avoids trapping at local optima and at the same time finds multiple optimal solutions.

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optimization technique which has been reported [23]–[25] to offer superior performance as compared to NSGA-II and can be considered as a competent candidate for multi-objective analog design methodology.

In this work a novel IDEA based multi-objective fast design methodology is proposed. This is applied to design of a current starved voltage controlled oscillator (CSVCO) as a case study. The proposed design methodology has following novel aspects.

1) Multi-objective (3-Objective) performance optimization of Current Starved Voltage Controlled Oscillator under real world constraints is carried out using IDEA.
2) The design methodology is simple as it relies on equation based approach yet achieves the targets with high precision.
3) The industrial design cycle of the circuit under consideration is faster with optimal performance.

The designer gets the flexibility to choose the parameters for minimum phase noise being aware of the required power specification. Though the methodology is applied to CSVCO circuit here, it can be extended for optimal design of any RFIC with multiple performance objectives with practical constraints.

The remaining part of the paper is organized as follows. The next section describes about the design objectives for CSVCO. Section III elaborates proposed IDEA based design methodology for the robust optimal CSVCO. In Section IV the performance analysis of the optimized circuit has been carried out. Finally the finding of the study has been concluded in Section V.

II. DESIGN OBJECTIVES FOR CSVCO

The current starved VCO is shown schematically in Fig. 1. The circuit has two distinct parts, the inverter stages and current starving circuitry. The design objective of this work is to minimize phase noise and power of the CSVCO with a desired frequency of oscillation, subject to the physical constraints. An N-stage current starved VCO circuit in general produces oscillations of frequency [26]–[29] given by

\[ f_{osc} = \frac{g_{m}}{\pi N (C_{in} + C_{gd} + C_{db} + C_{gso})} \]

where

- \( C_{in} = \frac{2}{3} C_{ox} W L \)
- \( C_{gd} = \frac{1}{2} C_{ox} W L \)
- \( C_{db} = C_{j} A_{d} \left( 1 + \frac{V_{dd}}{p} \right) \)
- \( C_{gso} = \left( 1 + \cos \left( \frac{\pi}{2N} \right) \right) W C_{gso} \)
- \( C_{pbn} = 2 C_{j} A_{d} + 2 C_{j} W L \)
- \( C_{pbn} = W C_{gso} \)
- \( C_{gso} = 2 L C_{gso} \)

Where

- \( C_{ox} = \) Oxide capacitance per unit area
- \( W = \) Channel width of nMOS
- \( L = \) Channel length of nMOS
- \( p = \) p-n junction potential
- \( m_{j} = \) Area junction grading coefficient

Fig. 1. Circuit schematic of CSVCO.
The total power dissipated \([30]-[33]\) by N-stage CSVCO circuit is given by

\[
P = P_{\text{avg}} + P_{\text{sc}}
\]

Where

- \(P_{\text{avg}}\) = Average power dissipated by the CSVCO
- \(P_{\text{sc}}\) = Short circuit power dissipation

**Phase Noise**

The phase noise of the CSVCO circuit \([34]-[36]\) is expressed as

\[
L\{\Delta f\} = \frac{8kT}{3n}\frac{V_{\text{char}}^2}{f_{\text{osc}}^2} \Delta f^2
\]

where

- \(V_{\text{char}} = \frac{AV}{\gamma}\)
- \(P = \text{Total power dissipated by the CSVCO.}\)
- \(\Delta V\) is the gate over drive voltage
- \(k\) is Boltzmann Constant
- \(T\) is absolute temperature
- \(\gamma\) is a coefficient which is \(2/3\) for long channel devices in saturation and twice or thrice of this for short channel devices and \(n\) is a characteristic constant which is taken here as 1.

\(\Delta f\) is the offset frequency from the carrier at which the phase noise is measured.

III. THE PROPOSED IDEA BASED ROBUST DESIGN METHODOLOGY FOR OPTIMAL CSVCO

The proposed IDEA based design flow of optimal CSVCO is depicted in Fig. 2.

A. Design Optimization

The required specifications, the design space constraints and the reference circuit model are the inputs to the IDEA processing block. The primary goal of this processor is to determine the design parameters of all transistor elements in the CSVCO. The implicitly parasitic dependant analytic equations of power consumption (2) and phase noise (3) constitute the optimization objectives of the IDEA processor. This processor is allowed to explore the optimal solutions in a limited design space with a very marginally tolerable frequency drift around the target frequency of CSVCO.

With these initial optimized design parameters the CSVCO schematic and subsequent physical layout are designed in Cadence Virtuoso ADE. The physical layout so generated is subjected to RCLK parasitic extraction. The algorithm starts with the reference circuit model (with SPICE parameters), and in every iteration of design, the design parameters for optimal performance are obtained and the post layout RCLK (Resistance, Capacitance, Inductance, Mutual Inductance) parasitic extraction is performed. Then the circuit model parameters are adapted or modified with the inclusion of the extracted parasitic and process variation parameters. These modified circuit model parameters are used as the input to the IDEA processor block in place of the reference circuit model in the next iteration of the design. This provides the IDEA processor with a near exact parasitic aware model of the circuit which
Minimize performance parameters. The IDEA block provides the final level parasitic aware performance optimized design parameters for the CSVCO circuit. These design parameters are utilized to generate the optimized physical layout which can be taped out for fabrication.

So the final design parameters obtained from this methodology meet the desired specs along with global best optimal performance parameters. The IDEA based optimization processing can be stated as

\[
\text{Minimize } \mu^{(n)} \\
\text{Subject to } \begin{cases} 
    \frac{f_{osc}}{2} = 2\text{GHz} \\
    W_{\text{net}} < W < W_{\text{max}} \\
    L_{\text{min}} < L < L_{\text{max}} \end{cases} \leq 8 \quad (4)
\]

where \(g_{\text{mos}}\) and \(g_{\text{pox}}\) are the transconductance parameters of NMOS and PMOS respectively. \(\delta\) is a very small positive definite constant. Simulated binary crossover (SBX) and polynomial mutation operators are used in IDEA to generate offspring from a pair of parents selected using binary tournament. Individual solutions in the population are evaluated using the problem definition (4) and the infeasible solutions are identified. The solutions in the parent and offspring population are divided into a feasible set \(S_f\) and an infeasible set \(S_{inf}\). The solutions in the feasible set and the infeasible set are ranked separately using the non-dominated sorting and crowding distance sorting based on the objectives.

**IDEA Processing for Current Starved VCO Problem:**

To make the circuit robust enough to work under random variations due to fluctuations in manufacturing processes and operating conditions, the extremities of the fabrication variations due to fluctuations in manufacturing processes and operating conditions, the extremities of the fabrication are incorporated in circuit model adaptation. The variations in internal noise parameters like \(V_{\text{thn}}, V_{\text{thp}}, \tau_{\text{oxn}}\) & \(\tau_{\text{oxp}}\) and external parameters like \(V_{\text{DD}}\) are taken to be \(+10\%\) and \(-10\\%\) respectively for worst-case analysis. This is injected into the IDEA processor for the robustification of the circuit during design stage.

**IV. PERFORMANCE ANALYSIS OF THE CSVCO**

The initial IDEA optimized circuit schematic is simulated in Cadence Virtuoso Analog Design environment. In the current design the IDEA processor targets the CSVCO circuit to produce oscillations of frequency 2 GHz. The schematic level estimated frequency of oscillations is 2.00097 GHz with the phase noise value of \(-88.33\) dBc/Hz at 1 MHz offset and the power consumption of 452.71 \(\mu\)W. The design parameters are listed in Table I-A comparison of the performance parameters of schematic level CSVCO designed using the parameters obtained from IDEA, NSGA-II and MPSO (Multi-objective Particle Swarm Optimization) is depicted in Table II. The initial level simulation results of performance parameters are provided in Table III. The observed oscillation frequency as per (4). The solutions for the next generation are selected from both the sets to maintain infeasible solutions in the population. The infeasible solutions are ranked higher than the feasible solutions to provide a selection pressure to create better infeasible solutions resulting in an active search through the infeasible search space. The marginally infeasible solutions in IDEA very often prove beneficial trade-offs for the integrated circuit design. Hence the technique is more attractive than NSGA-II for application in IC design optimization problem.

It is worth noting here that the final design is accomplished with only two runs of the IDEA processor and the designer has to draw the physical layout only once before the final physical layout taped out for fabrication. Hence the design process is very fast with almost no trials by the designer.

**B. Design Robustification**

To make the circuit robust enough to work under random variations due to fluctuations in manufacturing processes and operating conditions, the extremities of the fabrication are incorporated in circuit model adaptation. The variations in internal noise parameters like \(V_{\text{thn}}, V_{\text{thp}}, \tau_{\text{oxn}}\) & \(\tau_{\text{oxp}}\) and external parameters like \(V_{\text{DD}}\) are taken to be \(+10\%\) and \(-10\%\) respectively for worst-case analysis. This is injected into the IDEA processor for the robustification of the circuit during design stage.

**TABLE I**

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Lower Limit</th>
<th>Upper Limit</th>
<th>Initial Optimal Value (Obtained from IDEA)</th>
<th>Parasitic and Process Variation Aware Optimal Value (Obtained from IDEA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W_{\text{net}})</td>
<td>200 nm</td>
<td>500 nm</td>
<td>340 nm</td>
<td>355 nm</td>
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<td>(W_{\text{p}})</td>
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<td>1 (\mu)m</td>
<td>670 nm</td>
<td>740 nm</td>
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<td>1 (\mu)m</td>
<td>3.5 (\mu)m</td>
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<tr>
<td>(W_{\text{per}})</td>
<td>5 (\mu)m</td>
<td>20 (\mu)m</td>
<td>15.06 (\mu)m</td>
<td>5 (\mu)m</td>
</tr>
<tr>
<td>(c)</td>
<td>100 nm</td>
<td>110 nm</td>
<td>110 nm</td>
<td>100 nm</td>
</tr>
</tbody>
</table>

**TABLE II**

<table>
<thead>
<tr>
<th>Set: N</th>
<th>Population Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set: NG</td>
<td>Number of Generations</td>
</tr>
<tr>
<td>Set: ca</td>
<td>Proportion of infeasible solutions</td>
</tr>
<tr>
<td>1: (N_{\text{init}} = N)</td>
<td></td>
</tr>
<tr>
<td>2: (N = N_{\text{ref}})</td>
<td></td>
</tr>
<tr>
<td>3: while Parameter Constraints (C = [W_{\text{min}} &lt; W &lt; W_{\text{max}} , \ L_{\text{min}} &lt; L &lt; L_{\text{max}}] ) do</td>
<td></td>
</tr>
<tr>
<td>4: pop1 = Initialize () subject to (C)</td>
<td></td>
</tr>
<tr>
<td>5: Evaluate ([L(\Delta f),p_{\text{avg}}]_{\text{pop1}})</td>
<td></td>
</tr>
<tr>
<td>6: for (i = 2) to (NG) do</td>
<td></td>
</tr>
<tr>
<td>7: childpop(<em>i) = Evolve (pop(</em>{i-1}))</td>
<td></td>
</tr>
<tr>
<td>8: Evaluate ([L(\Delta f),p_{\text{avg}}]<em>{\text{childpop}</em>{i-1}})</td>
<td></td>
</tr>
<tr>
<td>9: Compute (D = [f_{\text{osc}} - f_{\text{avg}}])</td>
<td></td>
</tr>
<tr>
<td>10: if (D &lt; 0) then (S_f)</td>
<td></td>
</tr>
<tr>
<td>else (S_{inf})</td>
<td></td>
</tr>
<tr>
<td>11: ((S_f,S_{inf})=\text{Split} (pop_{i-1} + \text{childpop}_{i-1}))</td>
<td></td>
</tr>
<tr>
<td>12: Rank ((S_f))</td>
<td></td>
</tr>
<tr>
<td>13: Rank ((S_{inf}))</td>
<td></td>
</tr>
<tr>
<td>14: (p_{\text{avg}} = S_{inf}(1 : N_{\text{inf}}) + S_f(1 : N_f))</td>
<td></td>
</tr>
<tr>
<td>15: end for</td>
<td></td>
</tr>
<tr>
<td>16: end while</td>
<td></td>
</tr>
</tbody>
</table>
closely matches with the IDEA predicted values. This is due to the implicit inclusion of parasitic in the circuit model input to IDEA. The post layout oscillation frequency reduces to 1.60824 GHz because the exact parasitic are not available at this stage. Again in the worst case scenario the frequency further degrades to 1.40579 GHz. The performance parameters for final optimized robust design are listed in Table IV. It is clearly noticeable that the worst case post layout oscillation frequency is 2.00642 GHz which is very close to the IDEA prediction. The phase noise at 1 MHz offset is $-87.71$ dBc/Hz and power consumption is 765.641 μW which are in well acceptable agreement with the predictions.

![Fig. 3. The oscillations produced by CSVCO.](image)

![Fig. 4. CSVCO phase noise plot.](image)
Table V summarizes the performance of the robust optimal CSVCO parameters and compares those with other novel approaches on the same circuit reported in [19]–[21]. This design approach is entirely different from [19] and hence the performance achievement is considerable in the following aspects. Firstly the difference between the frequency reported in this work and target frequency is 6.42 MHz which is very less in comparison to the difference of 90 MHz between the target frequency and the frequency reported in [19]. Secondly the methodology presented here optimizes two other important

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reported in this work</th>
<th>Reported in [19]</th>
<th>Reported in [20 &amp; 21]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS Salicide 1.2V / 2.5V 1P5M</td>
<td>CMOS Salicide 1.2V / 2.5V 1P5M</td>
<td>CMOS Salicide 1V / 2V 1P9M</td>
</tr>
<tr>
<td>Optimization Algorithm</td>
<td>IDEA</td>
<td>Conjugate gradient</td>
<td>Polynomial regression based GA</td>
</tr>
<tr>
<td>Desired Frequency of Oscillation</td>
<td>2 GHz</td>
<td>2 GHz</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Optimized Schematic Level Power</td>
<td>412.710 µW (Deviation = 4.93 %)</td>
<td>—</td>
<td>50 µW (Deviation = 2.38 %)</td>
</tr>
<tr>
<td>Optimized Schematic Level Noise</td>
<td>-88.53 dBc/Hz (β) 1 MHz of Test</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PVT Variation Effects</td>
<td>Included</td>
<td>Included</td>
<td>Not Included</td>
</tr>
<tr>
<td>Nominal Oscillation Frequency</td>
<td>2.30560 GHz</td>
<td>2.54 GHz</td>
<td>—</td>
</tr>
<tr>
<td>Worst-Case Oscillation Frequency</td>
<td>2.00642 GHz</td>
<td>1.91 GHz</td>
<td>—</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-87.37 dBc/Hz (β) 1 MHz of Test</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Average Power Consumption</td>
<td>765.643 µW</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Physical Layout Area</td>
<td>0.9595 µm²</td>
<td>2.408 µm²</td>
<td>Layout Not Drawn</td>
</tr>
</tbody>
</table>

Fig. 5. Oscillation frequency variation with control voltage.

Fig. 6. The power estimation in cadence.

Fig. 7. The optimized parasitic and process variation aware physical layout of 13 stage CSVCO.
IC design objectives: phase noise and power consumption. Thirdly, this work reports CSVCO to occupy significantly less area in the same 90 nm process.

In [20], [21] optimization is performed to minimize power with frequency constraint where 100 MHz frequency is targeted. In our proposed approach, we report a substantially less deviation of 0.0485% (for 2 GHz) as compared to the deviation of 0.1% (for 100 MHz) reported in [20]. The VCO power deviation in this work is close to that reported in [20].

The power consumption in the proposed technique is expected to reduce further if we accept a little higher value of phase noise which is a trade-off case with the power consumption. It is worth noting that the simultaneous minimization of VCO power and phase noise with process variations are the extra considerations in our report. Moreover, the proposed technique is very much generic one which can be seamlessly applied to 45 nm technology also. The simulation of final optimized physical design yields the oscillations depicted in Fig. 3. Fig. 4 shows the phase noise plot. The oscillation frequency variation with control voltage is shown in Fig. 5 and the power measurements in Cadence environment is given in Fig. 6.

The optimized parasitic and process variation aware physical layout of the 13 stage CSVCO is depicted in Fig. 7. In this paper, we report the difference to be 299.18 MHz as compared to 630 MHz reported in [15]. Apart from the significant improvement in frequency, the phase noise and the power consumption values are found to be $-87.71 \text{ dBc/Hz}$ and 765.641 $\mu$W respectively. These values are very close to the IDEA predicted global minimum values at the desired frequency of oscillations. The process corner variation analysis of the final optimal robust optimal CSVCO is depicted in Fig. 8 which verifies its robustness.

V. Conclusion

The CSVCO is designed for optimal performance by using effective multi-objective evolutionary technique IDEA. The parasitics are extracted from an optimized layout using parasitic-aware model-based objectives. The actual extracted logic and interconnect parasitics are included in the models of objectives for CSVCO. The IDEA is again used to optimize power consumption and phase noise to achieve a target frequency of 2 GHz with the process constraints. The process variation-aware design of the optimal CSVCO is also reported here. The difference in frequency from the worst case to nominal case observed from the physical layout of the circuit is 299.18 MHz only which shows the robustness of the design. The optimum values of power consumption and corresponding phase noise are 765.641 $\mu$W and $-87.71 \text{ dBc/Hz}$ at 1 MHz offset. This work can be further extended to include many other performance objectives for optimization.
Power Efficient VCO Circuit with Performance Augmentation

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\textsuperscript{2}Research scholar, ECE Department, ITM University, Gwalior (MP), India
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\textsuperscript{4}Professor, AISECT University, Bhopal (MP), India

Abstract

This paper proposes various techniques for the designing of VCO (voltage controlled oscillator) circuit. Oscillator circuits are used in many electronic circuits. Certain process parameters should be taken care of while designing a oscillator. With the use of oscillator in both analog and digital fields, trade-off between parameters should be taken care of while modeling any circuit. With scaling of transistor size, power consumption in the circuit is the main reason for concern for efficient performance of the circuit designed. Having modification in the circuit with techniques like FinFET, MTCMOS, SVL and AVL have not only enhanced the performance of the circuit but reduced the leakage power in the circuit designed too. By applying leakage reduction techniques in the VCO circuit, efficiency in the circuit has increased with faster speed and lower noise. With the proposed design of the VCO circuit, better oscillation frequency is being observed. The circuits are simulated in Cadence Virtuoso tool at 45 nm technology.

Keywords: VCO, FinFET, MTCMOS, SVL, AVL, Speed, Frequency

I. INTRODUCTION

Oscillator circuit is used in electronic equipments. VCO circuit is used in the field of communication system for the generation of the periodic signal. In the digital domain, these periodic signal is used for the generation of the timing signals. While in the analog domain it is used as frequency signals. A VCO circuit is a function of voltage and frequency signal. With the change in the applied voltage, a change in the frequency takes place. Thus VCO circuit for better and efficient performance is the main objective of the designer for designing the circuit in the changing trend of technology. VCO circuit shows linearity when plotted against voltage and frequency. VCO circuit suffers the effect of noise, speed and leakage power in the circuit. So various leakage reduction techniques are being implied in the VCO circuit for better output response.

VCO circuit can be designed using various techniques like LC (Inductor-Capacitor) circuit, ring oscillator, Schmitt Trigger etc. For lower power consumption, the VCO circuit is designed using the ring oscillator. Among this other advantages of designing VCO using ring oscillator is it is easy to design, smaller chip area and have larger signal swing. But while designing the VCO circuit, uncertainty jitter should be taken into consideration. In ring oscillator VCO frequency of the circuit is proportional to delay time.

\[
F_{osc} = \frac{1}{2NT_d}
\]

VCO circuit can be designed using various methods. VCO circuit designed using LC topology provides higher figure of merit, tuning range etc in the circuit. The circuit is simulated at different channel length like 130nm, 90nm, 65nm and 45nm respectively. The comparisons of all these are made and much effective result are observed in 45nm technology [1]. Ring oscillator VCO circuit is being...
designed for higher speed and noise reduction in the circuit. Lower power dissipation is acquired in the circuit with high stability in the design. It is useful in case of high frequency application [2]. Simulating of VCO circuit and further using it for frequency divider can be used as one of its application. The use of the circuit in both analog and digital domain makes it a highly important resource. Thus designing of the circuit for driving higher load is needed and also with lower supply voltage consumption. Designing of the circuit for maximum frequency oscillation and minimum leakage power is essential for any VCO circuit [3]. One application of ring oscillator circuit is random number generation. So designing of the random number generator with different oscillator topologies are been calculated. The comparison of different topologies based on their output is observed [4]. VCO circuit for better performance is being simulated using various techniques. A better output result is obtained using the Schmitt trigger based topology. A circuit with lower power consumption and higher operating speed is more efficient. Schmitt Trigger based proposed circuit is used in this manner having higher noise immunity, faster speed of operation and lower power consumption [5]. MTCMOS technique is being applied in the two-stage Schmitt Trigger circuit for the reduction of leakage power in the circuit. The circuit is simulated at different supply voltages and the performance of the circuit is measured and calculated [6].

Comparison of various leakage reduction techniques are being done in the Schmitt Trigger circuit. Performance of the circuit is observed and the parameters are calculated. Effects of various techniques in the circuit are observed [7]. In different circuit, i.e., in half adder cell the leakage reduction is taken care of using low power diode approach. Using diode approach in the circuit leads to effectively decrease in the leakage current and also increase the speed of operation in the circuit [8].

II. PROPOSED CIRCUIT

While designing of any circuit, care must be taken in power consumption of the circuit. With the effect of power consumption i.e., static power and dynamic power, speed of the operation is also taken into consideration. Circuit should consume low power and must operate at high speed. Different leakage reduction techniques are being applied in the circuit for lowering the leakage power in the circuit and for enhancing the performance in the circuit.

Different VCO circuits designed in this paper:

1. Ring Oscillator VCO using CMOS
2. Ring Oscillator VCO using FinFET
3. MTCMOS in Ring Oscillator VCO
4. SVL technique in Ring Oscillator VCO
5. AVL technique in Ring Oscillator VCO

1. Ring Oscillator VCO Using CMOS

Ring Oscillator based VCO circuit consist of 2 stages. The former one is the input stage and the later one is the ring oscillator circuit as shown in Fig1. Ring oscillator circuit consists of five inverter circuit joined in series. This circuit is known as current starved type VCO circuit. The inverter circuit in the ring oscillator consists of complimentary pair of transistors which function as a current source in the circuit. Current source in the circuit helps in controlling and limiting the current that is being supplied to the inverter. Current mirror in the circuit helps in controlling the current starved in the circuit and also delay in the circuit designed. Input stage of VCO circuit has high input impedance. It consists of an additional pair of transistor added in the beginning of the circuit.

![Fig1. VCO Using Ring Oscillator](image-url)
place and thus the total capacitance is the sum of both input and output capacitance of the circuit.

The DC voltage helps in controlling the operating frequency of the VCO which further adjust the current after each inverter stage in the circuit.

2. **Ring Oscillator VCO Using FinFET**

VCO circuit is being designed using FinFET technology. The name FinFET is due to the fact that an additional fin is added to the transistor. FinFET came into existence for the reduction of the leakage power and other short channel effects in the circuit. Channel of the transistor is placed above the body and gate terminal is connected to it from three directions. A controllable output is acquired using this. VCO ring oscillator is shown in Fig 2.

![Fig2. VCO Ring Oscillator Using FinFET](image)

A better controlling of the voltage with higher output resolution is achieved using FinFET technology. Many gate terminals are joined to it for better operation of the device. Thus it is also known as dual gate or multi gate device.

Scaling of the transistor can be done up to a certain level after that short channel effects gets introduced. Thus FinFET is being introduced to overcome this drawback. The fin in FinFET is made up of thin silicon. The main reason of using FinFET is for low power operation, lower voltage of operation, higher speed and lower static power consumption in the device.

3. **MTCMOS in Ring Oscillator VCO**

For minimizing leakage in the circuit various technique are being introduced. One of the technique is MTCMOS. MTCMOS stands for “Multiple-Threshold CMOS”. A high threshold PMOS and high threshold NMOS is introduced in the circuit at the place of VDD and GND respectively. The source terminal of the high threshold PMOS and NMOS are connected to the actual VDD and GND terminal of the circuit respectively. The drain terminal of the PMOS and NMOS will act as virtual VDD and virtual GND for the circuit. Leakage power in the circuit is reduced using the higher threshold transistor in place of actual VDD and GND and thus enhance the performance of the circuit. The supply voltage for the PMOS is 0 V and for NMOS is 0.7 V. The main drawback of this technique is the sizing of the sleep transistor. MTCMOS in VCO is shown in Fig 3.

![Fig3. MTCMOS technique in VCO Using Ring Oscillator](image)
4. SVL technique in Ring Oscillator VCO

SVL stands for “Self-controllable voltage level”. SVL technique is introduced to overcome the limitations of the MTCMOS technique. It is of two types, L-SVL and U-SVL. It can work separately or both can be introduced in the circuit at the same time. When the oscillator circuit is in active state then Upper Vcont = low (0) and lower Vcont = high (1), then both the sleep transistor in upper and lower part is in ON state. Due to this maximum supply voltage and minimum ground stage voltage is provided to the circuit. Thus the operating speed of the circuit is increased. When the circuit is off then Upper Vcont = high (1) and lower Vcont = low (0). Thus minimum supply voltage and higher ground level is provided to the circuit. This will effectively decrease the leakage current in the circuit. SVL technique in VCO is shown in Fig4.

5. AVL technique in Ring Oscillator VCO

AVL stands for “Adaptive voltage level” technique. VCO circuit using AVL is shown in Fig5. It is of two type likewise as SVL i.e., AVL-G and AVL-S. AVL-G is the technique when the additional sleep transistor is connected at the ground terminal, while AVL-S is the technique when the sleep transistor is connected to the supply. Both the technique are being applied in the circuit to enhance the performance of the circuit. AVL-G leads to increase in ground level in the circuit when the circuit is in active mode. It leads to decrease in the leakage current when the circuit is in standby or cutoff mode. AVL-S technique helps in reducing the gate leakage current in the circuit.

III. SIMULATION RESULT

The parameters calculated for the comparison of the various VCO circuits:

I. Efficiency
II. Voltage Gain
III. Delay
IV. Leakage Power

V. Oscillation Frequency

Table I shows the comparison table of various parameters calculated for the design:

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Parameter(s)</th>
<th>VCO circuit using CMOS</th>
<th>VCO circuit using FinFET</th>
<th>MTC MOS in VCO</th>
<th>SVL in VCO</th>
<th>AVL in VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Efficiency (%)</td>
<td>7.38</td>
<td>7.75</td>
<td>13.35</td>
<td>15.76</td>
<td>16.28</td>
</tr>
<tr>
<td>2.</td>
<td>Voltage Gain (dB)</td>
<td>0.198</td>
<td>0.493</td>
<td>0.690</td>
<td>0.691</td>
<td>0.695</td>
</tr>
<tr>
<td>3.</td>
<td>Delay (sec)</td>
<td>2.35e-8</td>
<td>5.177e-9</td>
<td>5.175e-9</td>
<td>5.165e-9</td>
<td>5.163e-9</td>
</tr>
<tr>
<td>4.</td>
<td>Leakage Power (pW)</td>
<td>8.725</td>
<td>7.95</td>
<td>7.22</td>
<td>5.23</td>
<td>4.375</td>
</tr>
<tr>
<td>5.</td>
<td>Oscillation Frequency</td>
<td>42553</td>
<td>19316</td>
<td>19323</td>
<td>19361</td>
<td>19368</td>
</tr>
</tbody>
</table>

The comparison chart for the above parameters are shown in respective figures from Fig 6(a) to Fig 6(e) respectively.
OUTPUT GRAPHS OBTAINED

A. The output of VCO is shown in Fig7. The input supplied is in the form of voltage and output obtained is in the form of frequency.

B. Leakage Power graph in VCO is shown in Fig8.

IV. CONCLUSION

With the inclusion of the leakage reduction technique in the VCO circuit a vast enhancement in the performance of the circuit is observed. A fineness in the output is observed using FinFET technology in place of CMOS. Using FinFET, MTCMOS, SVL and AVL efficiency in the circuit has increased drastically. The efficiency of the circuit changed from 7.38% to 7.75%, 13.35% 15.76 and 16.28% respectively. A relatively increase in the voltage gain is also observed using the proposed design. A higher speed of operation is acquired in the circuit. It changed from 23.5 nsec in CMOS based to 5.163 nsec using AVL technique respectively. Leakage power in the circuit has changed from 8.725 pW in CMOS based to 7.95pW, 7.22pW, 5.23pW and 4.375pW using FinFET, MTCMOS, SVL and AVL technique respectively. The oscillation frequency of the circuit has increased drastically from CMOS to FinFET to other techniques. A better performance in the circuit is acquired using AVL technique. A higher performance in the parameters like efficiency, voltage gain, delay, leakage power and frequency is observed.

ACKNOLEDGEMENT

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REFERENCES


Design and Performance Analysis of Current Starved VCO for PLL using SVL Technique

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In the recent electronics, integrated circuits have been designed using complementary metal oxide semiconductor (CMOS). In 1963, Frank Wanlass at Fairchild technologies first examined the logic gate using CMOS VLSI [1]. With the improvement of Integrated Circuit (IC) technologies, communication systems and microprocessors are mainly operating at several gigahertz frequencies with low power, small chip area and an agreeable cost [2]. Nowadays is communications craving, requiring faster and more dependable ways to give an information flow. Voltage Controlled Oscillator finds expansive applications in many areas such as communication systems, wireless systems, digital circuits and power systems [3]. It is to designs an output signal which oscillates at the similar frequency as the input signal. The design is implemented in cadence virtuoso tool in 45nm CMOS technology at 0.7V power supply. Measured performances shows that leakage current, noise and power consumption in SVL technique is reduced as current starved voltage controlled oscillator.

Keywords: Ring Oscillator, Current Starved VCO, Power consumption, Leakage Current

1. INTRODUCTION

Most of the communication standards working together today are mobile, Wi-Fi and Bluetooth on the same chip system. We want to download music,
videos, make a call on the move, in a car, train or an aero plane [4]. To be portable, these mobile communication systems have to be relatively small, light and power efficient [5]. Voltage-controlled Oscillator (VCO) is the key component and challenging building blocks in a transceiver system. It produces the local oscillator signals which are used to carry radio frequency signals in transceivers. Voltage Controlled Oscillators are also utilized in analog music synthesizers. In 1980s audio frequency voltage controlled oscillators employed in musical contexts were fully removed but from the 1990s on, pure software was the primary sound-generating method, but Voltage Controlled Oscillator have come to be rapidly growing and grateful to the drawbacks.

There are two different categories of voltage controlled oscillator used in phase locked loop (PLL) current starved VCO and source coupled VCO [6]. This paper focuses on the current starved VCO whose working is same as ring oscillator. A ring oscillator is a type of non-linear oscillator [7]. This device is built of a quantity of NOT gates whose output oscillates among two voltage level corresponding right and wrong. The inverters or gates are joined in a closed loop; the output at the end inverter is fed return into the initial [8]. It can be present that the utmost output of a chain of an odd number of inverters is the reasonable NOT gates of the initial input since an only inverter estimates the logical NOT of its output. Ring oscillator is built a number of inverter and spherical chain is also built in the same condition; in this condition last output is the equal as the input [9]. This determines output is maintained a finite amount of duration later the start the input is declared and the feedback at the end of output to the input reason oscillation. So, three or more stages need to be cascaded to provide a ring oscillator and Figure 1 presents the block diagram of 5-stage ring oscillator. The frequency of oscillator builds upon the quantity of stages and also the time delay of every stage. The ring oscillators calculated with a chain of delay stages have composed great interest by reason of their numerous essential features. These captivate features are as follow: (i) It can achieve its oscillations at low voltage and can be electrically tuned. (ii) It can supply high-frequency oscillations with dissipating low power. (iii) Because of their basic structure, it can accumulate multi-phase outputs.

In recently, SVL technique is the most prevailing methodology in industry. SVL technique is applied to reduce power consumption and leakage current [10]. The proposed work verifies the analysis of SVL over current starved VCO and show that the applied SVL technique for supply voltage produces the excessive reduction in leakage current. In this paper current starved VCO is performed using SVL technique. It is more desirable than CMOS technology. It is shown in parameters calculated. Rest of the paper is as follows: section II gives brief description of Current Starved VCO, Section III, description of technique, Simulation work and results discussion is done in section IV, Finally section V concludes the paper.
2. CURRENT STARVED VCO DESIGN

Wireless system is widely used in communication system because it provide less area faster speed and low power consumption. The working of current starved VCO is almost same as ring oscillator and it behavior is also consistent to that. Figure 1 show the circuit diagram of ring oscillator. A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To attain oscillation, the ring must provide a phase shift of $2\pi$ and have unity voltage gain at the oscillation frequency.

From the schematic five stage current stage VCO is shown in figure 2, it is check out of middle PMOS M1 and NMOS M2 operate as inverter while upper PMOSM13 and NMOSM14 act as current source. The inverter designed is given in figure 3. The current source limits the current applied to the inverter. In other words, the inverter is starved for current. PMOSM11 and NMOSM12 drain currents are the resemblance and are set by the input control voltage. The current in M11 and M12 are mirrored each inverter/current source stage respec-

![Five Stage Ring Oscillator](image1)

**FIGURE 1**
Five Stage Ring Oscillator

![Schematic Circuit of Current Starved VCO](image2)

**FIGURE 2**
Schematic Circuit of Current Starved VCO
Ankit Srivastava et al.

The upper PMOS transistors are connected to the gate of M12 and source voltage is implemented to the gate of all lower NMOS transistors.

The oscillation frequency of the current starved VCO for $N$ (an odd $\geq 5$) of stages is

$$F_{osc} = \frac{1}{N} \ast Td \quad (1)$$

$$\frac{1}{N \cdot C_{tot} \cdot V_{DD}} \quad (2)$$

Where, $Td$ is the time delay. The maximum VCO oscillation frequency then,

$$V_{max} = V_{DD} \quad (3)$$

The bias theory is build with the help of transistors PMOS and NMOS. The whole arrangement is in such a way that it provides a controlled bias current and a controlled voltage in a manner that the transistors of delay cell remains in saturation region for the whole control voltage range. The inverter schematic, shown in Figure 3, current starving factor in inverter i.e. When current sources are active Vdd is given to the inverter and current is applied to inverter which leads inverter on and oscillations are produced but when current sources are off then no current is provided to inverter hence inverter will stop working and oscillations will not be produced.

FIGURE 3
Schematic Circuit of Inverter
3. CURRENT STARVED VCO USING SVL TECHNIQUE

3.1. Self Voltage Level Technique
Self voltage level technique is applied on the Current Starved VCO circuit. The SVL circuit commonly consists of a lower SVL circuit and an upper SVL circuit. The lower SVL circuit is formed pull down n-MOSFET switch which is connected in parallel with series connected two p-MOSFET resistors. The pull down n-MOSFET switch and only one of the PMOS resistors are handled by a complement square wave clock (Clk) signal. The upper SVL circuit is formed by a pull up p-MOSFET switch which is joined in parallel with series connected two n-MOSFET resistors. The pull up p-MOSFET switch and n-MOSFET only one resistors are handled by a square wave clock (Clk) signal.

The SVL circuit (lower and upper) is used one by one on the circuit and various circuit parameters were calculated like leakage current, leakage power, noise and power consumption as shown further in simulation results. The circuit has operate in two modes first is the active mode and second is the standby mode. Active mode is the normal operational mode of the load circuit in which the upper and the lower SVL circuit which do one’s best to make the load circuit of Current starved VCO act normally to produce its desired functionality. In Standby mode the load circuit avoids its normal operation.

3.1.1. Upper SVL Technique
In the active mode of Figure 4 when the load circuit is active, in this case upper SVL will turn ON p-MOSFET (Psw1) switch and turn OFF both n-MOSFET (Nsw1 and Nsw2) resistors. Thus the ON p-MOSFET switch

![FIGURE 4](image)
Circuit Diagram of U-SVL Technique
will connect a direct path connection of the supply voltage Vdd to the load circuit. Hence the circuit operates in standby mode the circuit controlling is low, this low pulse as a complement in upper SVL will turn OFF p-MOSFET switch and turn ON both n-MOSFET resistors and the upper PMOS and NMOS transistor connected in series and supply voltage VDD is applied to the transistor. The gate leakage current maybe decreases in this way.

3.1.2. Lower SVL Technique

In the active mode of Figure 5 the circuit will turn ON the n-MOSFET (Nsw3) switch and turn OFF both the serially connected Psw2 and Psw3 resistors. Thus ground supply is provided directly by ON n-MOSFET to the circuit for operation. On the other part standby mode as a signal are low then n-MOSFET switch is OFF and both p-MOSFET resistor turn ON connecting a ground supply to the circuit.

3.1.3 Current Starved Voltage Controlled Oscillator Using Combined (LSVL + USVL)

The upper and lower SVL is applied together to the load circuit as shown in Figure 6. To give decreased supply voltage and enhance ground voltage level to the circuit in standby mode of operation and supports normal supply voltage and ground voltage in active mode.

These leakage current waveforms are used for calculating the leakage power and the total dissipated power at respective varying supply voltage.
4. SIMULATION RESULT

4.1. Leakage Power

The leakage power in the current starved VCO circuit is given as follows in Equation (4)

\[ P_{\text{Leakage}} = VDD \times \Sigma I_{\text{leakage}} \]  

\[ I_{\text{leakage}} = \text{penetrating leakage current in the turn OFF transistors} \]
Leakage power which directly depends upon leakage current from CMOS implemented current starved circuit and SVL (upper and lower SVL) based current starved VCO circuit. Figure 8 reflects graphical analysis of leakage power reduction.

### 4.2. Leakage Current

Leakage current of the current starved VCO is calculated with the help of this equation.

\[
I_{\text{leak}} = I_{\text{sub-thr}} + I_{\text{gate-ox}} \tag{5}
\]

Where, \(I_{\text{sub-threshold}}\) = sub-threshold leakage current, \(I_{\text{gate-ox}}\) = gate – oxide leakage current.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Simple Current Starved VCO</th>
<th>U-SVL</th>
<th>L-SVL</th>
<th>Both (L-SVL and U-SVL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7V</td>
<td>12.80nW</td>
<td>9.91nW</td>
<td>6.86nW</td>
<td>0.97nW</td>
</tr>
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<td>0.8V</td>
<td>17.45nW</td>
<td>12.7nW</td>
<td>8.70nW</td>
<td>2.34nW</td>
</tr>
<tr>
<td>0.9V</td>
<td>20.90nW</td>
<td>25.09nW</td>
<td>13.02nW</td>
<td>1.67nW</td>
</tr>
<tr>
<td>1V</td>
<td>26.01nW</td>
<td>20.95nW</td>
<td>14.89nW</td>
<td>3.99nW</td>
</tr>
</tbody>
</table>

**FIGURE 8**

Graph of Leakage Power
TABLE 2
Leakage Current

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Simple Current Starved VCO</th>
<th>U-SVL</th>
<th>L-SVL</th>
<th>Both(L-SVL and U-SVL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7V</td>
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<td>26.99nA</td>
<td>18.21nA</td>
<td>11.22nA</td>
<td>3.59pA</td>
</tr>
</tbody>
</table>

FIGURE 9
Graph of Leakage Current

Basically leakage current is found in two ways, firstly standby mode and other one is active mode.

4.3. Total Power
The total power dissipation arises in two conditions. Firstly due to the static power in this condition, it is connected direct path between VDD to VSS ground. And another one is dynamic power this power is arises due to switching capacitances and the unit of power is watt.

TABLE 3
Total Power Dissipation

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current Starved VCO</th>
<th>U-SVL</th>
<th>L-SVL</th>
<th>Both(L-SVL and U-SVL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7V</td>
<td>2.71nA</td>
<td>6.78nA</td>
<td>1.73nA</td>
<td>0.24pA</td>
</tr>
<tr>
<td>0.8V</td>
<td>6.07nA</td>
<td>8.24nA</td>
<td>4.89nA</td>
<td>6.72pA</td>
</tr>
<tr>
<td>0.9V</td>
<td>6.24nA</td>
<td>9.04nA</td>
<td>7.83nA</td>
<td>7.83pA</td>
</tr>
</tbody>
</table>
4.4. Noise of Current Starved Voltage Controlled Oscillator
Noise produced by electronic device and is a random fluctuation in an electronic signal. The graph of noise is shown in figure

5. CONCLUSION
SVL based Current starved VCO circuit is designed and simulated on cadence virtuoso tool at 45nm semiconductor node. In this paper, a new leakage reduction technique is employed to SVL based current starved
VCO for performance improvement in terms of leakage, power and noise. The efficiency of the proposed leakage reduction techniques is demonstrated using USVL, LSVL and than combination of both is applied in the circuit. The SVL based current starved circuit also shows a great reduction in terms of circuit noise as the delay reduces to 31% from the noise analyzed in conventional current starved circuit. In USVL, LSVL and combination of USVL+LSVL based current starved the leakage current observed is 1.89pA at 0.8 volt supply However the total power consumption in SVL based current starved VCO is lower than Conventional current starved VCO design which is estimated nearly to be 6.24pA at 1 volt supply. Thus the proposed circuit shows tremendous reduction in terms of leakage current, noise, and total power consumption. The different values we used for simulation: supply voltage = 0.7V, capacitance = 1µf and temperature = 27ºC. The simulation result of different parameter based current starved voltage controlled oscillator with different voltage is shown below in the figure 12.

6. ACKNOWLEDGEMENT

This work has been supported by ITM University, Gwalior along with the calibration cadence design system, Bangalore for providing the tools and technology for the work to be completed.
REFERENCES


Comparative Study Of Different Voltage Controlled Oscillator Using CMOS Technology

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Abstract

Oscillators are integral part of many electronic systems. An oscillator is an electronic device used for the purpose of generating a signal. Most electronic signal processing systems require frequency or time reference signals. This paper deals with the analysis and design of CMOS oscillators more specifically voltage controlled oscillators (VCOs). Voltage Controlled Oscillator is an electronic oscillator whose output frequency is controlled by a voltage input. VCO can be built using many circuit techniques. Primarily, there are two methods of designing CMOS VCOs, one uses a ring oscillator and other uses a Schmitt trigger. Though there are so many design requirements of a VCO, which are phase stability, large electrical tuning range, linearity of frequency verses control voltage, large gain factor, capability of accepting wideband modulation and low cost but the most important factor in designing the VCO is the linearity, on the basis of which the comparison between CMOS VCOs is described. With respect to digital phones that use these circuits, low power consumption, small size, and leakage current and low fabrication costs are important design factors. In this paper main objective is to reduce the leakage current, voltage and power consumption. It is observed by the parameters calculated.

Keywords: Leakage current, Average Power, Ring oscillator, Voltage Controlled Oscillator.

1. Introduction

The crystal oscillator, mainly, cannot generate a frequency up to 100MHz, so it makes use of off-chip as the reference signal. In the chip, a Voltage Controlled Oscillator is applied to give the higher frequency periodic signal for the systems [1]. One of the causes that VCO is a usually utilized circuit is that it is a fundamental component of a PLL. PLL finds expansive applications in many areas such as communication systems, wireless systems, digital circuits and power systems [2]. It is to compose an output signal which oscillates at the similar frequency as the input signal. When the Phase Locked Loop is in lock, it acts as follows: The phase detector develops an output whose direct current value is proportional to the phase difference in middle of the input periodic signal which arranges the oscillator output [3]. The low pass filters than reduce the high frequency change in the phase detector output because the VCO input signal is direct current and this restricts the oscillation frequency of the VCO equal to that of the input signal [4]. At one time lock, Phase Locked Loop tracks the input frequency because of little variation. In this case the phase difference in middle of the input signal and the VCO output will enhance, due to the fact the direct current output of the phase detector and low pass filter will increase and the frequency of the input signal will also expand [5]. For that reason, the frequency will rise to save the increase in the frequency of the input and its VCO of the input will also soar. It is realized that the Voltage Controlled Oscillator frequency will increment at the end of the accurate number and then reduce to the desired value [6]. As the loop won’t retake close up to the Voltage Controlled Oscillator frequency similar to the input frequency thus the static phase inaccuracy is put into order to its proper value [7].
which necessitates larger power consumption [8]. The two high frequency blocks in PLL, namely the Voltage-Controlled Oscillator (VCO) and the Current Controlled Oscillator are most essential in the feasibility of integration in a CMOS process [9]. But in this thesis, main topic is Voltage Controlled Oscillator, so we briefly describe it. In Voltage Controlled Oscillator (VCO), let us discuss oscillator. The first electronic oscillating was constructed by Elihu Thomson in 1892 [10]. Oscillators are circuits that produce an output signal at a certain frequency with DC power supply as it transforms direct current from a power supply to an alternating current signal. Oscillators are extensively applied in different electronic devices [11]. Clock signals that regulate quartz clocks and computer but oscillators contain signals broadcast by radio and television transmitters and sounds produced by electronic beepers and video games [12]. An oscillator must accommodate amplification and the output is feedback to sustain the input. Abundant power must be feedback to the input for the oscillator to control itself as in occurrence of signal generator. The oscillator is self-controlled, since the feedback signal is regenerative i.e. positive feedback [13].

2. Proposed Design

Different leakage reductions Technique are being applied in the VCO circuit for lowering the leakage power and leakage current in the circuit for enhancing the performance in the circuit. Different VCO circuits designed in this paper are following.

2.1 Ring oscillator VCO using CMOS

Ring Oscillator based VCO circuit consists of 2 stages. The former one is the input stage and the later one is the Ring Oscillator circuit as shown in Fig.4.1. Ring oscillator circuit consists of five inverter circuits joined in series. This circuit is known as current starved type VCO circuit. The inverter circuit in the Ring Oscillator consists of complimentary pair of transistors which function as a current source in the circuit. Current source in the circuit helps in controlling and limiting the current that is being supplied to the inverter. Current mirror in the circuit helps in controlling the current starved in the circuit and also delay in the circuit designed. Input stage of VCO circuit has high input impedance. It comprises of an additional pair of transistor added in the beginning of the circuit. The frequency of the circuit is defined as the time taken by the circuit for charging and discharging of the circuit takes place, thus the total capacitance is the sum of both input and output capacitance of the circuit. The DC voltage helps in controlling the operating frequency of the VCO which further adjusts the current after each inverter stage in the circuit.

2.2 MTCMOS in Ring Oscillator VCO

For minimizing leakage in the circuit, various techniques are being introduced. One of the technique is MTCMOS. MTCMOS stands for “Multiple-Threshold CMOS”. A high threshold PMOS and high threshold NMOS are introduced in the circuit at the place of VDD and GND respectively. The source terminal of the high threshold PMOS and NMOS is connected to the actual VDD and GND terminal of the circuit respectively. The drain terminal of the PMOS and NMOS will act as virtual VDD and virtual GND for the circuit. Leakage power in the circuit is reduced using the higher threshold transistor in place of actual VDD and GND, thus enhancing the performance of the circuit. The supply voltage for the PMOS is 0 V and for the NMOS is 0.7 V. The main drawback of this technique is the sizing of the sleep transistor. MTCMOS in VCO is shown in Figure 1.3.
2.3 AVL Technique in Ring Oscillator VCO

AVL stands for “Adaptive Voltage Level” technique. VCO circuit using AVL is displayed in Fig.4.5. It is of two types likewise SVL i.e., AVL-G and AVL-S. AVL-G is the technique when the additional sleep transistor is connected at the ground terminal, while AVL-S is the technique when the sleep transistor is connected to the supply.

3. Simulation Result

The proposed FinFET based Voltage Controlled Oscillator (VCO) has been designed using the cadence virtuoso tool of IC 6.1 version and the simulations are performed using the 45nm technology. The different values used for simulation were supply voltage = 0.7V, capacitance = 1µf and temperature = 27ºC. The simulation result of different technique based Voltage Controlled Oscillator with different power is shown below in the Table 1.1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Simple VCO</th>
<th>MTCMOS based VCO</th>
<th>AVL based VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power (W)</td>
<td>84.12nW</td>
<td>64.42nW</td>
<td>36.02nW</td>
</tr>
<tr>
<td>Leakage Current (A)</td>
<td>10.64pA</td>
<td>7.69pA</td>
<td>8.34 nA</td>
</tr>
</tbody>
</table>

Table 1.1 Different Technique based Voltage Controlled Oscillator

3.1 Parameters of simple VCO

The functionality of the Voltage Controlled Oscillator using FinFET is defined by the simulation result.

3.1.1 Transient Response

The transient response shows the response of a system in the form of output by giving different input to it.
Figure 3.1 indicates input/output waveform of Voltage Controlled Oscillator with the help of cadence virtuoso tool with schematic result analysis.

3.1.2 Leakage Current
Leakage current of the Ring Oscillator is estimated during the standby mode. To calculate the leakage current of the current starved VCO, NMOS transistor is desired to measure the leakage current that is connected at the pull down network below the whole circuit. Sleep transistor is OFF for this technique whenever leakage current calculation is estimated. Leakage current is derived by the equation given below:

\[ P_{\text{leakage}} = I_{\text{leakage}} \times V_{DD} \]

The leakage current versus time graph is shown in Figure 3.3. The calculate leakage current is 1.64pA.

3.1.3 Average Power
The average power is also calculated. The average power dissipation happens due to the static and dynamic power dissipation and the unit of power is watt. It needs battery power consumption and is linked to the cooling. The average power is calculated as 16.71nW.

3.2 Parameters of MTCMOS based VCO
3.2.1 Transient Response
The transient response shows the response of a system in the form of output by giving different input to it.

3.2.2 Leakage Current
For the design of Voltage Controlled Oscillator, it calculates 7.49pA. The leakage current versus time graph is illustrated in figure 3.6.
3.2.3 Average Power

The graph of average power of VCO using MTCMOS technique is shown in Figure 3.7. It helps us to read the values of the parameters that are calculated with the CADENCE virtuoso tool.

![Figure 3.7 Average Power versus Time Graph MTCMOS based VCO](image)

3.3 PARAMETER OF AVL BASED VCO

3.3.1 Transient Response

The transient response shows the response of a system in the form of output by giving different input to the circuit. It helps us to read the values of the parameters that are calculated with the CADENCE virtuoso tool.

![Figure 3.8 Transient Response of Voltage Controlled Oscillator](image)

3.3.2 Leakage Current

For the design of Voltage Controlled Oscillator, it calculates 5.18pA. The leakage current versus time graph is exhibited in figure 3.9.

![Figure 3.9 Leakage Current versus Time Graph Using AVL Technique](image)

3.3.3 Average Power

The graph of average power of VCO using AVL technique is illustrated in Figure 3.10. It helps us to read the values of the parameters that are calculated using the CADENCE virtuoso tool.

![Figure 3.10 Average Power versus Time Graph using AVL Technique](image)

4. Conclusions

With the help of the leakage reduction technique in the VCO Circuit, a vast enhancement in the performance of the circuit is observed. The average power in the circuit is changed from 84.12nw in CMOS based to 64.42nw,36.02nw using MTCMOS and AVL technique respectively. The leakage current in the circuit is changed from 10.64 pA in CMOS based to 7.69pA,8.34nA using MTCMOS and AVL technique respectively.

References


Analysis of Leakage Power suppression Technique for CMOS VCO in 45nm Technology

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²Professor, ECE Department, ITM University, Gwalior (MP), India
³Professor, AISECT University, Bhopal (MP), India

Abstract— This paper proposed SVL self voltage level technique for the designing of VCO (voltage controlled oscillator) circuit. Certain process parameters should be taken care of while designing of oscillator. With the scaling of transistor size power consumption in the circuit is the main reason for concern for efficient performance of the circuit designed. Having modification in the circuit with techniques SVL have not only enhanced the performance of the circuit but reduced the leakage power in the circuit designed too. By applying leakage reduction techniques in the VCO circuit, efficiency in the circuit has increased with faster speed and lower noise. The circuits are simulated in cadence virtuoso tool at 45 nm technology.

Keywords: VCO, CSVCO, Ring VCO, SVL, Leakage power, leakage current.

I. INTRODUCTION

VCO circuit is used in the field of communication system for the generation of the periodic signal. In the digital domain these periodic signal is used for the generation of the timing signals. While in the analog domain it is used as frequency signals. A VCO circuit is a function of voltage and frequency signal. With the change in the applied voltage apparent change in the frequency takes place. Thus VCO circuit for better and efficient performance is the main objective of the designer for designing the circuit in the changing trend of technology. VCO circuit shows linearity when plotted against voltage and frequency.

VCO circuit suffers the effect of noise, speed and leakage power in the circuit. So various leakage reduction techniques are being implied the VCO circuit for better output response.

VCO circuit can be designed using various techniques like LC (Inductor-Capacitor) circuit, ring oscillator, Schmitt Trigger etc. For lower power consumption the VCO circuit is designed using the ring oscillator and current starved VCO. Among this other advantages of designing VCO using ring oscillator and CSVCO is that they are easy to design, smaller chip area and have larger signal swing. But while designing the VCO circuit uncertainty jitter should be taken into consideration. In ring oscillator VCO frequency of the circuit is proportional to delay time.

II. PROPOSED CIRCUIT

While designing of any circuit, care must be taken in power consumption of the circuit. With the effect of power consumption i.e., static power and dynamic power, speed of the operation is also taken into consideration. Circuit should consume low power and must operate at high speed. SVL leakage reduction techniques are being applied in the circuit for lowering the leakage power in the circuit and for enhancing the performance in the circuit.

Different VCO circuits designed in this paper:

1. SVL technique in Ring Oscillator VCO
2. SVL technique in Current starved Oscillator VCO

SVL stands for “Self-controllable voltage level”. SVL technique is introduced to overcome the limitations of the MTCMOS technique. It is of two types, L-SVL and U-SVL. It can work separately or both can be introduced in the circuit at the same time. When the oscillator circuit is in active state then Upper Vcont = low (0) and lower Vcont = high (1), then both the sleep transistor in upper and lower part is in ON state. Due to this maximum supply voltage and minimum ground stage voltage is provided to the circuit. Thus the operating speed of the circuit is increased. When the circuit is off then Upper Vcont = high (1) and lower Vcont = low (0). Thus minimum supply voltage and higher ground level is provided.
to the circuit. This will effectively decrease the leakage current in the circuit. SVL technique in VCO is shown in Fig1.

2. SVL technique in Current starved Oscillator VCO

Self voltage level technique is applied on the Current Starved VCO circuit. The SVL circuit commonly consists of a lower SVL circuit and an upper SVL circuit. The lower SVL circuit is formed pull down n-MOSFET switch which is connected in parallel with series connected two p-MOSFET resistors. The pull down n-MOSFET switch and only one of the PMOS resistors are handled by a complement square wave clock (Clk) signal. The upper SVL circuit is formed by a pull up p-MOSFET switch which is joined in parallel with series connected two n-MOSFET resistors. The pull up p-MOSFET switch and n-MOSFET only one resistors are handled by a square wave clock (Clk) signal.

The SVL circuit (lower and upper) is used one by one on the circuit and various circuit parameters were calculated like leakage current, leakage power, noise and power consumption as shown further in simulation results. The circuit has operate in two modes first is the active mode and second is the standby mode. Active mode is the normal operational mode of the load circuit in which the upper and the lower SVL circuit which do one’s best to make the load circuit of Current starved VCO act normally to produce its desired functionality. In Standby mode the load circuit avoids its normal operation.

2.1 Upper SVL Technique

In the active mode of Figure 2 when the load circuit is active, in this case upper SVL will turn ON p-MOSFET (Psw1) switch and turn OFF both n-MOSFET (Nsw1 and Nsw2) resistors. Thus the ON p-MOSFET switch will connect a direct path connection of the supply voltage Vdd to the load circuit. Hence the circuit operates in standby mode the circuit controlling is low, this low pulse as a complement in upper SVL will turn OFF p-MOSFET switch and turn ON both n-MOSFET resistors and the upper PMOS and NMOS transistor connected in series and supply voltage VDD is applied to the transistor. The gate leakage current maybe decreases in this way.

2.2 Lower SVL Technique

In the active mode of Figure 3 the circuit will turn ON the n-MOSFET (Nsw3) switch and turn OFF both the serially connected Psw2 and Psw3 resistors. Thus ground supply is provided directly by ON n-MOSFET to the circuit for operation. On the other part standby mode as a signal are low then n-MOSFET switch is OFF and both p-MOSFET resistor turn ON connecting a ground supply to the circuit.

2.3 Current Starved Voltage Controlled Oscillator Using Combined (LSVL + USVL)

The upper and lower SVL is applied together to the load circuit as shown in Figure 4. To give decreased supply voltage and enhance ground voltage level to the circuit in standby mode of operation and supports normal supply voltage and ground voltage in active mode.

These leakage current waveforms are used for calculating the leakage power and the total dissipated power at respective varying supply voltage.
III. SIMULATION RESULT

3.1 Leakage Power
The leakage power in the current starved VCO circuit is given as follows in Equation (1)

\[ P_{\text{Leakage}} = V_{DD} \times \Sigma I_{\text{leakage}} \]  

\[ I_{\text{leakage}} \] penetrating leakage current in the turn OFF transistors

Leakage power which directly depends upon leakage current from CMOS implemented current starved circuit and SVL (upper and lower SVL) based current starved VCO circuit.

Figure 5 reflects graphical analysis of leakage power reduction.

Table 1 Leakage Power in CSVCO

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Simple Current Starved VCO</th>
<th>U-SVL</th>
<th>L-SVL</th>
<th>Both(L-SVL and U-SVL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7V</td>
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</tr>
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<td>0.9V</td>
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<tr>
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<td>14.89nW</td>
<td>3.99nW</td>
</tr>
</tbody>
</table>

Figure 5 Graph of Leakage Power in CSVCO

3.2 Leakage Current
Leakage current of the current starved VCO is calculated with the help of this equation.

\[ I_{\text{leak}} = I_{\text{sub-threshold}} + I_{\text{gate-oxide}} \]  

Where, \( I_{\text{sub-threshold}} \) = sub-threshold leakage current, \( I_{\text{gate-oxide}} \) = gate – oxide leakage current.

Basically leakage current is found in two ways, firstly standby mode and other one is active mode.

Table 2 Leakage Current in CSVCO

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Simple Current Starved VCO</th>
<th>U-SVL</th>
<th>L-SVL</th>
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</tr>
<tr>
<td>1V</td>
<td>26.99nA</td>
<td>18.21nA</td>
<td>11.22nA</td>
<td>3.59pA</td>
</tr>
</tbody>
</table>

Figure 6 Graph of Leakage Current in CSVCO

Figure 7 Leakage power waveform of Current Starved VCO using Combined (LSVL + USVL) Technique

Figure 8 Noise Waveform of Current Starved VCO Using Combined (U-SVL and L-SVL) Technique

Table 3 of various parameters calculated for the Ring oscillator VCO

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Efficiency (%)</td>
</tr>
<tr>
<td>2.</td>
<td>Voltage Gain (dB)</td>
</tr>
<tr>
<td>3.</td>
<td>Delay (sec)</td>
</tr>
<tr>
<td>4.</td>
<td>Leakage Power (pW)</td>
</tr>
</tbody>
</table>
IV. CONCLUSION

SVL based Current starved VCO circuit is designed and simulated on cadence virtuoso tool at 45nm semiconductor node. In this paper, a new leakage reduction technique is employed to SVL based current starved VCO for performance improvement in terms of leakage, power and noise. The efficiency of the proposed leakage reduction techniques is demonstrated using USVL, LSVL and than combination of both is applied in the circuit. The SVL based current starved circuit also shows a great reduction in terms of circuit noise as the delay reduces to 31% from the noise analyzed in conventional current starved circuit. In USVL, LSVL and combination of USVL+LSVL based current starved the leakage current observed is 1.89pA at 0.8 volt supply.

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References


