CHAPTER 4

LOW POWER VOLTAGE CONTROLLED
OSCILLATOR AUGMENTATION
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OBJECTIVE OF CHAPTER

This chapter proposes various techniques for the designing of VCO (Voltage Controlled Oscillator) circuit. Oscillator circuits are used in many electronic circuits. Certain process parameters should be taken care of while designing an oscillator. With the use of oscillator in both analog and digital field, trade-off between parameters should be adhered to while modeling any circuit. With the scaling of transistor size, power consumption in the circuit is the main reason for concern for efficient performance of the circuit designed. Modification in the circuit with techniques like FinFET, MTCMOS, SVL and AVL has not only enhanced the performance of the circuit but reduced the leakage power in the circuit design too. By applying leakage reduction techniques in the VCO circuit, efficiency in the circuit has increased with faster speed and lower noise. With the proposed design of the VCO circuit, better oscillation frequency is also being observed. The circuits are simulated in cadence virtuoso tool at 45 nm technology.

4.1 INTRODUCTION

Oscillator circuit is used in electronic equipments. VCO circuit is used in the field of communication system for the generation of the periodic signal. In the digital domain, This periodic signal is used for the generation of the timing signals, while in the analog domain it is used as frequency signals. A VCO circuit is a function of voltage and frequency signal. With the change in the applied voltage, apparent change in the frequency takes place. Thus VCO circuit with better and efficient performance is the main objective of the designer for designing the circuit in the changing trend of technology.
Ring Oscillator is cascaded combination of delay stages, connected in a closed loop chain. The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are: (i) It can easily design with the state-of-art integrated circuit technology (CMOS, BICMOS). (ii) It can achieve its oscillations at low voltage. (iii) It can provide high frequency oscillations with dissipating low power. (iv) It can be electrically tuned. (v) It can provide wide tuning range. (vi) It can provide multiphase outputs because of their basic structure. The oscillations frequency of a ring oscillator depends on the propagation delay per stage, and the number of stages used in the ring oscillator. As we have already mentioned, the ring oscillators is realized with N inverter stages. There are numerous types of inverter stages by which a ring oscillator can be realized. Designs of current starved type, for which the charging and discharging output capacitor current is limited by a bias circuit. Relative frequency deviations in term of temperature variations for 3-stages ring oscillators based on type of inverters stages. In general all frequency deviations have similar behavior, but the basic type and current starved with symmetrical load inverters have the highest, while current starved with output-switching inverter has the lowest sensitivity. The ratio of relative frequency deviations between basic type and current starved with output-switching inverters is 5:1.

Relative frequency deviations in term of power voltage supply variations for 3-stages ring oscillators based on type of inverters stages. The basic type and current starved with symmetrical load inverters have characteristics with negative slope, while current starved with output-switching and current starved with power-switching inverters have characteristics with positive slope. Absolute value of inverters sensitivity in function to power supply voltage variation is within a range of 10% excluding current starved inverter with power-switching inverters which has sensitivity of 5%. Taking into consideration the opposite slope characteristics of the relative frequency deviations in terms of power voltage supply variations of the mentioned inverters, we can conclude that is reasonable to design a ring oscillator composed of cascade chain of inverters. For example, odd numbered inverters can have positive, while even numbered negative slope. In this way, the relative frequency deviation in term of power voltage supply can be drastically reduced (more than 100%).
VCO circuit shows linearity when plotted against voltage and frequency. VCO circuit suffers the effect of noise, speed and leakage power in the circuit. So, various leakage reduction techniques are being implemented in the VCO circuit for better output response.

VCO circuit can be designed using various techniques like LC (Inductor-Capacitor) circuit, ring oscillator, Schmitt Trigger, etc. For lower power consumption, the VCO circuit is designed using the Ring Oscillator. Among this other advantages of designing VCO using Ring Oscillator is it is easy to design, with smaller chip area and having larger signal swing. But while designing the VCO circuit uncertainty jitter should be taken into consideration. In Ring Oscillator, VCO frequency of the circuit is proportional to the delay time.

\[ F_{\text{osc}} = \frac{1}{2NT_d} \]  

VCO circuit can be designed using various methods. VCO circuit which is designed using LC topology provides higher figure of merit, tuning range, etc in the circuit. The circuit is simulated at different channel length like 130nm, 90nm, 65nm and 45nm respectively. The comparisons of all these are made and much effective result is observed in 45nm technology [74]. Ring oscillator VCO circuit is being designed for higher speed and noise reduction in the circuit. Lower power dissipation is acquired in the circuit with high stability in the design. It is useful in case of high frequency application [75]. Simulating of VCO circuit and further using it for frequency divider can be used as one of its application. The use of the circuit in both analog and digital domain makes it a highly important resource. Thus, designing of the circuit for driving higher load is needed with lower supply voltage consumption. Designing of the circuit for maximum frequency oscillation and minimum leakage power is essential for any VCO circuit [76]. One application of Ring Oscillator circuit is random number generation. So designing of the random number generator with different oscillator topologies are been calculated. The comparison of different topologies based on their output is observed [77]. For better performance, VCO circuit is being simulated using various techniques. A better output result is obtained using the Schmitt trigger based topology. A circuit with lower power consumption and high operating speed is more efficient. Schmitt Trigger based proposed
circuit is used in this manner having higher noise immunity, faster speed of operation and lower power consumption [78]. MTCMOS technique is being applied in the two-stage Schmitt Trigger circuit for the reduction of leakage power in the circuit. The circuit is simulated at different supply voltages and the performance of the circuit is measured and calculated [79].

Comparison of various leakage reduction techniques is being undertaken in the Schmitt Trigger circuit. Performance of the circuit is observed and the parameters are calculated. Effects of various techniques in the circuit are observed [80]. In different circuits, i.e., in half adder cell the leakage reduction is taken care of using low power diode approach. Using diode approach in the circuit leads to effectively decrease in the leakage current and also increase the speed of operation [81].

4.2 PROPOSED CIRCUIT

While designing any circuit, care must be taken regarding power consumption of the circuit. With the effect of power consumption i.e., static power and dynamic power, speed of the operation is also taken into account. Circuit should consume low power and must operate at a high speed. Different leakage reduction techniques are being applied in the circuit for lowering the leakage power in the circuit and for enhancing the performance in the circuit.

Different VCO circuits designed in this paper:

1. Ring Oscillator VCO using CMOS
2. Ring Oscillator VCO using FinFET
3. MTCMOS in Ring Oscillator VCO
4. SVL technique in Ring Oscillator VCO
5. AVL technique in Ring Oscillator VCO

4.2.1 Ring Oscillator VCO Using CMOS

Ring Oscillator based VCO circuit consists of 2 stages. The former one is the input stage and the later one is the Ring Oscillator circuit as shown in Fig.4.1. Ring oscillator circuit
consists of five inverter circuits joined in series. This circuit is known as current starved type VCO circuit. The inverter circuit in the Ring Oscillator consists of complimentary pair of transistors which function as a current source in the circuit. Current source in the circuit helps in controlling and limiting the current that is being supplied to the inverter. Current mirror in the circuit helps in controlling the current starved in the circuit and also delay in the circuit designed. Input stage of VCO circuit has high input impedance. It comprises of an additional pair of transistor added in the beginning of the circuit. The frequency of the circuit is defined as the time taken by the circuit for charging and discharging of the capacitance at each inverter stage in the circuit. During transition, charging and discharging of the circuit takes place, thus the total capacitance is the sum of both input and output capacitance of the circuit. The DC voltage helps in controlling the operating frequency of the VCO which further adjusts the current after each inverter stage in the circuit

![Figure 4.1 VCO using Ring Oscillator](image-url)

Figure 4.1 VCO using Ring Oscillator
4.2.2 Ring Oscillator VCO Using FinFET

VCO circuit is being designed using FinFET technology. The name FinFET is due to the fact that an additional fin is added to the transistor. FinFET came into existence for the reduction of the leakage power and other Short Channel Effects in the circuit. Channel of the transistor is placed above the body and gate terminal is connected to it from the three directions. A controllable output acquired using this. VCO Ring Oscillator is shown in Figure 4.2.

![Figure 4.2 VCO Ring Oscillator using FinFET](image)

A better controlling of the voltage with higher output resolution is achieved using FinFET technology. Many gate terminals are joined to it for better operation of the device. Thus, it is also known as dual gate or multi-gate device.
Scaling of the transistor can be done up to a certain level as Short Channel Effects get introduced after that. Thus, FinFET is being introduced to overcome this drawback. The fin in FinFET is made up of thin silicon. The main reason of using FinFET is low power operation, lower voltage of operation, higher speed and lower static power consumption in the device.

4.2.3 MTCMOS in Ring Oscillator VCO

For minimizing leakage in the circuit, various techniques are being introduced. One of the technique is MTCMOS. MTCMOS stands for “Multiple-Threshold CMOS”. A high threshold PMOS and high threshold NMOS are introduced in the circuit at the place of VDD and GND respectively. The source terminal of the high threshold PMOS and NMOS is connected to the actual VDD and GND terminal of the circuit respectively. The drain terminal of the PMOS and NMOS will act as virtual VDD and virtual GND for the circuit. Leakage power in the circuit is reduced using the higher threshold transistor in place of actual VDD and GND, thus enhancing the performance of the circuit. The supply voltage for the PMOS is 0 V and for the NMOS is 0.7 V. The main drawback of this technique is the sizing of the sleep transistor. MTCMOS in VCO is shown in Figure 4.3.

![Figure 4.3 MTCMOS Technique in VCO using Ring Oscillator](image-url)
4.2.4 SVL Technique in Ring Oscillator VCO

SVL stands for “Self-controllable Voltage Level”. SVL technique is introduced to overcome the limitations of the MTCMOS technique. It is of two types, L-SVL and U-SVL. They can work separately or both can be introduced in the circuit at the same time.

When the oscillator circuit is in active state then Upper Vcont = low (0) and lower Vcont = high (1), and both the sleep transistors in upper and lower part are in the ON state. Due to this, maximum supply voltage and minimum ground stage voltage is provided to the circuit. Thus, the operating speed of the circuit is increased. When the circuit is OFF then Upper Vcont = max (1) and min Vcont = min (0). Thus, lower power supply and maximum ground leveled are provided to the circuit. This will effectively decrease the leakage current in the circuit. SVL technique in VCO is shown in Fig.4.4.

Figure 4.4 SVL in VCO using Ring Oscillator
4.2.5 AVL Technique in Ring Oscillator VCO

AVL stands for “Adaptive Voltage Level” technique. VCO circuit using AVL is displayed in Fig.4.5. It is of two types likewise SVL i.e., AVL-G and AVL-S. AVL-G is the technique when the additional sleep transistor is connected at the ground terminal, while AVL-S is the technique when the sleep transistor is connected to the supply.

![AVL Diagram](image)

Figure 4.5 AVL in VCO using Ring Oscillator

Both the techniques are being applied in the circuit to enhance the performance of the circuit. AVL-G leads to increase in ground level in the circuit when the circuit is in active mode. It leads to decrease in the leakage current when the circuit is in standby or cutoff mode. AVL-S technique helps in curtailing the gate leakage current in the circuit.
4.3 SIMULATION RESULT

The parameters calculated for the comparison of the various VCO circuit are:-

I. Efficiency
II. Voltage Gain
III. Delay
IV. Leakage Power
V. Oscillation Frequency
VI.

<table>
<thead>
<tr>
<th>S. No</th>
<th>Parameters</th>
<th>VCO circuit using CMOS</th>
<th>VCO circuit using FinFET</th>
<th>MTCMOS in VCO</th>
<th>SVL in VCO</th>
<th>AVL in VCO</th>
</tr>
</thead>
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<tr>
<td>1</td>
<td>Efficiency (%)</td>
<td>7.38</td>
<td>7.75</td>
<td>13.35</td>
<td>15.76</td>
<td>16.28</td>
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<td>2</td>
<td>Voltage Gain (dB)</td>
<td>0.198</td>
<td>0.493</td>
<td>0.690</td>
<td>0.691</td>
<td>0.695</td>
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<td>3</td>
<td>Delay (sec)</td>
<td>2.35e-8</td>
<td>5.177e-9</td>
<td>5.175e-9</td>
<td>5.165e-9</td>
<td>5.163e-9</td>
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<tr>
<td>4</td>
<td>Leakage Power (pW)</td>
<td>8.725</td>
<td>7.95</td>
<td>7.22</td>
<td>5.23</td>
<td>4.375</td>
</tr>
<tr>
<td>5</td>
<td>Oscillation Frequency</td>
<td>4255319.14</td>
<td>19316206.3</td>
<td>19323671.5</td>
<td>19361084.2</td>
<td>19368584.1</td>
</tr>
</tbody>
</table>

Table 4.1 Comparison Table of various parameter of VCO using Different Techniques

The comparison charts for the above parameters are shown in respective figures from Fig. 4.6 to 4.10 respectively.
Fig. 4.6 Comparison Chart of Efficiency

Fig. 4.7 Comparison Chart of Voltage Gain
Fig. 4.8 Comparison Chart of Propagation Delay

Fig. 4.9 Comparison Chart of Leakage Power
4.5 OUTPUT GRAPHS OBTAINED

A. The output of VCO is shown in Fig.4.11. The input supplied is in the form of voltage and output obtained is in the form of frequency.

B. Leakage Power graph in VCO is shown in Fig.4.12.
4.5 CONCLUSION

With the inclusion of the leakage reduction technique in the VCO circuit, a vast enhancement in the performance of the circuit is observed. A fineness in the output is observed when FinFET technology is used in place of CMOS. Using FinFET, MTCMOS, SVL and AVL efficiency in the circuit has increased drastically. The efficiency of the circuit changed from 7.38% to 7.75%, 13.35% 15.76 and 16.28% respectively. A relative increase in the voltage gain is also observed using the proposed design. A higher speed of operation is acquired in the circuit. It changed from 23.5 nsec in CMOS based to 5.163 nsec using AVL techniques respectively. Leakage power in the circuit has changed from 8.725 pW in CMOS based to 7.95pW, 7.22pW, 5.23pW and 4.375pW using FinFET, MTCMOS, SVL and AVL technique respectively. The oscillation frequency of the circuit has increased drastically from CMOS to FinFET to other techniques. A better performance in the circuit is acquired using AVL technique. A higher performance in the parameters like efficiency, voltage gain, delay, leakage power and frequency is observed.