CHAPTER 2
LITERATURE SURVEY

There are different design techniques to implement a digital logic circuit. In this regard many innovative designs for basic logic functions have appeared in the literature recently. This includes static CMOS, mirror image, CMOS transmission gates, pass transistor logic circuits: CPL and DPL [2].

Static CMOS circuits are based on duality principle in which p-block is obtained as the dual network of the n-block. Output is connected to ground through n-block and to $V_{DD}$ through dual p-block. In mirror image circuits, p-block is exactly mirror image of n-block which leads to a fully symmetric circuit topology and hence easy to design. CMOS transmission gates also known as CMOS pass gates consist of one pMOS and nMOS transistor, connected in parallel and complementary signals are applied to gate of both transistors. This transmission gate works as a bidirectional switch. The complexity of CMOS pass gate logics can be reduced by adopting CPL. It consists of purely nMOS transistors for logic operations. All inputs are applied in complementary form and output is also obtained in complementary form. The elimination of pMOS transistors gives rise to threshold voltage drop whenever high signal is passed from the nMOS. DPL is modified version of CPL for low voltage applications. Instead of using only nMOS both pMOS and nMOS are used. pMOS passes logic high signal whereas nMOS passes logic low signal in order to achieve full output swing. Thus, using both pMOS and nMOS reduces threshold voltage drop as well as power consumption.

The implementation of the full adders can be divided into several categories. The conventional design of 1-bit full adder circuit uses standard static CMOS and complementary pass transistor logic circuits.

In the last decade, some new designs and optimizations on full adder circuits for the deep submicron technology were reported. Based on this full adder has gone through
substantial improvement in power consumption, power-delay product, speed and area. Thus, these circuits have better performance than conventional designs. Starting with the conventional 28T full adder implemented using mirror technique and then gradually moving towards full adder consisting of as less as 8T, the study on adders can be summarized as follows:

In 1992, Zhuang and Wu [8] implemented the two different full adder circuits using transmission function theory. The full adders were designed with driving outputs and without driving outputs. These new circuits were compared with the two conventional designs of full adders based on transmission function and as a result four MOS transistors were saved.

In 1997, Zimmermann and Fichtner [9] compared full adder designed in complementary MOS logic and pass-transistor logic as shown in Fig. 2.1 and 2.2. Complementary CMOS, however, proves to be superior to CPL with respect to speed, area, power consumption, and power-delay products with only few exceptions. CPL was found to be the most efficient but CMOS to be 20% faster and superior to CPL. An implemented 32-bit adder using complementary CMOS has a power-delay product of less than half that of the CPL version. The paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits, if low
voltage, low power, and small power-delay products are of concern. Complementary static CMOS performs much better than CPL and other pass-transistor logic styles if low power is of concern.

In 1999, Vesterbacka [10] explained how XOR and XNOR circuits are used to realize a 1-bit full adder circuit based on transmission gates. A 6T CMOS XOR circuit that also produces a complementary XNOR output is introduced in the full adder. The resulting full adder circuit is realized using only 14T and compared with existing 16T full adder circuit [8]. Both circuits are shown in Fig. 2.3 and 2.4 respectively. Also the layout of 14T and 16T full adder cells have been designed and simulated for comparison. Both adders yield similar performance in terms of power consumption, propagation delay and power delay product, but 14T adder cell has the advantage of full voltage swing at all circuit nodes. The area is somewhat lower for the proposed adder on account of reduced device count. However, due to two feedback MOSFETs in the proposed adder that need to be ratioed, there is a higher cost in terms of design effort.
Afterwards in same year, Shalem, and John [11] proposed 10T static energy recovery full adder (SERF) shown in Fig. 2.5. It is based on energy recovering logic in the pursuit of energy efficient circuitry. Energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The power consumption and general characteristics of the SERF adder are then compared against other low power full adder cells proposed in past literature. The proposed SERF adder design was proven to be superior to other designs in terms of power consumption, area and propagation delay. It takes approximately 26% to 55% less energy than the other designs and is shown to be 19% faster.
Further in 2001, Radhakrishnan [12] presented a formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell that is fully compensated for threshold voltage drop in MOS transistors. This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. Also, a low transistor count full adder cell using this new XOR-XNOR cell was presented.

In 2002, Bui [13] proposed 10T full adder cells using new proposed XOR and XNOR gates. All new adder circuits showed low power consumption in different input conditions, high frequencies and loading conditions. It consumes on average 10% less power and has 90% higher speed compared with previous full adder circuits. It gave threshold degradation at output but can be used to build larger systems. The area can also significantly reduce for the larger systems built upon them.

In 2004, Jiang [14] proposed a novel multiplexer based 12T adder shown in Fig. 2.6. This circuit has reduced transition activity and charge recycling capability and has no direct connections to power supply which leads to reduction in power consumption. This circuit has more than 26% power savings over conventional 28T CMOS adder and 23% than 10T adders and 64% in speed improvement.

In 2005, Vasefi [15] proposed two designs of 10T adder as shown in Fig. 2.7 and one 12T full adder by adding two extra stack transistors to 10T adder. 10T adder suffers
from threshold loss while 12T eliminated this problem completely. The 10T adder achieved a 43.68% improvement in power consumption. Both proposed adders were further used to implement 4-bit RCA and 4x4 array multiplier. The schematic of 12T adder is shown in Fig. 2.8.

![12T Full adder](image1.png)

**Fig. 2.6 12T Full adder**

![10T Full adders](image2.png)

**Fig. 2.7 10T Full adders**

In 2006, Vigneswaran [16] proposed high speed 14T CMOS full adder cell shown in Fig. 2.3 and compared it against SERF 10T full adder of Fig. 2.5. The serious threshold loss of SERF adder was reduced to 50% by sacrificing the MOS Transistor count. It has also shown 45% improvement in speed and considerably less power consumption in order of micro watts.
Moving further in 2006, Saberkari and Shokouhi [17] proposed a novel design of a low power 1-bit full adder cell, where the GDI technique has been used for the simultaneous generation of XOR and XNOR functions. This new full adder circuit outstrips many latest designs in energy efficiency and has the lowest power-delay product over a wide range of voltages among several low-power adder cells of different CMOS logic styles but on the other side it has large area consisting of 26 MOSFETs.

In 2007, Lee [18] proposed four different types of 10T full adder using GDI design methodology shown below in Fig. 2.9. These different design architectures of full adder were based on 4T GDI XOR and XNOR gates. The proposed designs possess the advantage of flexibility, less transistor counts and improved power consumption as well as delay making it a better alternative.

While entering in the year 2008 Navi and Kavehei [19] proposed a new low power and high performance adder cell using a new design style called “Bridge”. The bridge design style enjoys a high degree of regularity, higher density than conventional CMOS design style as well as lower power consumption, by using some transistors, named bridge transistors. Simulation results illustrate the superiority of the resulting proposed adder against conventional CMOS 1-bit full-adder in terms of power, delay and PDP.

Further in the same year, Chowdhury [20] proposed 8T full adder using novel 3T XOR gate combining complementary CMOS with pass transistor logic shown in Fig.
2.10. It showed significant improvement in silicon area but power consumption is slightly more than that of 10T full adder but it has a much less delay and much less power-delay product than its peer designs. The layout of the proposed full adder has also been designed and gives better performance than most of the adders mentioned in the literature so far as the power-delay product is concerned.

In 2009, Hosseinghadiry [21] proposed 10T and 9T full adders using 4T XNOR and 3T XOR gates respectively and evaluated its performance with respect to 12T circuit. 10T circuit shown in Fig. 2.9 (b) has threshold loss problem due to degraded XNOR output and output multiplexers. 9T adder shown below in Fig. 2.11 showed 24% improvement in term of power consumption and has better PDP for different operating voltages as well as frequencies but 10T adder is 12% faster than earlier reported full adder cells.

Fig. 2.9 10T Full adders using GDI Structure

In 2010, Sharma [22] did modification by changing aspect ratios of the transistors of earlier proposed 8T adder shown in Fig. 2.10. By reducing the transistor size the
threshold loss remains the same while reducing the power consumption. This effort results into low power adder design.

In 2011, Mishra [23] implemented two 9T full adder circuits to overcome the double threshold loss problem, driving capabilities in cascaded operations and low speed of operation. The implemented circuit required either 3T XOR circuit or 3T XNOR circuit, an inverter circuit and 2-to-1 multiplexer. This new design encounters only one threshold voltage loss. It consumes 6% to 67% less power and overall PDP for both the proposed circuit have been improved by 52% to 72% and 72% to 82% when compared with the various reported full adder circuits. Both proposed circuits are shown below in Fig. 2.12
Further in 2011, Sinha [24] proposed 9T full adder circuit shown in Fig. 2.13. This circuit has eliminated serious threshold problem in 8T adder due to simultaneous enabling of two transistors by adding an extra transistor and gives full voltage swing at low supply voltage. The circuit shows improvement in power, delay and power-delay product with varying operating voltages, frequencies under different temperature ranges.

Afterwards in the same year Kumar [25] implemented a new low power XNOR gate with three transistors. On comparison with earlier reported XNOR gates, this proposed circuit showed less power consumption and better output signal levels with reduce transistor count. A single bit full adder with 8 transistors based on proposed XNOR gate has also been presented and compared with high transistor count adder...
circuits. As a result it outperforms the previously reported circuits in terms of power consumption with less number of transistors.

Recently in 2012, Bazzazi [26] proposed low power and high performance 1-bit full adder cell using 3T XOR gate already designed by Chowdhury [20] but with some modifications. In this paper authors have changed the substrate biasing of MOSFETs in order to achieve low power consumption and hence reduced Power-delay product.

Concisely, the above discussion on literature reveals that all the modifications and size shrinking of single bit full adders are done to improve the power consumption of the cell so that it can be better useful for portable applications.

There are three major sources of power consumption in digital CMOS circuits [1] - [6] and [27], which are summarized in the Eq. (2.1) given below:

\[
P_{\text{total}} = \alpha C_l V_{\text{DD}}^2 f_{\text{clk}} + I_{\text{sc}}V_{\text{DD}} + I_{\text{leakage}}V_{\text{DD}}
\]  

(2.1)

The first term represents the switching component of power, where \( \alpha \) is the switching factor, \( C_l \) is the load capacitance, \( f_{\text{clk}} \) is the clock frequency. In most cases, the voltage swing is the same as the supply voltage \( V_{\text{DD}} \), however in some logic circuits, such as in single-gate pass transistor implementations, the voltage swing on some internal nodes may be slightly less. The second term is due to direct path short circuit current \( I \), which arises when both nMOS and pMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current \( I \), which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. The dominant term in a well-designed circuit is the switching component, and low power design thus becomes the task of minimizing \( C_l \), \( V_{\text{DD}} \), and \( f_{\text{clk}} \), while retaining the required functionality.

The power-delay product can be interpreted as the amount of energy expended in each switching event (or transition) and is thus particularly useful in comparing the power consumption of various circuit styles. If it is assumed that only the switching component of the power consumption is important, then it is given by following equation:

\[
\text{Energy per transition} = P_{\text{total}} / f_{\text{clk}} = C_l V_{\text{DD}}^2
\]  

(2.2)

Where \( C_l \) is the load capacitance being switched to perform the computation.

Therefore for low power what we have to look out for is the switching power
consumption and techniques to reduce switching power consumption. Some general logic style requirements for low power circuit implementation are as follows:

- **Clock frequency reduction**

  Reducing the clock frequency is not as beneficial as reducing the supply voltage. However, many processors of today have different power-down modes where the clock signal is silenced to blocks of the application that are not used at the moment. This is referred to as clock gating. Clock gating can in most cases be used in conjunction with other low-power techniques.

- **Switched capacitance reduction**

  Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible, and by reducing transistor sizes to a minimum. In particular, the number of (high capacitive) inter-cell connections and their length (influenced by the circuit size) should be kept minimal. Transistor downsizing is an effective way to reduce switched capacitance of logic gates on noncritical signal paths. For that purpose, a logic style should be robust against transistor downsizing, i.e., correct functioning of logic gates with minimal or near-minimal transistor sizes must be guaranteed.

- **Supply voltage reduction**

  Reducing the supply voltage is an attractive solution to reduce the power consumption since both the switched and the short-circuit power consumption have a strong $V_{DD}$ dependence. There are however some drawbacks with this method:

  - A lower $V_{DD}$ causes longer delays.
  - There is an overhead in generating another lower $V_{DD}$ on chip.
  - The supply voltage in state-of-the-art processes is already very low, which does not leave much margin to play with.

  A delay penalty can be mitigated by reducing the threshold voltage but then the subthreshold leakage will increase exponentially.

  The supply voltage and the choice of logic style are indirectly related through delay-driven voltage scaling [28]. That is, a logic style providing fast logic gates to speed up
critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction, i.e., performance and correct functioning of gates must be guaranteed at low voltages as well. This becomes a severe problem at very low voltages of around 1 V and lower, where noise margins become critical.

**Switching activity reduction**

Switching activity of a circuit is predominantly controlled at the architectural and registers transfer level (RTL). At the circuit level, large differences are primarily observed between static and dynamic logic styles. On the other hand, only minor transition activity variations are observed among different static logic styles and among logic gates of different complexity, also if glitching is concerned. To reduce the power consumption Gray code can be one solution since in this code only flip one bit between consecutive numbers. Activity-based decomposition is another activity-based reduction technique [29].

**Short-circuit current reduction:**

Short-circuit may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better) and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (10–30%), except for very low voltages. A low power logic style should have minimal short-circuit currents and of course, no static currents besides the inherent CMOS leakage currents.