CONCLUSION

The multilevel 2-D DWT is widely used in image compression and image coding for multimedia applications. Area-delay efficient hardware realization of the multilevel 2-D DWT has great practical interest for low-power resource constrained mobile and portable devices. Multilevel 2-D DWT computation can be performed using PA, RPA or folded scheme. Due to design simplicity, maximum HUE and lower arithmetic resource requirement, folded scheme is more popular than the PA and RPA for hardware realization. Keeping this in view, several VLSI architectures have been suggested in the last decade for efficient implementation of folded 2-D DWT. The hardware complexity of folded 2-D DWT structure is broadly divided into two parts (i) arithmetic and (ii) memory. In Chapter 2, hardware complexity of existing folded 2-D DWT structures is analyzed to explore an appropriate design strategy to derive an area-delay efficient hardware structure. From the complexity analysis, it is found that memory complexity is almost 97% of the overall hardware complexity of folded 2-D DWT structure, where arithmetic complexity is only 3%. However, the most of the existing design strategies are focused on optimization of arithmetic complexity, reduction of cycle period and to increase throughput. There is no significant effort is made for optimizing memory complexity which is a major component of a multilevel folded 2-D DWT structure. From the complexity analysis we propose a design outline to derive an area-delay efficient hardware design for 2-D DWT. The proposed design outline is (i) priority must be given for memory complexity optimization over the arithmetic complexity optimization or reduction of cycle period and (ii) memory utilization efficiency to be considered ahead of memory reduction due to design complexity of memory optimization method. Based on the proposed design outline four separate design approaches and concurrent architectures are presented in this thesis for area-delay and power efficient realization of multilevel 2-D DWT.

In Chapter 3, a block processing scheme is proposed to improve the on-chip memory and frame buffer utilization efficiency of line-based folded 2-D DWT structure. Using this block processing scheme, a line-based parallel and pipeline structure is derived. A frame buffer design is also presented in this Chapter using single-port RAM to support data flow requirement of the proposed block processing scheme. The proposed line-based block processing structure involves nearly the same amount of on-chip memory words and same frame buffer words as the existing folded structures, but it provides $P$ times higher
throughput, where $P$ is the input block size. The structure easily configured for different block size. Since, on-chip memory and frame buffer size does not increases with the block size, the proposed structure offers better memory utilization for higher block sizes and it has less ADP and EPI.

In order to reduce the size of the transposition memory of folded 2-D DWT structure given in Chapter 3, a new data access scheme is presented in Chapter 4. Based on the new data access scheme area-delay efficient structure for folded 2-D DWT is derived. In this Chapter, a frame buffer design is also presented using single-port RAM to support data flow requirement of the new data access scheme. The proposed structure involves transposition memory of size $N$ words which is the lowest in size so far achieved in all the existing designs. The structure is regular, modular, involves less on-chip memory words than the line-based structure of Chapter 3, and it does not required any control circuitry. Due to these features, ADP of the proposed structure is significantly less than the line-based structure of Chapter 3. However, this structure requires a specially designed input buffer to feed the input blocks based on new data access scheme.

Both the folded structures presented in Chapter 3 and Chapter 4 involve frame buffer to perform multilevel 2-D DWT computation. On-chip implementation of frame buffer is a major design problem due to its large size where off-chip implementation degrades the speed and power performance of the 2-D DWT structure. To overcome this problem, recently parallel structures have been suggested for multilevel 2-D DWT without using frame buffer. It is found that, the existing parallel structures are not efficient due to some inherent design problems. To overcome these problems, block processing scheme is presented in Chapter 5 for generating continuous input blocks for the succeeding PUs of the parallel structure to achieve 100% HUE without any block folding and introduces embedded down sampling without time-multiplexing the intermediate components. Embedded down sampling and continuous generation of scaled data blocks make the parallel design simple with a regular data flow. Using the proposed block processing scheme, two separate parallel structures (PAR-1 and PAR-2) for parallel computation of multilevel lifting 2-D DWT are derived. Both these parallel structures are highly regular, modular and do not require any interfacing unit between DWT levels or overlapping memory unlike the existing parallel structures. Both these parallel structures have same arithmetic and time complexity, but the PAR-2 requires nearly $(3N/2^{J})$ less on-chip memory words than the PAR-1. PAR-1 and PAR-2 do not
required frame buffer unlike the folded structures presented in Chapter 3 and Chapter 4. However, PAR-1 and PAR-2 involve slightly higher core area than the folded structures of Chapter 3 and Chapter 4. But they involve significantly less computation time than the folded structures. Due to less memory complexity, ADP and EPI of the proposed folded and the parallel structures are significantly less than the similar existing structures. The memory utilization efficiency of the proposed structures increases for higher block sizes. Consequently, the ADP and EPI of the proposed folded and parallel structures reduce for higher block sizes.

Since, both the parallel and folded block-based 2-D DWT structures involve large number of arithmetic component (multiplier and adder). The arithmetic complexity of a block-based structure increases proportionately with the block size. Multiplier is more complex than the adder and it consumes a major part of the arithmetic core area and power. Keeping these facts in mind, an efficient multiplierless 1-D DWT structure based on DA is presented in Chapter 6. CSFA and CSAC are used to improve the performance of DA-based 1-D DWT structure. The proposed DA-based 1-D DWT structure involves significantly less logic resources and it has less bit cycle period than the existing similar DA-based structure. The proposed DA-based 1-D DWT structure is used to construct 2-D DWT structures based on the line-based and parallel data access scheme. Both the DA-based 2-D DWT structures involve same logic resources but they differ with on-chip memory size and frame buffer size. The DA-based architecture based on parallel data access scheme involves a small size core and it is suitable for low complexity realization.

The proposed parallel and folded architectures are individually best amongst the existing structures. These designs have specific features like throughput scalability, memory efficiency, higher memory utilization efficiency and regular data flow. These features are very useful for hardware implementation of 2-D DWT structure to meet area, speed and power requirement of different image processing applications. However, proposed structures have few shortcomings like critical path delay, fixed point error, and interconnect delay which could be further investigated to reduce the area-delay-power of the 2-D DWT structures. These issues will be addressed in the future work.