CHAPTER 2

LITERATURE REVIEW

Faster growth in electronic industries introduced a technology called FPGA. It is flexible and reconfigurable. It helps to reduce the design time. The basic idea of the research work is to find a better alternative to PLC using FPGA. As it is known that the PLC has analog and digital input / output modules, this chapter reviews the earlier research works carried out by several researchers.

i) Review on the design of multi-channel ADC using processor or FPGA – AIM.

ii) Review on the design of single or multiple PID controller (Processor based or FPGA based) – AOM.

iii) Review on the issues related to ladder programming and its conversion into HDL codes.

2.1 ANALOG INPUT MODULE – AIM

Conventional AIM has multiplexer type ADC along with a processor and RAM. At a time, only one signal will be considered for conversion. The turn of next conversion for the same signal depends on the total number of signals connected to the multiplexer. Hence the scan time of an analog signal is not fixed. Multi-channel ADCs designed for different applications are reviewed in this section.
Tan et al (2013) have experimented the evaluation of gamma-ray spectroscopic performance of multi-channel ADCs including their energy resolution, nonlinearity and timing resolution. It is proved that multi-channel ADCs are suitable for gamma-ray spectroscopic measurement. Digital processing components such as ADC, DAC, DSP and FPGA are able to meet the need of improved time, position and energy resolution in nuclear physics experiments. AD9222, ADS6425 and AFE5801 multi-channel ADCs are chosen for the purpose of evaluation. Performance of these multi-channel ADCs has been compared with the single channel ADC, AD9432 which were already proved for spectroscopic performance. A new daughter board shown in Figure 2.1 was built to evaluate two of the multi-channel ADCs AD9222 and ADS6425.

![Figure 2.1 Block diagram of the prototype board HDDB (Tan et al 2013)](image-url)
Due to board space limitation, only two channels of the AD9222 and ADS6425 are connected to analog inputs from the front panel connectors. Outputs of multi-channel ADCs are serial. FPGA processed these outputs for pulse detection and waveform capture. Each of the captured waveforms has 16,384 samples and they are stored in high density daughter board (HDDB) FPGA board. Then, it was transformed into Synchronous Dynamic RAM (SDRAM). A host software reads these data and stores in hard drives. These waveforms can be processed offline to characterize the timing, energy resolutions and nonlinearities of these ADCs. It is concluded that multi-channel ADCs AD9222 and ADS6425 showed excellent energy resolution. ADS6425 showed best integral linearity. Excellent timing resolution was measured with all four ADCs.

Atalik et al (2012) have proposed a digital controller developed using multiple DSP and FPGA boards for parallel operated Cascaded Multilevel Converter (CMC) which is used in Flexible AC Transmission System (FACTS) applications. A DSP acts as a master controller. Multiple DSP boards, FPGA boards and microcontrollers were connected as slave devices. An industrial computer can communicate to all these devices in addition to the peripheral devices. Intercommunication among all these devices was established mainly through fibre optic link. The entire system was implemented on a sample 11 level, CMC based 154kV, + / –50-MVAr Transmission type Static Synchronous Compensator (T-STATCOM). The controller was able to provide good transient response and steady-state characteristics for the overall system including protection and monitoring functions. Transmission and distribution system has high voltage and high power converters. It includes a multilevel converter topologies which necessitates the use of parallel processing techniques in the control loops. This is possible by implementing a digital control technique with the help of DSP and FPGA. This CMC-based T-STATCOM acts as a FACTS device.
which is shown in Figure 2.2. It can be operated in one or more than one of the following modes.

i) Reactive power compensation.

ii) Terminal voltage regulation.

iii) Power system stability improvement such as inter-area oscillation damping.

![Diagram](image-url)

**Figure 2.2** Line diagram of 'm' parallel operated CMCs T-STATCOM (Atalik et al 2012)

Each CMC is connected to the medium voltage side of the coupling transformer through a series filter reactor. All the CMCs are charged by DC-link capacitors in a preprogrammed manner. The major functions of the control system are:
i) Waveform synthesizing,
ii) Closed loop control,
iii) Protection,
iv) Built-in monitoring and
v) Remote monitoring and control.

The control system uses the topology of a DSP-based master controller in combination with 'm' pairs of FPGA and slave DSP boards. 5 paralleled CMCs is considered for this FACTS application. It can control reactive power in the range of + 50MVAr to – 50MVAr. Intercommunication among CMCs is established through fibre optic cable. In this sample system, all the necessary calculations are completed in 40µs. It has 17 word data which includes modulation indices, phase angles, line current directions, DC-link capacitor reference voltage, PI coefficients and checksum words. DSP boards require 20µs time period to transfer these data to FPGA boards. Hence the total time delay in control action was 60µs. The master DSP board has two chips. One chip controls the functions and serial communication with PLC and two slave DSP boards. Another chip is used to establish protection for under / over frequency and communication with the remaining three slave DSP boards. Major functions of the master DSP board are listed below:

i. Master DSP board receives start command from the industrial computer through the PLC. It activates slave DSP boards to start the first phase of the DC-link capacitors, pre-charge period. The second phase of the pre-charge starts after the completion of this. After the completion of the second phase, the master DSP commands the PLC to by-pass the pre-charge resistor.
ii. Master DSP activates any one of the mode, reactive power compensation or terminal voltage regulation set by the operator.

iii. The master DSP continuously refreshes and updates the CMCs.

iv. The master DSP board establishes some protective actions on both FACTS device and CMC unit based on the details it receives from PLC, slave DSPs and FPGAs.

v. When the operator issues the stop command, the master DSP turns off IGBTs by communicating to FPGA through the slave DSPs.

vi. The master DSP continuously checks the validity of fiber-optic links in the PLC and the slave DSPs.

The major functions of the slave DSP are listed below:

i. Every slave DSP board generates three PLL signals for each line-neutral voltage. This is necessary to synchronize every CMC with the supply voltage at Point of Common Coupling (PCC).

ii. Slave DSP boards sample line current waveforms, decide whether the current is greater than zero or not and send a pulse train to the FPGA board through Serial Peripheral Interface (SPI) communication link.

iii. Each slave DSP board computes active and reactive powers, \( P, Q, \text{rms} \) values of AC quantities, \( V, I \) for the associated CMC and sends these signals to industrial computer for monitoring.
iv. Slave DSP boards take care of over / under voltage and unbalanced protection functions for the CMC units.

v. Slave DSP boards continuously verify the fiber optic link connected to the FPGA board and the master DSP board.

FPGA board has an FPGA chip, multiplexer circuit, fiber optic transmitters / receivers and other peripheral devices. The functions performed by FPGA board are described below:

i. FPGA board ensures that the load angle value is under control. This is used to maintain the active power flow under control.

ii. Optimum angles are calculated off-line using a hybrid algorithm and it is stored in FPGA memory. FPGA board extracts optimum angles once in $40 \mu s$ using the modulation index that is sent by the slave DSP and implements them using the shifted Phase Locked Loop (PLL) signal.

iii. FPGA receives the DC-link capacitor voltages and determines the voltage level using a shifted PLL signal whenever a selective swapping is needed.

iv. FPGA board changes the IGBT status based on the request from the master DSP board. Charging of DC-link capacitors in the first and the second phases of pre-charging period is done through IGBT.

v. PLC establishes discharging of DC-link capacitors in DC_PD boards through FPGA board. FPGA board also communicates the status of discharging to the PLC.

vi. FPGA board verifies the fiber optic connection with the slave DSP board.
PLC establishes control actions based on the signals it has received from the master DSP boards, digital / analog I/Os. Major functions performed by the PLC are listed below:

i. Based on the protection signals received from the de-ionized water cooling system, the PLC commands the FACTS device to change the status of circuit breakers and the load break switch.

ii. The PLC maintains interior temperature of CMCs and acts as a PI controller also.

iii. PLC transfers the fault / failure signals received from the control system elements to the industrial computer.

The result of digital implementation of active power controller proves that the Modified Selective Swapping (MSS) method has yielded a perfect equalization of DC-link capacitor voltages. The performance of digitally implemented Q controller and the associated PI settings are found to be satisfactory in transmission system applications for reactive power compensation or terminal voltage regulation modes.

Abdallah et al (2011) have developed a multichannel data acquisition system using a system on chip and FPGA. The following features are incorporated in the design:

i) The design has been developed for medical applications,

ii) Simultaneous data acquisition, cost, power consumption and hardware scalability and

iii) A dedicated display to display the signals acquired in a suitable form.
DAQ system can be established using a microprocessor or microcontroller or FPGA. Microcontroller or microprocessor-based DAQ system has the drawback of fixed architecture, high cost and high power consumption. FPGA-based DAQ system is flexible as it is reconfigurable. It satisfies the basic requirements of a DAQ system like storage capacity, input and output options. FPGA-based stand alone DAQ system can also perform the functions listed below:

i) Accepts different types of sensor signals as inputs simultaneously,

ii) Stores the acquired signals in memory without the help of a computer. A network control module (NCM) is able to transmit the acquired signals through internet,

iii) Performs digital signal processing functions like FFT and DCT and

iv) Performs adaptive scheduling for multiplexed ADC interface.

Use of a high speed ADC with a high speed analog multiplexer can eliminate the problem of hardware redundancy. Transient effects of switching input channels by the multiplexer can be removed by using bandpass or high pass filters. The conceptual design of Universal Host Interface Module (UHIM) developed by Abdallah et al (2011) is reproduced in Figure 2.3. Bridging block acts as a multipurpose electronic interface and acquires different types of input signals. It has electric circuits to match the output impedance of the sensor with the input impedance of the analog filter bank. FPGA has optimal ADC scheduler to manage the variable switching time of the ADC multiplexer. This ensures that large number of channels can be sampled without loss of signal quality.
Real-time Archiving and Monitoring Module (RAMM) has been designed to provide visual monitoring of the acquired data. It is capable of interfacing with LCD to plot continuously the time varying signals. An on-chip hardware reconfigurable NCM has also been developed and incorporated in FPGA to transfer the acquired data for remote control applications. The design of RAMM and NCM developed by Abdallah et al (2011) is shown in Figure 2.4.

It transmits the stored data in a secured manner through the internet with a minimal hardware interface. It eliminates the need for external network interface card. To establish secured communication with the internet, the FPGA forms network packets so that it has data identification numbers and
the collected data. NCM supports different types of data records. When the acquired data are stored in memory, a unique identifier has been built for different types of sensors. Simultaneous acquisition of signals is achieved by following proper time scheduling. Let 'n' be the number of samples per time slot, 'S', be the number of time slots that are assigned for channel, 't_{sa}' be the sample acquisition time and 'T' be the elapsed time. Data acquisition starts from the first channel with the help of analog multiplexer, and the last channel data will be acquired before the elapsed time. Acquired data will be temporarily stored in FPGA buffers.

![Conceptual design of RAMM and NCM](image)

**Figure 2.4 Conceptual design of RAMM and NCM (Abdallah et al 2011)**

RAMM module transfers these data into the flash memory card with minimal interface. Multiple-block write approach is used to write data into the flash memory. RTOS is not used in the design for displaying acquired data in the LCM. Display has been designed using FPGA hardware alone and
no software driver is used. The intention of the display is to monitor the acquired signals. The input range of analog signal for acquisition is fixed as $-1.25V$ to $+1.25V$. A signal generator is used to generate sine waves in the frequency values of 1, 4, 8 and $10kHz$ as four inputs to the DAQ system respectively. ADS7891 ADC chip is used to convert analog signal into digital signal. An operational amplifier is used to increase the analog input range as $-1.25V$ to $+1.25V$ from $-0.2V$ to $+0.2V$. The NI test bench, PCI 6024E 200-kS/s 16-channel DAQ card is used to verify and validate the concept. Cyclone II FPGA with a main clock frequency of $50MHz$ is used to establish UHIM and NCM modules. This design can be used in areas like wideband communications, medical, environmental and radar applications.

Monmasson et al (2011) have discussed the use of FPGAs in industrial control applications along with FPGA-based sensorless motor controller, artificial intelligent-based industrial controllers and case studies. Microcontrollers and DSPs are the two major devices that are used for the implementation of industrial control system applications. The main drawback of these two devices is the level of parallelism that can be established to execute a specific algorithm. This creates an impact on the performance of the device in terms of throughputs and achievable bandwidth. The alternative for these two devices is found to be FPGA. High level of parallelism can be achieved from FPGA since the entire algorithm execution is based on its hardware architecture. The main reasons for choosing FPGA is listed below:

i. FPGA is a reconfigurable device.

ii. It has high potential of parallelism in logic execution.

iii. It is possible to establish real-time control loop with a sampling frequency of above one $MHz$. 
iv. It is best suited for high speed applications because of its parallel execution of an algorithm.

v. Its density keeps on increasing along with its high degree of flexibility; designers use it for larger range of industrial control applications.

vi. It supports various communication protocols like Ethernet, USB, CAN, PCI and SPI.

Monmasson et al (2011) have developed an FPGA-based sensorless motor controller for synchronous motor based on an Extended Kalman Filter- (EKF). Figure 2.5 shows the control system implemented in FPGA.

![FPGA implementation of sensorless control system](image)

**Figure 2.5** FPGA implementation of sensorless control system (Monmasson et al 2011)

The hardware specifications define the sensors, digital control unit and ADC interfaces. The controlled AC drive has a synchronous motor fed by
a voltage source inverter (VSI). An EKF-based algorithm (Bolognani et al 2003) estimates the rotor position and speed. PI controller calculates the d-q voltage references according to the measured and reference currents. Three-phase voltage references are processed after a co-ordinate transformation. Carrier-based pulse width modulation generates the PWM signal for the VSI. The speed control was achieved using a P-PI regulator (Naouar et al 2008). A hysteresis controller and a buck converter is implemented to maintain the rotor current equivalent to a constant value (Naouar et al 2007). The voltage interface aims to generate the three-phase stator voltages after a multiplication of the per-unit voltages by the measured DC-link voltage. The design is optimized in terms of algorithm used for control and the hardware required to accommodate the algorithm. FPGA optimization is realized using Algorithm Architecture Adequation (A³) technology. It helps to establish maximum number of operations using minimum number of operators. VHDL code for the design is synthesized using various FPGAs like SPARTAN3E, SPARTAN6, VIRTEX2P and VIRTEX6. The total execution time is found to be 6µs. For the purpose of comparison, the same sensorless controller is implemented in the software based on the synthesizable MicroBlaze processor core and a TI TMSF2808 DSP device.

Monmasson et al (2011) have also discussed a case study named as FPGA neural network-based electronic nose. This particular case study shows an Artificial Neural Network (ANN) used as a pattern recognition module in an artificial olfaction system (Tisan et al 2010). The olfactory system, developed using ANN has

i. Seven gas sensors chosen to react to a wide spectrum of odors

ii. Temperature sensor
*iii. Humidity sensor*

*iv. Test chamber*

*v. Three pumps to carry gas*

*vi. Circuits for signal conditioning and pumps command*

*vii. Data acquisition board*

*viii. Pattern recognizing module hardware, implemented in FPGA*

*ix. User interface developed using LabVIEW*

The data acquisition module has been created to acquire data generated by all the sensors, preprocess the signals acquired and save data in a text file format. Hence the virtual instrument (VI) designed using LabVIEW has pumps control module, data acquisition control module, sub-Vis control time module, preprocessing signal module, C grade conversion module of the signal generated by the temperature sensor and %RH conversion module of the signal generated by the humidity sensor.

Costas-Perez et al (2008) have designed an educational laboratory which is implemented for the purpose of practical education in sensors, data acquisition and basic control skills. It is optimized for remote access of the laboratory infrastructure. It is identified that the combination of reconfigurable hardware and virtual instruments have significant advantages to implement a friendly, robust and adaptive educational framework for the students. Virtual instrumentation has been the best choice for data acquisition. It also supports the web-based educational tools. The proposed approach includes the features of learning management systems such as dynamic access to learning units. LabVIEW, the product of National Instruments, has been a well-known professional tool for data acquisition (Mohanty & Kar 2006) and implementation of control algorithms (Koutroulis & Kalaitzakis 2006).
Figure 2.6 indicates the establishment of a control system and a monitoring scheme for a physical process. The laboratory is set up with the temperature sensors, level sensors, flow sensors, pressure sensors, current sensors, speed and position sensors with different scale models to measure the physical quantities.

Different types of sensors are provided so that the students can choose the required sensor by referring to the specifications in the data sheet. This makes the students become familiar with the characteristics of commercial sensors. The next stage is the signal conditioning. A predefined general purpose circuit is provided with an instrumentation amplifier, zero adjusting circuit, two independent second order low pass active filter stages, voltage reference with temperature compensation and a voltage to current converter. Three types of operators help the students to verify the characteristics and the operation of sensors. An NI USB-6009 module connected through a universal serial bus port to a computer acquires the
analog signals from the signal conditioning circuit. Students can develop their own LabVIEW application using the sensors.

Perelman & Ginosar (2007) have developed a prototype for multichannel neuronal recording. Neuronal recording devices are useful to carry over the neurophysiological research (Black et al 2003). It is possible to extract the significant features of the neuronal signals using the wavelet transform method (Oweiss et al 2005). Power consumption of the system can be reduced when this algorithm is used in VLSI technology (Zviagintsev et al 2005). An integrated wireless recording device is able to acquire neuronal activity over a large number of channels and communicate the data over a bi-directional wireless link. The integrated circuit is fabricated in 0.35μm standard CMOS process. It can acquire neuronal signals from 12 true differential recording channels. The entire data acquisition process for neuronal recording is shown in Figure 2.7.

![Figure 2.7 Chip architecture of data acquisition system (Perelman & Ginosar 2007)]
This on-chip controller is responsible for host communication, chip timing, internal register access, channel readout and spike detection. The controller operates in either of the two modes, namely programming or streaming. In the streaming mode, neuronal signals are read from the ADCs and transferred to the host. The chip communication is established through a five wire, full duplex, bit serial synchronous bus. FPGA is used as an interface to establish the communication, and hence data transfer among the host computer and the neuronal recording device. It uses an Altera Cyclone II FPGA device and an integrated ethernet physical interface. The Altera Nios II embedded processor executes the real-time operating system to handle the neuronal data stream. The top level Java GUI module is for data display and system control.

Thomas et al (2000) have developed an embedded system-based data acquisition system. Conventional data acquisition system uses a multiplexer to acquire data from different sensors. It is used in between the sensors and a processor. The software part activates the processor to activate the multiplexer to select a specific channel to read the data and then moves to the next channel to read the data. It repeats the procedure till the data in all the channels are read out. This work helps to realize a certain software function in FPGA. The existing method uses the following steps to establish analog data acquisition system:

i. Processor releases address to analog multiplexer to select a channel.

ii. Ensures that the data in the input side of the multiplexer is transferred to its output.

iii. Samples the analog signal using sample and hold circuit.
iv. The processor sends start conversion pulse to the ADC and reads the end of conversion pulse from it.

v. The processor reads the digital output data.

Let the total time required to acquire one analog signal using the above procedure be \( t_a \). Therefore, the time required to acquire 'n' analog signals will be \( (n \times t_a) \). This can be reduced by using high speed devices. However, the software code remains the same. Similarly, digital data acquisition also consumes time to acquire one digital data. It gets multiplied with respect to the number of digital signals to be read. Digital multiplexer is used for this kind of data acquisition. It is understood that the use of multiplexer for analog or digital data acquisition increases acquisition time along with the increase in the number of channels.

The design proposed by Thomas et al (2000) first acquires and stores the signals in latches. Then the processor reads all the data in a single clock pulse. In the case of analog data acquisition system, all the analog signals are read one by one and stored in latches. Control logic for channel selection, latch selection to store data is designed using FPGA. Now, the data acquisition is stopped and the processor reads the data from the latches one by one. In digital data acquisition system, serial to parallel converter, latches and control logic circuit are designed by FPGA. This is adopted with the same procedure used for analog data acquisition. As a whole, this work has shifted the role of control logic performed by processor to FPGA. Since FPGA has the property of parallelism, data acquisition time is reduced.

2.2 ANALOG OUTPUT MODULE – AOM

Fernandez et al (2012) have proposed a composition control and inventory control for a continuous ethanol – water non-linear pilot distillation column monitored using LabVIEW. Neural network model is the best choice
to develop the model for a process condition when the clear knowledge about process condition is unknown (Haykin 2008). Distillation has been the important separation technique of any chemical process industry.

Challenges in modeling and control of distillation process are non-linearity, multivariable and non-stationary processes subjected to constraints and disturbances (Skogestad 2007). LabVIEW is used for the purpose of monitoring distillation column since it facilitates instrumentation control, data acquisition control and its analysis. It can directly interface to sensors and actuators (Bishop 2004). Adaptive neural networks are used to predict product composition, establish dual control of distillate and bottom composition and have inventory control for a continuous ethanol – water non-linear pilot distillation column. The pilot distillation column is composed of nine plates and distributed into three sections: water-refrigerated tubular condenser, heated electric boiler coupled with a personal computer to evaluate the performance of both the soft sensor estimation, identification and the control task. The distillation unit has temperature sensors, differential pressure sensors, flow meters, plant actuators for flow, temperature and level control as in Figure 2.8. The whole system is connected to the neural controller through PCI and USB buses. All the instruments are monitored using LabVIEW. The control system has been developed using a neural network model of the process. Genetic algorithm is used to establish the control scheme which determines and monitors the composition of light and heavy components from secondary variable measurements. The neural network composition estimator derives the concentrations in the distillate and bottom stream from the secondary variable measurements. The controller response is based on the dynamic system modeled by a neural network. The final product specification is based on the composition control. Composition values for control are derived from the secondary variables. This approach is defined as a software sensor (Brosilow & Joseph 2002). Thus, derived inferential system has increasing
computation time in line with the increase in the number of variables. Neural networks can be used to infer the composition from the secondary variables as it is termed as a universal approximator (Haykin 2008).

Figure 2.8 Distillation unit setup (Fernandez et al 2012)

A multivariate statistical technique based on the Principal component analysis (PCA) methodology is used to select the secondary variables suitable for composition control (Zamprogna et al 2001). Four
secondary variables are identified as inputs to the neural estimation network. They are, reflux, top and bottom temperatures and differential pressure drop. Since the controlled variables cannot be directly measured, the product levels are fixed as the output of neural model. The front panel developed using LabVIEW provides the possibility of defining the internal configuration structure of neural network. GA is used for optimization. The network model relates the past states, current states and the control inputs with the available future outputs. The neural network model makes use of neural composition estimator to derive the neurogenetic controller. The neurogenetic controller is compared with a PID control to validate the proposed control scheme. Four decoupled PID controllers are used for comparison. The composition set points of top-bottom purity and top-bottom product levels are changed to identify the performance of both the neurogenetic and PID controllers. The PID controller performance has a greater settling time, overshoot and poor response to changes in the targets. The neurogenetic controller is able to reach the required references with slow response time. The integral square error (ISE) values of neurogenetic controller are lower when compared with those of the PID controller.

Carlos et al (2011) have designed and implemented a data acquisition and speed control action using vector controlled method for a three phase induction motor. Data acquisition is established under LabVIEW environment. Control actions on energy usage in the power stage and tracking of the reference at low and high speed are executed through a DSP processor. Three-phase induction motors are widely used in both homes and industries. These motors have the drawback of complexities in controlling their speed and torque (Veerachary 2002). The field-oriented control (FOC) method is used to achieve control on torque and speed (Santisteban 2001; Rodriguez et al 2011). The coincidence of real axis with the rotor flux vector is considered as a reference frame. This frame helps to control the flux and the
torque. The use of PI controller helps to establish control action and maintain the motor speed at the desired value and this is shown in Figure 2.9.

Three-phase current measurements using current transducers, phase voltage measurement from the PWM signals generated by the DSP processor are done to compute the current and voltage model. Current measurement will help to calculate the fluxes in stator and rotor (Veerachary 2002) which in turn indicates the motor speed and torque. The time frame is obtained from the three axes of currents or voltages using linear transforms. Park transformation helps to modify this two-phase orthogonal system into a rotating reference frame. This transformation can rotate with the angular velocity. Motor speed is calculated based on the calculation of \( \sin \theta \) and \( \cos \theta \) which is available in the transformation. A look-up table in the DSP processor is referred to for calculation. DSP processor generates PWM output to change...
Bayindir & Cetinceviz (2011) have designed a water pumping control system which is useful for production plants in harsh environments. Chemicals, vibrations or moving parts may damage the wires that are part of the control system. The control system uses a PLC and Industrial Wireless Local Area Network (IWLAN) to establish control action. Pumping equipment is the primary equipment especially in chemical or food industries (Ali et al 2009). Data communication is necessary for an industrial automation system. Industrial automation system controls production units. The top-level management is able to gather information about the production units through the data communication which is wired or wireless. Wireless communication system plays an important role in the manufacturing industries. They are adopted in the sensor level itself because of its continuous, high resolution, support for mobility, redundancy and compactness (Flammini et al 2009). A survey of industrial requirements to use wireless system discussed by Egea-Lopez et al (2005) confirms that the existing wireless standards meet the industrial requirements.

The process variable in the water pump control system is the water level in a tank. A pressure transmitter measures the water level and the limit switches indentify the minimum and the maximum water levels in the tank. The controller actuates the pump based on the difference between the present water level and the desired water level. The type of the controller is on-off. Hence the controller turns on the pump when the water level is minimum and turns off when the water level is maximum. The entire system has three units. The first unit is a personal computer that is used to develop control program for the PLC. The second unit has a PLC with analog and digital modules, a communication processor and a wireless access point. This unit acts as a
master. The third unit which acts as a client is directly connected to the device which is to be controlled. It has wireless client module, distributed I/O interface module and motor protection package. The PLC sends control command to the pump through the industrial wireless module. The industrial wireless module is connected to the pump through the distributed I/O system. On the PLC side, it is connected through the industrial ethernet. The cycle time for this control is 50ms and the update time of input and output signals is 32ms.

Czeczot et al (2010) has implemented a solution for the problems of control in the simple heat distribution system using Balance – Based Adaptive Control (B-BAC) methodology. It includes the control of outlet temperature of electric flow heater and the fluid flow through equal percentage valve. The B-BAC methodology ensures better disturbance rejection when compared with the conventional PI controller. Even though the disturbances rejected by the PI controller are satisfactory, further improvements in the controller performance will bring economical benefits for longer period of time (Jelali 2006). The laboratory heat distribution plant block diagram shown in Figure 2.10 has the electric flow heater of constant volume, controller C2, equal percentage control valve V1, pump P1, heat exchanger, linear control valve V2 and a PI controller. Impeller type flow meters and RTD are used to measure the flow and temperature of water respectively.

PWM algorithm changes the power supply to the electric flow heater with the help of a thyristor-based unit. Analog I/O plug-in cards from National Instruments are used to interface the process to a computer. LabVIEW is used to implement the SCADA system and the control algorithms for both valves and the electric flow heater. B-BAC controller is implemented in the LabVIEW programming environment as a virtual controller.
The performance of B-BAC type controller is compared with the conventional PI controller. The parameters considered for comparison are the regulation time, overshoot, Integral of the Absolute Error (IAE) and the absolute values of the manipulated variable changes. The B-BAC methodology ensures good control properties without any steady state bias of the regulation error. The antiwind-up action is not necessary since the B-BAC methodology has no integral action.

Ioannides (2004) has implemented a speed monitoring and control of a three-phase induction motor using PLC. It is observed that the efficiency of PLC control is good at high speed. The closed loop control system has speed sensor and load current sensor. PLC controls the PWM inverter based on the inputs it received from these sensors and the desired speed. The PWM inverter changes the induction motor speed which drives a variable load. This implementation provides three functionalities, namely motor speed control,
protection and cut-off or restart of the motor. PI control function block in the ladder diagram takes care of the control action. The PLC uses 7 analog inputs of AIM, 6 outputs of AOM, 8 digital inputs of DIM and 9 digital outputs of DOM. The PLC software regulates and monitors the speed to be constant irrespective of the torque variation. The operator can set the speed and direction of rotation of motor from the control panel. PLC receives the required speed, calculates the actual speed from the tachogenerator and stator current value from the current sensor. These inputs are actually connected as inputs to the AIM. PI control function block uses these data and generates controller output to the final control element. PLC transfers this output to the PWM inverter through AOM. Thus, the PLC ensures that the motor speed is always at the speed set by the operator.

2.3 LADDER DIAGRAM TO HDL CODE

Patel et al (2015) proposed a PLC design using FPGA which can perform parallel execution. It ensures less scan time and higher execution speed. The performance of a conventional PLC is based on the program length and the microprocessor speed. The inability of the PLC to satisfy the needs of certain real-time applications has explored the use of FPGA as an alternate solution to the PLC (Rodriguez et al 2007). A dedicated ladder programming software reads the ladder program, debugs it and converts it into a hex code. Thus, the generated hex code is transmitted to the FPGA through a serial communication. The 52-bit hex code contains information regarding the selection of particular rungs, components and their inputs. This is stored in FPGA block RAM. Each rung is executed by a PLC RISC processor designed using FPGA. An example ladder program implemented in FPGA indicates the maximum and the minimum processing scan time as 226.108ns and 39.308ns respectively. This proves faster scanning time by the FPGA-based micro-PLC than the conventional PLC.
Gawali & Sharma (2009) have done FPGA implementation of microPLC. It is expensive to use PLC for small process control applications. MicroPLC receives ladder program as its input when it is in the program mode. Ladder execution block in the microPLC converts the ladder diagram into VHDL code. This code is used to execute the ladder program in terms of FPGA. Hence it ensures parallel execution of all the rungs.

Economakos & Economakos (2008) have proposed an automated design methodology to generate efficient FPGA implementation for the assigned PLC programs. A white paper by National Instruments (PACs for industrial control 2006) indicates that PLCs are used in small applications contributing to 77% with fewer than 128 inputs. Also, 80% of PLC applications are solved with a set of 20 ladder logic instructions. The number of high speed applications require an alternative for PLC. FPGA implementation has been the best solution for this. However, this requires expertise in both FPGA technology and industrial automation. Conversion of PLC program prepared by PLC programmer into FPGA program is able to overcome this problem. The ladder diagram representation is converted into a high level language C which will be used by Catapult C synthesis software from Mentor Graphics. It produces a VHDL register transfer level description of a particular logic circuit. This will be used for the implementation in FPGA. PLC scan time is maintained as constant by concurrent execution of data acquisition and update process irrespective of the number of rungs and the number of I/Os to be handled. The design methodology is applied to three PID controllers, adaptive and fuzzy logic controllers to validate the concept.

Silva et al (2007) have developed a hardware-software platform to convert logic controllers into HDL codes using petri nets. The hardware of Simatic S7 PLC, reconfigurable hardware, Cyclone FPGA, USB controller and a set of digital and analog I/O cards are used to prove the concept. PLCs
can be implemented using microprocessor (Uzam et al 2001). It can be implemented using FPGA also. The advantages of FPGA are its higher capacity of logic resources, reconfigurability and speed. The flexibility of FPGA technology to develop reconfigurable logic controllers is already proved by Wegrzyn et al (1998). It performs parallel execution and is used to control industrial processes. However, PLCs are widely used to control industrial processes. PNs are used to overcome the sequential execution of PLC, and the parallel execution of FPGA technology is introduced to the industrial market. Logic controllers are designed using petri net (PN) as it is the well-known software in the field of industrial automation. The design automation software identifies the design developed by means of a PN-based graphic system and converts it into a matrix model and stores the retrieved design information in the form of data structure. The algorithm in the software calculates the logic equation from the data structure and translates it into the VHDL code. Now, this code is used for FPGA implementation. A monitor and communication module help to monitor and test the application in the hardware and communicate between the software and the hardware. A specific card with an FPGA and USB communication are used for this purpose. The advantage of using reconfigurable logic controller is the maintenance of cycle time at a constant value because of the parallel execution capability of the hardware.

Miyazawa et al (1999) have developed a controller implemented using FPGA as an application specific integrated circuit. LD was also implemented into FPGA. LD is the most popular programming language to realize the sequential control using programmable controller like PLC. The complication in the FPGA implementation of controller realizes the PLC cycle scan. The clock event of VHDL or translating the coil into an appropriate flip flop element is the way to implement cyclic scan. The
implementation has proposed the manual conversion of an LD representation into VHDL code.

Ikeshita et al (1999) have developed a conversion program from sequential flow chart to VerilogHDL. Programmable controller used in factory automation of a large manufacturing industry is unable to meet the required operation speed because its execution nature is sequential. Being a reconfigurable and flexible device, FPGA is able to obtain the required speed. The outcomes of the literature review and the possible incorporations are summarized in Table 2.1.

**Table 2.1 Summary of literature review**

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Author</th>
<th>Nature of the work done</th>
<th>Extractions of Literature review</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Tan et al (2013)</td>
<td>Multichannel ADC-based Data acquisition system using FPGA was developed. Input range to the ADCs was 0 to 2V.</td>
<td>• Process industries require the input range of 0V to 5V. A suitable alternative must be found out.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The design used the existing ADC. FPGA-based implementation of multichannel ADC will enhance the conversion speed and eliminate the use of separate ADC.</td>
</tr>
<tr>
<td>2.</td>
<td>Atalik et al (2012)</td>
<td>Multiple DSP and FPGA-based digital controller for parallel operated CMCs. PLC was used • As a PI controller,</td>
<td>• FPGA can also be used as a PI controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• To generate digital outputs,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• To inform failures in the control system to the computer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• FPGA can be used to establish the functions performed by the PLC. This increases the execution speed and eliminates the need for PLC.</td>
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<th>Extractions of Literature review</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.</td>
<td>Abdallah et al (2011)</td>
<td>Design of Analog input module</td>
<td>• Process industries require the input range of 0 to 5V. A suitable alternative must be found out.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data acquisition system using FPGA for medical applications.</td>
<td>• Data acquisition system used ADC with analog multiplexer. Acquisition speed will improve further when all the signals are acquired simultaneously. A multichannel ADC can be designed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low power ADC whose range is –0.2V to +0.2V was used. It was increased to the range –1.25V to +1.25V.</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>Monmasson et al (2011)</td>
<td>FPGA-based sensorless motor controller and artificial intelligent-based industrial controller. FPGA was used as a PI controller.</td>
<td>• The parallelism capacity of FPGA can be used in the design of data acquisition and control system effectively.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The execution time of the controller was 85μs.</td>
</tr>
<tr>
<td>5.</td>
<td>Costas-Perez et al (2008)</td>
<td>Educational laboratory system for practical education with sensors, data acquisition and basic control skills. NI USB-6009 module was used to acquire the signals from various sensors.</td>
<td>• LabVIEW can be used to develop the data acquisition system application.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• NI USB-6009 accesses only one analog signal at a time. Multichannel ADC can be designed to access all the signals simultaneously.</td>
</tr>
<tr>
<td>6.</td>
<td>Perelman &amp; Ginosar (2007)</td>
<td>Neuronal recording system with a capacity to process 12 differential signals was developed.</td>
<td>• Since FPGA was involved in the design, simultaneous access of all the signals can speed up the acquisition.</td>
</tr>
<tr>
<td>7.</td>
<td>Thomas et al (2000)</td>
<td>FPGA-based multichannel data acquisition system was developed.</td>
<td>• FPGA processes analog signals one by one even though all the signals can be processed concurrently.</td>
</tr>
<tr>
<td>Sl.No</td>
<td>Author</td>
<td>Nature of the work done</td>
<td>Extractions of Literature review</td>
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| 8.    | Fernandez et al (2012) | Composition and inventory control for a continuous ethanol-water nonlinear pilot distillation column. Adaptive neural network in combination with genetic algorithm was used to control product composition. | • Neural network model using MATLAB and control action by genetic algorithm was done through a computer.  
• This concept may be implemented using FPGA and the improvement can be analyzed. |
| 9.    | Carlos et al (2011) | Data acquisition and speed control of three phase induction motor using vector controlled methods. DSP processor acted as a controller. | • ADC input range is 0V to 3V. Input scan time is 50µs. Industrial standard input range is 0V to 5V.  
• FPGA can be used instead of DSP and its performance can be analyzed. |
| 10.   | Czeczot et al (2010) | Control system for a heat distribution system using B-BAC methodology. | • Processor-based analog I/Os were used. The computer acted as a controller.  
• FPGA can process the analog signal and initiate control action. This eliminates the processor and increases the execution speed. However, LabVIEW and computer can be used for the purpose of monitoring. |
| 11.   | Bayindir & Cetinceviz (2011) | Water pumping control system that will be useful for production plant. | • Monitoring and control of water level was established through wireless system. |
• It is possible to establish control action using FPGA. |
<table>
<thead>
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</tr>
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<tbody>
<tr>
<td>13.</td>
<td>Patel et al (2015)</td>
<td>It identifies the sequential and parallel structures in the LD program. Then, implement it into FPGA after converting the LD code into HDL code.</td>
<td>• The number of rungs is limited by the hardware design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Every rung requires an FPGA-based processor. Therefore, the hardware requirement increases along with the number of rungs.</td>
</tr>
<tr>
<td>14.</td>
<td>Gawali &amp; Sharma (2009)</td>
<td>FPGA implementation of micro-PLC.</td>
<td>• The design does not guarantee concurrent execution of all the rungs since it has duplicated the PLC architecture.</td>
</tr>
<tr>
<td>15.</td>
<td>Economakos &amp; Economakos (2008)</td>
<td>FPGA implementation of PLC programs by converting them into equivalent HDL code.</td>
<td>• LD program is converted into either C or System C using custom-made compiler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The way of eliminating this compiler and direct conversion of LD into HDL code can be looked into.</td>
</tr>
<tr>
<td>16.</td>
<td>Silva et al (2007)</td>
<td>Hardware-software platform to convert logic controller designed using PN into HDL codes.</td>
<td>• The design expects a commercial software tool and a PLC to develop LD.</td>
</tr>
<tr>
<td>18.</td>
<td>Ikeshita et al (1999)</td>
<td>Conversion program from sequential flow chart to VerilogHDL.</td>
<td>• The conversion method has been discussed for a specific example only. The list of LD elements that shall be used for conversion is not explored.</td>
</tr>
</tbody>
</table>
2.4 REVIEW SUMMARY

The detailed review on industrial automation system developed using processor-based PLC and FPGA has been discussed. It is found that FPGA is contributing enough for automation in process industries and it has started to replace the role of PLC. It has been used in the design of AIM, AOM and conversion of LD to HDL code in the form of micro-PLC. The following possibilities are explored out of the review.

- Design and implementation of multichannel ADC that performs concurrent conversion.
- Development of a multiple closed loop control system performs concurrent control of all the physical parameters.
- A direct conversion mechanism that converts LD into HDL code.

FPGA design and implementation of the above concepts have been discussed in the next chapter.