CHAPTER 3

DESIGN AND ANALYSIS OF BRIDGELESS PFC BOOST CONVERTER FED CASCADED H BRIDGE MULTI-LEVEL INVERTER

3.1 INTRODUCTION

Currently, industrial equipments are in necessity of high power and voltage for their operation. Several topologies were introduced to satisfy their power demand. But due to the low power factor, high harmonic distortion and increased losses, the power generated at the output gets lowered, which cannot be sufficient for driving the equipment. Hence it is vital to develop a topology that generates high power with high power factor and less harmonic distortion. In this chapter, a topology of Bridgeless PFC boost converter fed Asymmetrical Seven level Cascaded H bridge multi-level inverter is discussed for generating a high output power with less THD (Total Harmonic Distortion) and a PF (Power Factor) near to unity.

3.2 POWER FACTOR CORRECTION

Power factor correction (Mohanraj et al. 2014) is significant in order to obtain optimistic control over power generation. Power factor is the angle by which load current leads or lags the supply voltage. When voltage and current are in phase, the power factor is unity, so that the power drawn from the supply is utilized efficiently. When it is out of phase, the power factor signifies zero or low, causing the voltage drop and thereby the

efficiency gets lowered. Hence, it is necessary to shape the current related to supply voltage. Various power factor correction topologies are introduced; they are passive power factor correction methods and active power factor correction methods. The passive power factor correction method is used in low power and sensitive application because they are composed of passive components such as resistor, capacitor and inductor. active power factor method is used in medium to high power applications and they use active elements for its construction and have buck (or) boost (or) buck boost converters in their circuit construction.

3.3 BLOCK DIAGRAM OF PROPOSED CONVERTER FED MULTI-LEVEL INVERTER

The Figure 3.1 shows the Closed loop controlled Bridgeless PFC boost converter fed multi-level inverter.

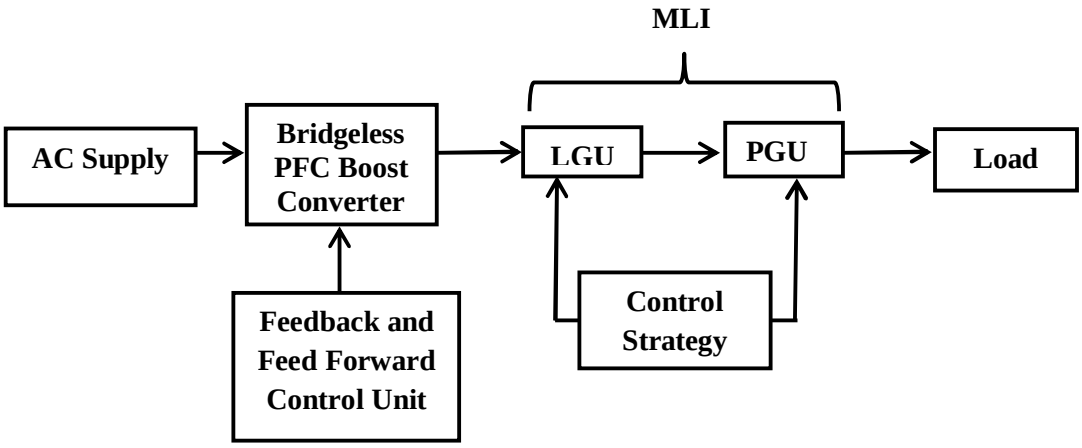


Figure 3.1 Block diagram of proposed converter fed inverter

The AC Supply is given to the Bridgeless PFC Boost converter. Feed forward and feedback control unit is applied to the converter, makes the power factor correction and increases the power factor near to unity. The output of the Bridgeless PFC Boost converter is given to a new seven-level

asymmetrical cascaded multi-level inverter, which is composed of two units LGU (Level Generation Unit), PGU (Polarity Generation Unit). The Level generation unit is used to generate output voltage with required level. The PGU is used to produce output voltage with positive or negative polarity. Staircase PWM technology is used to control the multi-level inverter.

3.4 CIRCUIT DIAGRAM OF PROPOSED CONVERTER FED MULTI-LEVEL INVERTER

The Figure 3.2 shows the circuit diagram of the closed loop controlled Bridgeless PFC Boost converter fed inverter.

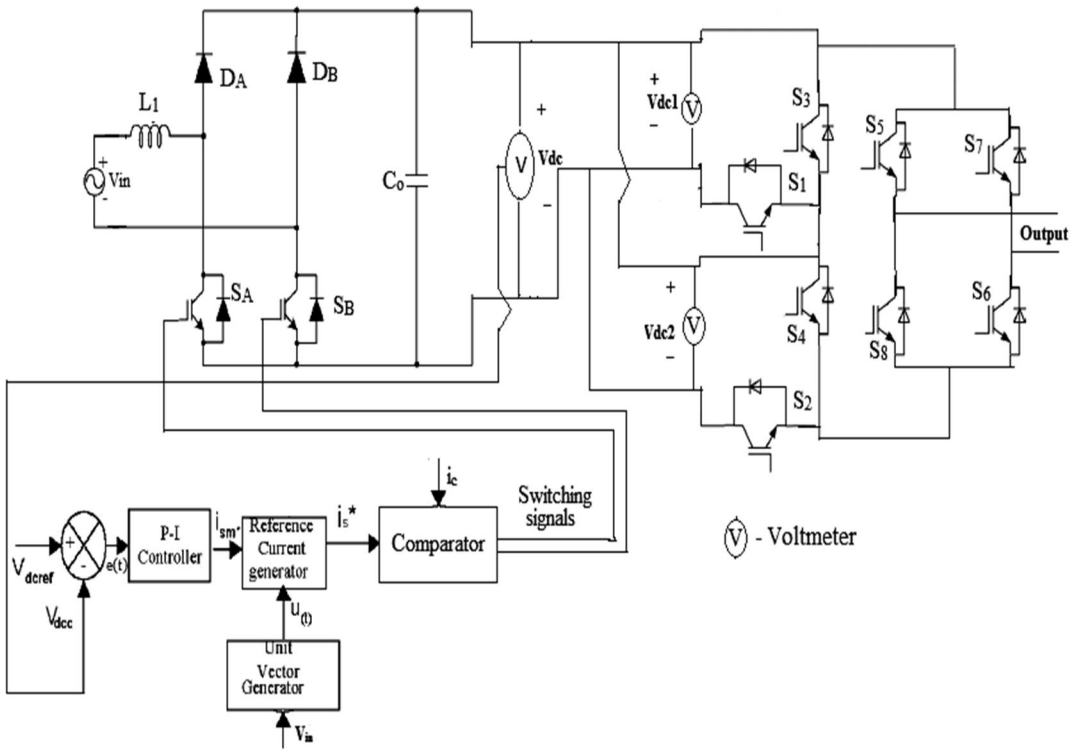


Figure 3.2 Circuit diagram of the Closed loop controlled Bridgeless PFC Boost converter fed inverter

This Closed loop controlled Bridgeless PFC Boost converter fed inverter is proposed to have good output voltage regulation with increased power factor to produce multi- level voltage AC output voltage by using

lower level AC input voltage. The Proposed topology is divided into two sections. One is converter section and the other one is inverter section. PFC Boost Converter section consists of AC input voltage source V_{in}, inductor L_1, diodes (D_A and D_B), IGBT Switches (S_A and S_B) and capacitor $C_{o.}$. The Control unit of the converter section produces switching signals to IGBT switches S_A and S_B. Multilevel inverter section has eight switches. Switches S1, S2, S3 and S4 are used to generate required output voltage levels without polarity. Switches S5 and S6 are used to produce positive half cycle output voltage. Switches S7 and S8 are used to produce negative polarity output voltage. Staircase modulation control technique is used to control the inverter section switches (S_1 to S_8) which minimize Total Harmonic Distortion (THD).

The Proposed multilevel inverter is a seven-level asymmetrical topology, which requires less number of switches and voltage sources. Therefore, the overall cost and complexity are greatly reduced. This topology gives less Total Harmonic Distortion (THD) and high output voltage.

3.5 OPERATION OF PROPOSED CONVERTER FED MULTI-LEVEL INVERTER

3.5.1 Converter Section

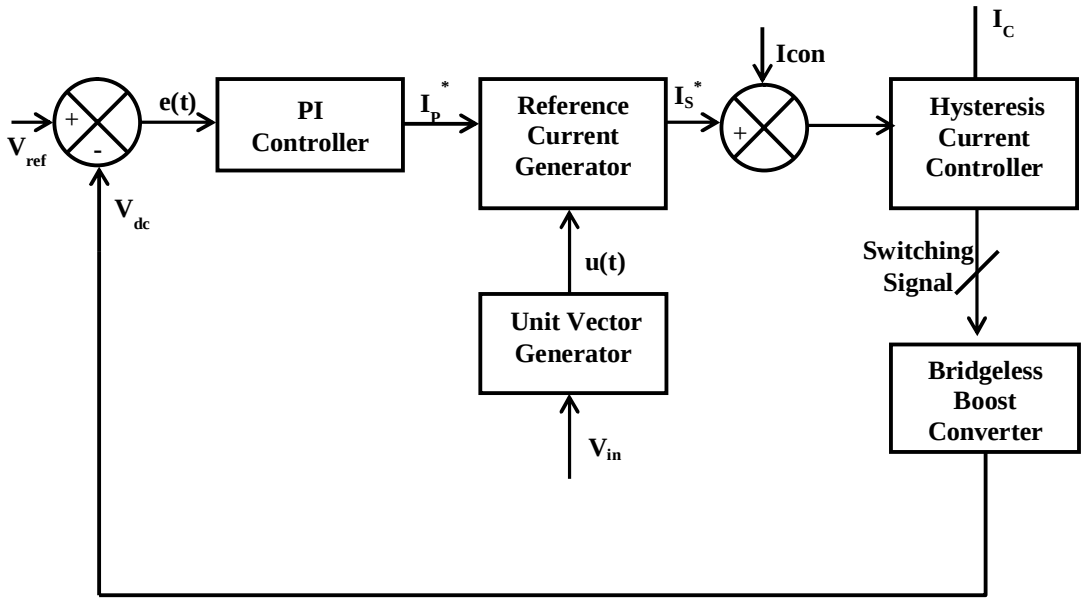
The operation of the Bridgeless boost converter is categorized in four modes. Modes 1 and 2 emanates under the positive half cycle of the input voltage while modes 3 and 4 emanate under the negative half cycle of the input voltage.

During the first mode, the diode D_A and switch S_B conducts and the current flows from the source-L_1-D_A-C_O-S_B. Alternatively, in mode 2, the current flows from S_A and S_B to the load. In mode 3, diode D_B and switch S_A conducts. In mode 4, the switches S_A and S_B conducts and the current flows

through S_1-S_2 and inductor. The capacitor charges and supplies current to the load. This circuit makes the power factor correction and improves the power factor to 0.985.

The Control unit of the converter which produces switching signals to IGBT switches, S_A and S_B is discussed below.

3.5.2 Control Unit for the Bridgeless PFC Boost Converter



(Source : Suja C Rajappan et al. 2013)

Figure 3.3 Control Unit of Bridgeless PFC boost converter

Figure 3.3 shows the block diagram of the Control Unit. The Control unit consists of PI controller, unit vector generator, comparator and reference current generator.

The input AC voltage is given to the Bridgeless PFC boost converter and it produces an output voltage V_{dc}. This V_{dc} is compared with the reference voltage and is given to the PI controller, which is used for tight regulation of output voltage.

After limiting to a safer permissible value, the output of PI controller is taken as amplitude of reference current.

Unit vector of supply voltage is fed to the reference current generator and produces reference sinusoidal unit vector current I_s*. This is compared with converter current to produce reference converter current. Corrective action takes place and produces faster response. The output voltage of PFC boost converter is controlled by D or F_s and thus the power factor correction is achieved.

Initially the output voltage V_{DC} from the converter and the reference voltage V_{ref} are compared by the comparator to produce the error signal e(t). The error signal is given by

$$e(t) = V_{ref} - V_{DC} \tag{3.1}$$

PI (Proportional and Integral) controller in the control unit minimizes the error signal from the comparator and generates the peak value of the reference current (I_p^*).The peak value of the reference supply current (I_p^*) generated is given by

$$I_p^* = e(t).K_p + K_i T_i \int e(t)\, dt \tag{3.2}$$

where K_p and K_i are proportional and integral gain constant of PI controller.

The (I_p^*) reference current peak value and unit vector u(t) supply voltage produced by the unit vector generator are fed to the reference current generator which produces the reference sinusoidal unit vector current (I_s^*). The reference supply current (I_s^*) produced is given by

$$I_s^* = u(t).I_p^* \tag{3.3}$$

Where, u (t) is the unit vector of the input supply voltage.

The reference supply current is compared with the converter current (I_c) by the comparator to generate reference converter current (I_c^*). It is then processed in hysteresis current controller to generate switching signals for the IGBT switches (S_A and S_B).This process takes place in each and every cycle of the input supply and generate fast dynamic response for the converter. The output voltage of the PFC Boost converter is controlled by the duty cycle ratio or the switching frequency variation.

The reference converter current obtained is given by

$$I_c^* = I_c + I_s^* \tag{3.4}$$

Based on the comparison between the converter current (I_c) and reference converter current (I_c^*), the switching signals are given by

$$if\,(I_c > I_c^* + h_b) switch\ S_A\ is\ ON \tag{3.5}$$

$$if\,(I_c < I_c^* - h_b) switch\ S_B\ is\ ON \tag{3.6}$$

Where, $h_b$is the hysteresis bandwidth (ampere).

3.5.3 Inverter Section

The inverter section of the proposed topology consists of Asymmetrical Seven level Cascaded H bridge multi-level inverter using Sub Multi-level inverter and the circuit diagram is shown in Figure 3.4.

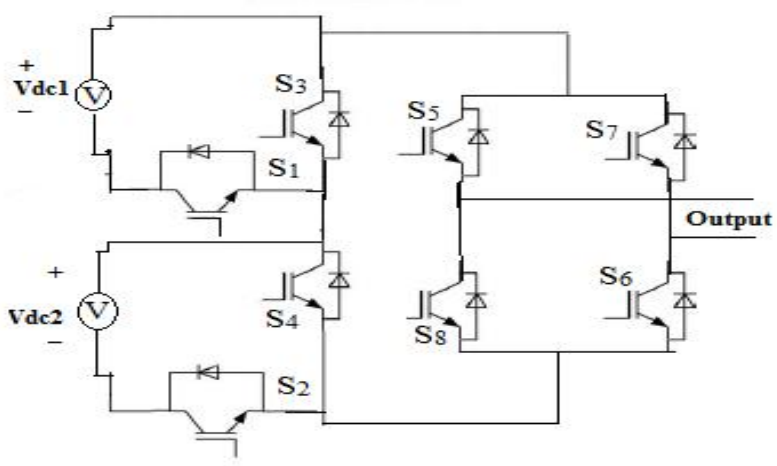


Figure 3.4 Asymmetrical Seven level Cascaded H bridge multi-level inverter using Sub Multi-level inverter

The above asymmetrical multi-level inverter has eight switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7 and S_8). The Switches S_1, S_2, S_3 and S_4 are used to produce required output voltage levels without polarity. The switches S_5 and S_6 are used to produce positive polarity output voltage, whereas the switches S_7 and S_8 are used to produce negative polarity output voltage. The switches in the inverter section are controlled by staircase modulation control technique to get less Total Harmonic Distortion (THD).

The operation of the seven level cascaded multi-level inverter is discussed as follows. In the first four levels, the two of the four switches in sub multi-level inverter conducts alternatively to generate the output level. The switches S_5 and S_6 in cascaded H-Bridge is utilized to generate the positive polarity output. Similarly for the next three levels, the switches S_7 and S_8 in cascaded H-Bridge is utilized to generate the negative polarity output. The Levels of Operation of seven-level asymmetrical multi-level inverter is shown in the Figure 3.5.

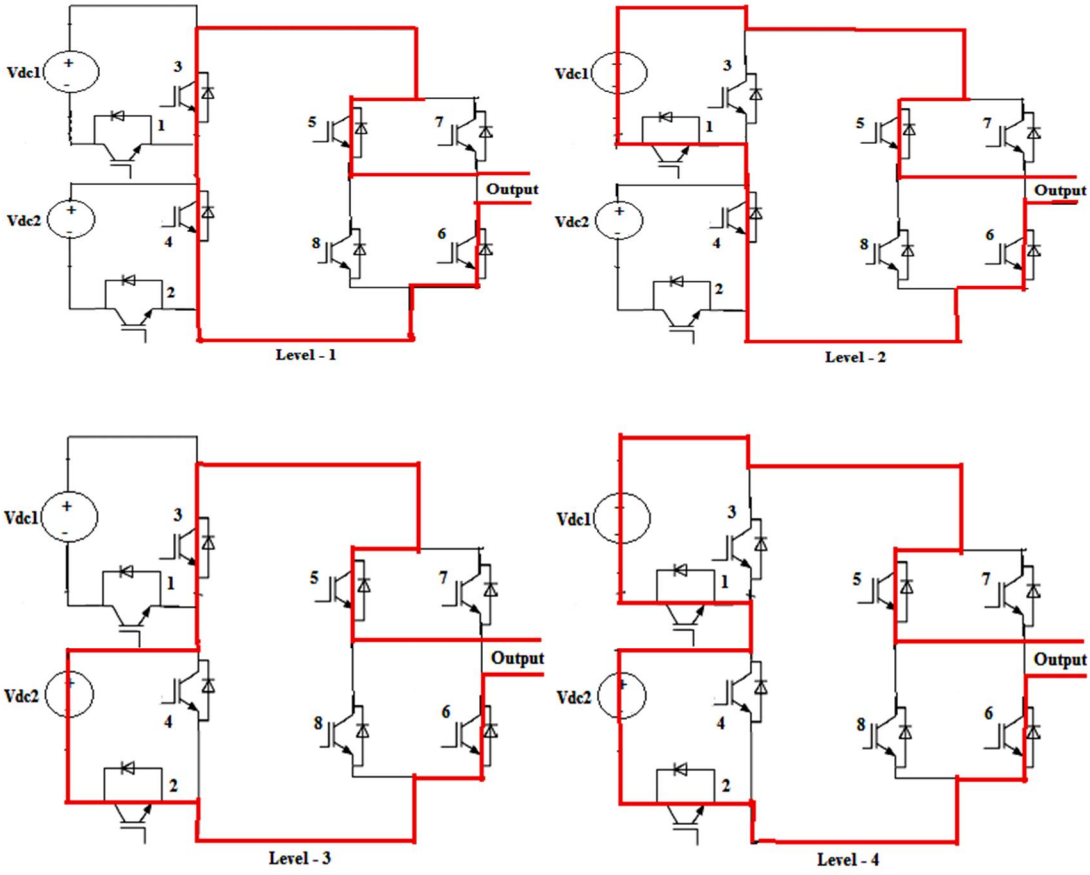


Figure 3.5 Levels of Operation of proposed seven-level asymmetrical multi-level inverter Switching Pattern

The Switching sequences for proposed seven-level asymmetrical multilevel inverter is shown in Table 3.1.

Table 3.1 Switching pattern of the seven level asymmetrical multi-level inverter

Switching sequence								Output Voltage
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Vo
1	1	0	0	1	1	0	0	$V_{DC1}+V_{DC2}$
0	1	1	0	1	1	0	0	V_{DC2}
1	0	0	1	1	1	0	0	V_{DC1}
0	0	1	1	1	1	0	0	$0V_{DC}$
1	0	0	1	0	0	1	1	$-V_{DC1}$
0	1	1	0	0	0	1	1	$-V_{DC2}$
1	1	0	0	0	0	1	1	$-(V_{DC1}+V_{DC2})$

3.6 ANALYSIS OF ASYMMETRICAL MULTI-LEVEL INVERTER

In asymmetrical multi-level inverter, the maximum output voltage is obtained by the following equation

$$V_{omax} = k \sum_{j=1}^{m} VDC, j \; (j = 1, 2, 3 \ldots . . m) \quad (3.7)$$

Similarly, the number of maximum output voltage levels, switches and DC sources are determined by the

$$N_{levels} = 2\,(k + 1)m - 1 \quad (3.8)$$

$$N_{switches} = 2mk + 4 \quad (3.9)$$

$$N_{dc\ sources} = m * k \quad (3.10)$$

Where ‘m’ is the number of cascaded sub multi-level inverters and ‘k’is the number of cascaded H-Bridge inverter.

The DC voltage source of the sub multi-level inverters is determined as follows

$$V_{dc,1} = V_{dc1} \quad (3.11)$$

$$V_{dc,2} = (k + 1)\, V_{dc2} \quad (3.12)$$

$$V_{dc,3} = (k + 1)^2 V_{dc3} \quad (3.13)$$

Where, V_{DC1} - DC voltage source of the first sub multi-level inverter.

V_{DC2} - DC voltage source of the second sub multi-level inverter.

For seven level, two sub multi-level inverters and one cascaded H-bridge multi-level inverter are utilized to generate the V_{DC1}+V_{DC2}, V_{DC2}, V_{DC1}, $0V_{DC}$, -V_{DC1}, -V_{DC2}, -(V_{DC1}+V_{DC2}). The number of output levels and number of switches are calculated as N_{levels} = 7, $N_{switches}$ = 8. The maximum output voltage for seven level is given by

$$V_{omax} = V_{dc1} + 2V_{dc2} \quad (3.14)$$

Where, V_{DC1} - DC voltage source of the first sub multilevel inverter

V_{DC2} - DC voltage source of the second sub multilevel inverter

3.7 RESULT AND DISCUSSION

The performance of the Proposed converter fed multi –level inverter is done by simulation and verified experimentally.

3.7.1 Simulation of Proposed Converter Fed Multi–Level Inverter

The simulation results of the proposed converter fed inverter topology are presented and is are carried out by using Matlab/Simulink. The value of boost up inductor is 1mH and the capacitor used in the converter side is 470 µF.The inverter output is connected to a single phase R-L load. The value of R is 50 ohm and L is 182mH.

The MATLAB / Simulink circuit diagram of the proposed topology is shown in the Figure 3.6.

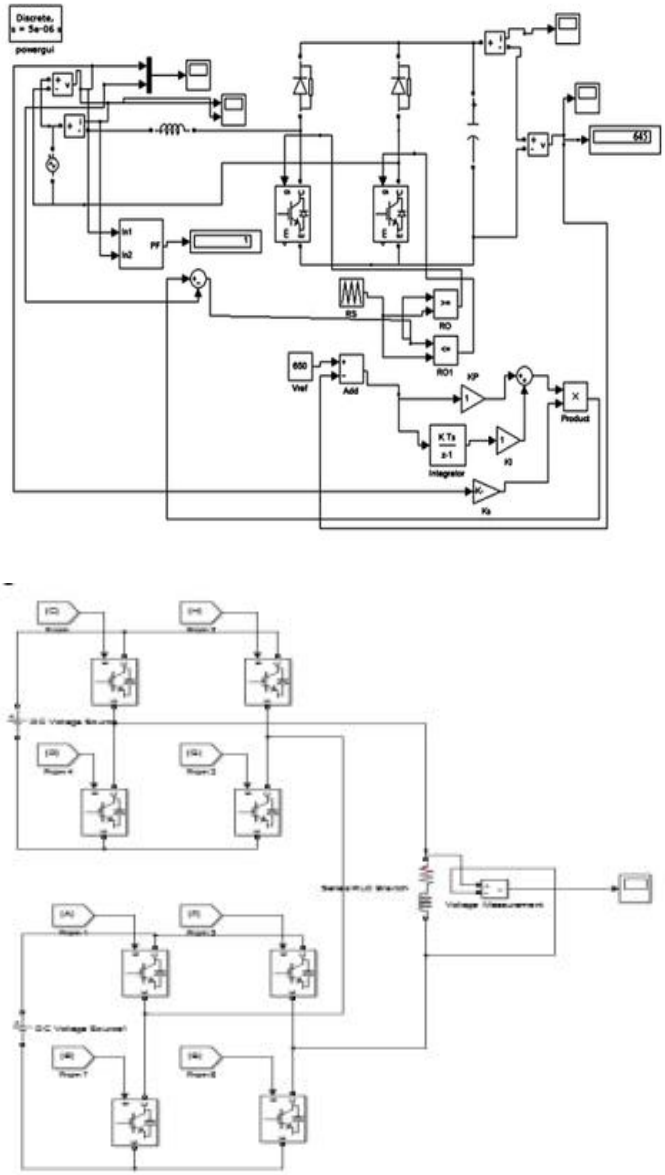


Figure 3.6 MATLAB/Simulink circuit diagram of Bridgeless PFC Boost converter fed inverter

The simulation results of the proposed topology are as follows,

Figure 3.7 shows the AC input voltage of the proposed converter. Input RMS voltage of the converter is 230V AC i.e. 325V peak to peak. The switching pulses produced by the feed forward network for the switches S_A and S_B is shown in the Figure 3.8.

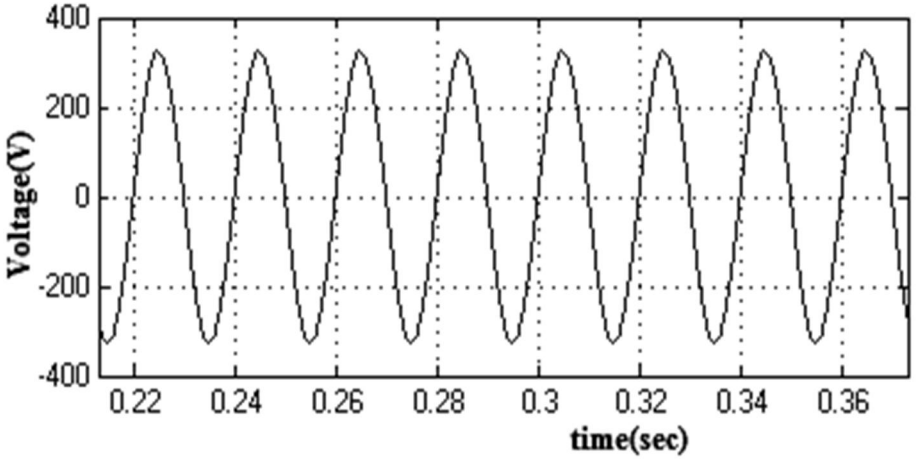


Figure 3.7 Input Voltage waveform of the converter

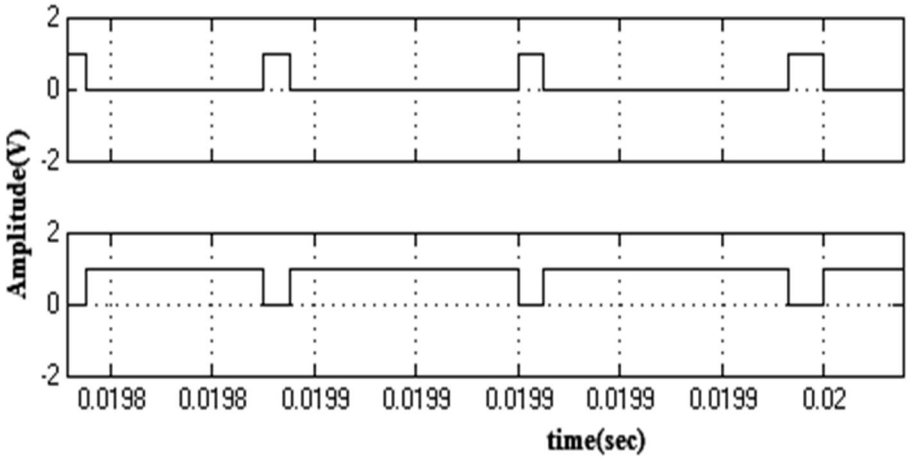


Figure 3.8 Pulses pattern to switches

The current and voltage are nearly in phase as shown in Figure 3.9. Thus the power factor at the supply side is improved and found to be 0.985. The output voltage obtained from the proposed converter is 602 V DC output which is shown in Figure 3.10.

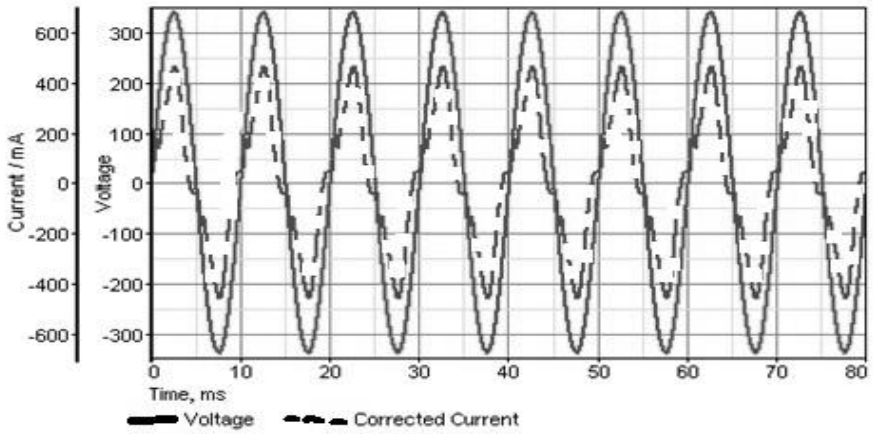


Figure 3.9 Power Factor at the supply of proposed converter

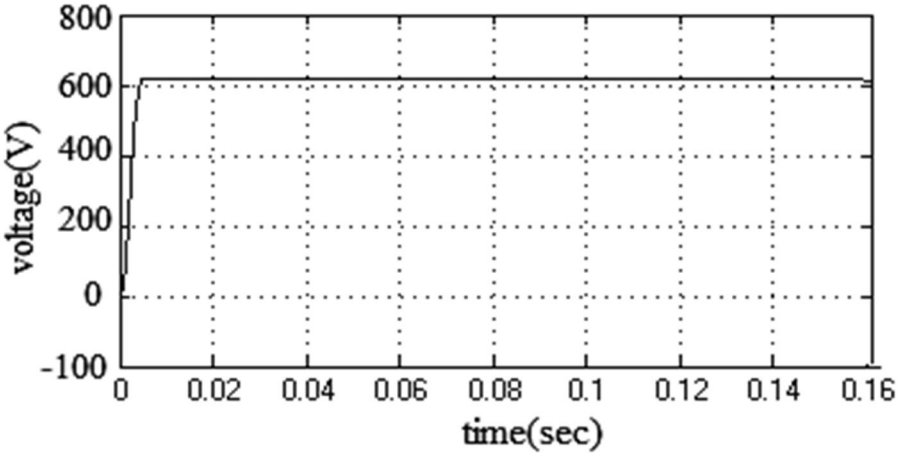


Figure 3.10 Output Voltage of proposed converter

The proposed inverter topology is used to generate seven-level stepped output voltage for a resistive and inductive load. The seven-level inverter stepped output voltage waveform is shown in Figure 3.11 and the corresponding voltage and current harmonic spectrum are shown in Figure 3.12 (a),(b) and Figure 3.13 (a),(b)

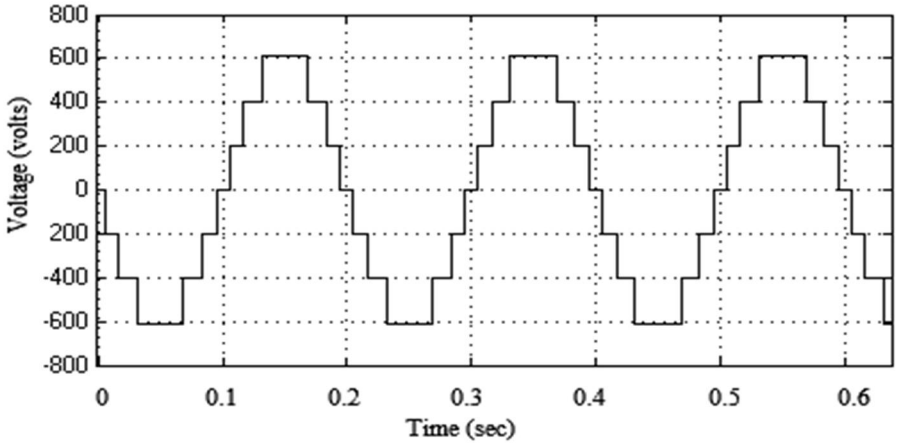
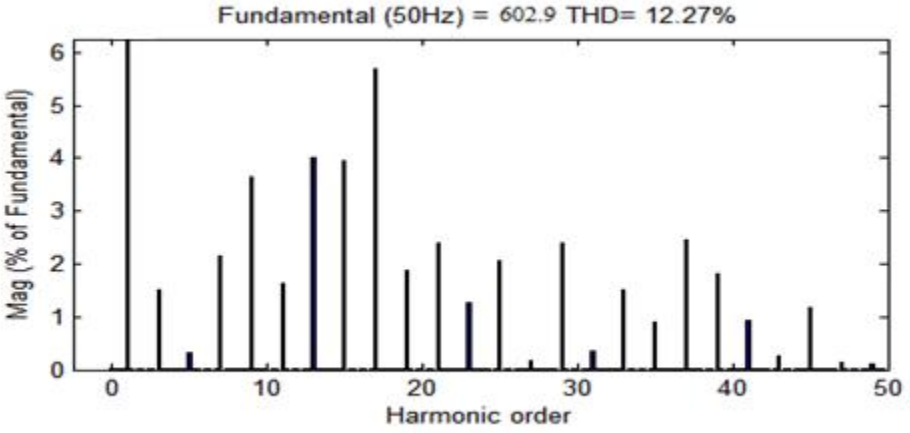
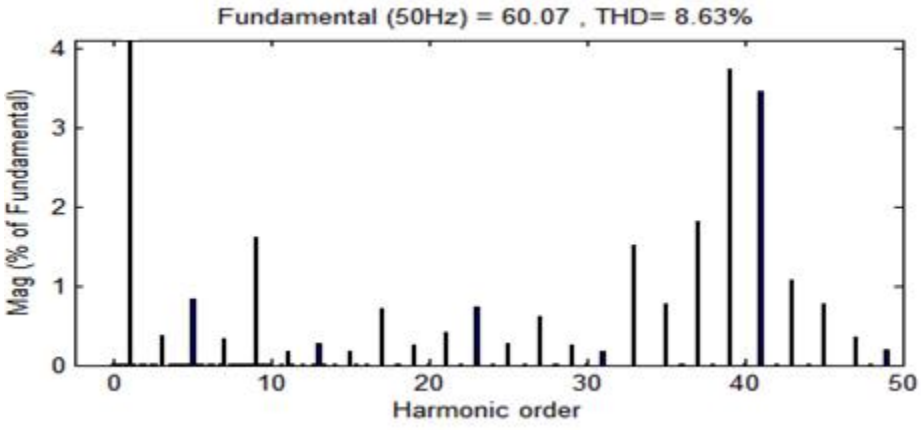


Figure 3.11 Seven-level inverter output voltage waveform



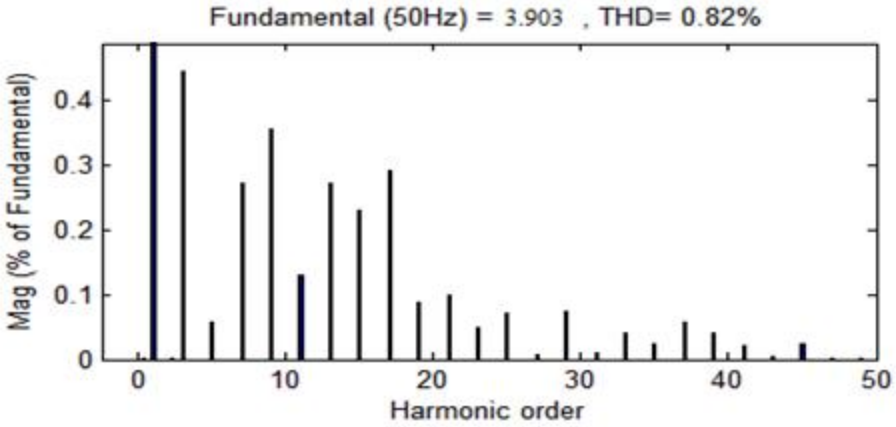
(a)



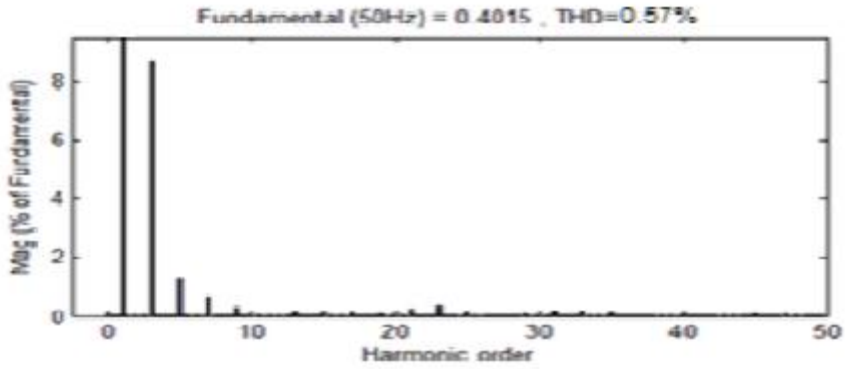
(b)

Figure 3.12 (a) Voltage Harmonics of Conventional cascaded H bridge MLI (b) Voltage Harmonics of Proposed Converter fed Reverse voltage MLI

From the Figure 3.12, it is observed that the voltage THD of conventional cascaded H bridge Multi-level Inverter is 12.27% and with the Proposed Converter fed Reverse voltage Multi-level Inverter is 8.63%.



(a)



(b)

Figure 3.13 (a) Current Harmonics of Conventional cascaded H bridge MLI (b) Current Harmonics of Proposed Converter fed Reverse voltage MLI

It is observed that the current THD of Conventional cascaded H bridge Multi-level Inverter is 0.82 % and with the Proposed Converter fed reverse voltage Multi-level Inverter is 0.57%.

It is inferred that by reducing the THD and by improving the power factor, the efficiency and power gain are increased along with high power and voltage at the output.

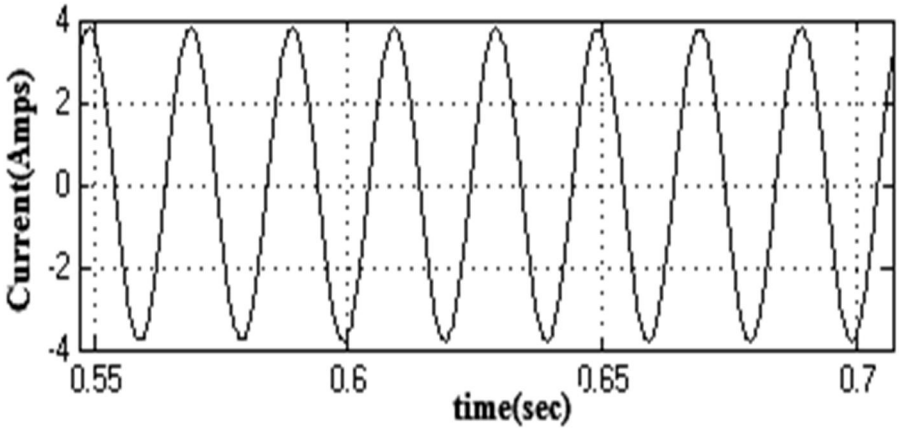


Figure 3.14 Output current waveform

Finally, the output current of the proposed topology is 3.9A and is shown in Figure 3.14.

3.7.2 Hardware Implementation of Proposed Converter Fed Multi–Level Inverter

Experimental prototype for proposed converter fed seven-level inverter topology is shown in Figure 3.1.5. It consists of regulators, converter unit, inverter (level and polarity generation units)**,** four driver circuits and micro controller units.

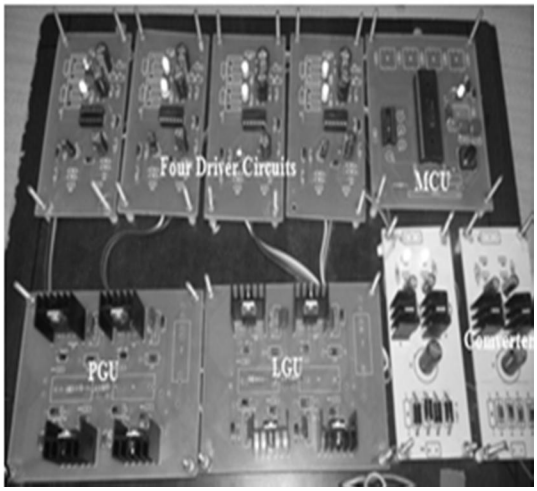


Figure 3.15 Hardware implementation

IRF840 MOSFET is used in both converter and inverter units. Each MOSFET are driven by driver circuits. IR2112 driver IC is used in driver circuits.The PWM controller is implemented by PIC16F877A microcontroller. The 5V regulator (LM7805) is used to give supply to the micro controller unit and the 12V regulator (LM7812) is used to give supply to the four driver circuits. Diodes (1N4000 and 1N5408) and capacitor (470 µF) are used in converter section. The driver circuit of the proposed technique is shown in Figure 3.16.

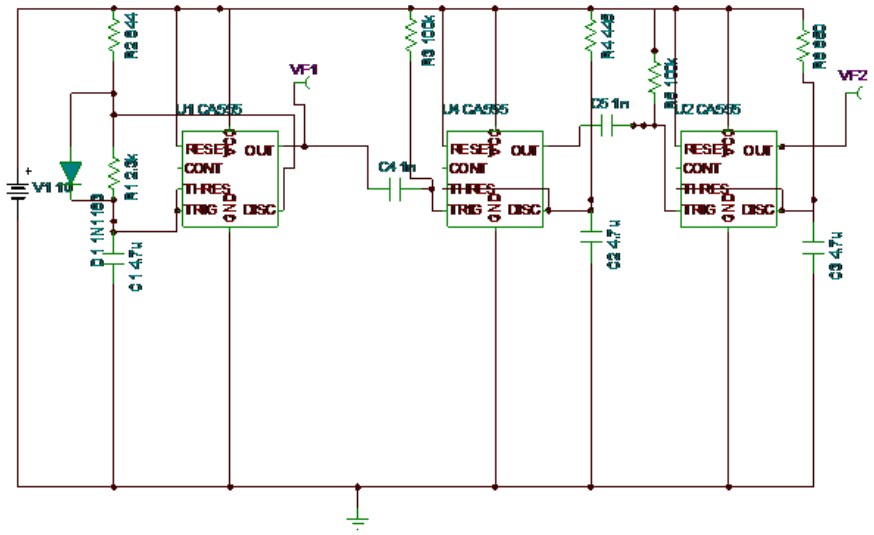


Figure 3.16 Driver circuit

In this, 230V AC supply is given to PFC Boost converter section. The output voltage of the PFC Boost converter is 605V DC, is given to inverter section. It is used to convert 605V DC to 605V AC. i.e. this proposed converter fed inverter topology is used to generate seven voltage levels for a resistive (R=50ohm) and inductive load (L=182mH).

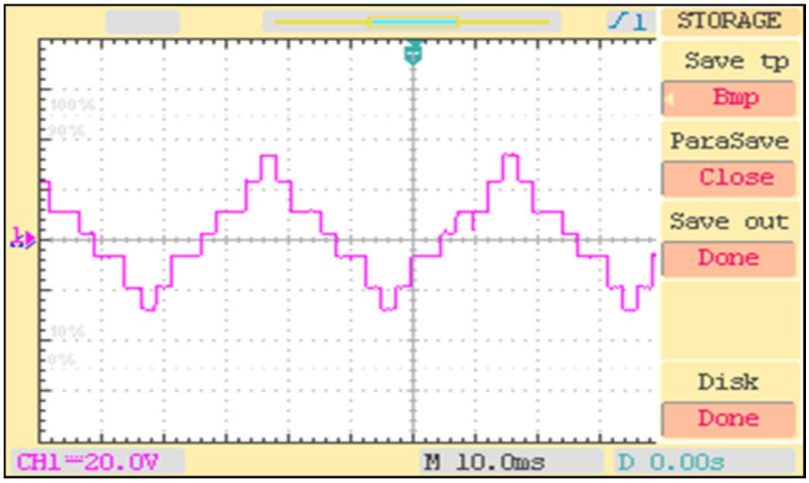


Figure 3.17 Inverter output voltage (scale 300V/div), Time scale (5ms/div)

Figure 3.17 shows the seven-level stepped output voltage at inverter side. Output voltage of the inverter is 605V AC. By using 230V AC input voltage, this topology can generate 605V AC output voltage. So this topology can be used for medium to high power applications.

3.8 CONCLUSION

This chapter provides a brief description about the implementation and performance of Bridgeless PFC Boost converter + cascaded H bridge multi-level inverter topology. Initially the closed loop block diagram and the circuit diagram of closed loop controlled Bridgeless PFC Boost Converter fed multi-level inverter for power factor correction are discussed. The operation and switching sequences of asymmetrical seven level cascaded H-Bridge inverter are explained to produce high power and medium voltage for the industrial applications. The proposed topology has the power factor correction and reduced voltage and current total harmonic distortion. It is observed that the power factor is improved to 0.985. The voltage THD and current THD are 8.63% and 0.57% respectively and also the single phase output voltage is

610V with an output current of 3.9A. This ensures that the proposed method is advantageous over the existing methodologies, with an improved power factor, reduced voltage and current THD and high power output with reduction in number of components, reduction in circuit complexity and less switching losses.