CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

Nowadays many apparatus in industrial applications, are in need of high power and voltage for their operation. But due to high harmonic distortion and low power factor, the power generated at the output gets lowered which cannot be sufficient for driving the industrial apparatus. Hence, it is vital to improve the power factor and to reduce the harmonics in the circuit for producing high power and voltage. For minimizing harmonics and improving the power factor, various schemes have been introduced. Thus in this chapter, reviews on various Multi-level inverter topologies and the schemes employed in those topologies to generate AC voltage, have been presented. Also, it includes reviews on various control techniques and converter topologies for power factor correction and compensators for DC-DC converters for an effective control is presented.

2.2 REVIEWS ON VARIOUS TOPOLOGIES FOR POWER FACTOR CORRECTION

Tanitteerapan & Thanpo (2009) introduced the Continuous Conduction Mode (CCM) Pulse-Width-Modulated (PWM) controller for high power factor boost converters. The duty ratios for this control is obtained by the comparison of sensed signal from inductor current or switch current with the negative slope ramp carrier waveform in every switching period. The

input current waveform is shaped near to sinusoidal waveform, thus providing high power factor and low harmonics.

Keipour et al. (2012) proposed a new technique for power factor correction in the SEPIC (Single-ended Primary-inductor Converter) based rectifier. The input and output voltages of the SEPIC rectifier are sampled so that the input current follows the sinusoidal path. As a result, the input power factor is enhanced and line current's Total Harmonic Distortion (THD) is reduced.

A new parallel-connected power flow technique to enhance the input power factor with instant output voltage regulation by the concern of current harmonic standards is proposed by Vijetha Inti et al. (2013). The converter modules are parallelized to accomplish the preferred output by utilizing smaller size high frequency transformers. This parallel connected arrangement offers smaller passive components with fewer losses in continuous conduction inductor current mode and also moderates the volt-ampere rating of resonant (DC/DC) converter.

Aysha Kemaidesh AL-Kaabi et al. (2013) proposed a step-up bridgeless single phase AC-DC power factor correction (PFC) rectifier attributed to Cuk topology for high voltage battery charger application. This topology involved mutual input stage and parallel output stages with single control signal for exhibiting low magnetic emissions and low inrush current. Moreover, it provides low conduction loss when compared to the conventional Cuk topology.

Suja C Rajappan et al. (2013) proposed a bridgeless power factor correction boost converter for enhancing the power factor and minimizing the harmonic content in the input line currents. In the conventional bridge power factor correction converter, the line-voltage drop is more and hence the use of

bridge rectifier is avoided. Thus in the Bridgeless power factor correction, boost converter is used for reducing the conduction losses and augmenting proficiency of the front-end PFC rectifiers.

The single phase matrix converter topology by Aspalli et al. (2014), operates as UPS (uninterruptible power supply) circuit. This topology functions as a rectifier and inverter in which the H-bridge inverter converts the DC (Direct Current) input into an AC (Alternating Current) output. The MOSFETs are used as switching device, which is controlled by the PWM (Pulse width modulation) technique to generate pulses. Thus this topology ensures input power quality as well as bidirectional energy flow.

Satheyaraj & Yamuna (2014) presented a Single Phase Single Stage Power Factor Corrected (SSPFC) AC/DC converter that uses a single controller to attain regulated DC output voltage. The SSPFC AC/DC converter is the integration of a three-level DC/DC converter and a boost power factor correction converter. It has a supplementary circuit that terminates the capacitor voltage to persuade the input inductor as boost inductor for acquiring unity power factor. The performance and also the power factor gets increased in light load operation.

Himanshu Singh & PratibhaTiwari (2014) developed a circuit for power factor correction by employing an active filter approach. The active filter approach is implemented by the arrangement of the dual boost converters in parallel. It is constructed on an enhanced power sharing strategy to improve the quality of the current and to reduce the switching loss.

Ramesh et al. (2014) presented a Single Phase AC-DC converter topology for power factor correction. It is realized by using the high frequency transformer isolation with Buck topology controlled by Microcontroller and DSP. The major cause behind the converter design is the

accessibility of high frequency with MOSFET as the switching device, have the great switching proficiency with negligible losses. Instead of using a buck topology (Yogesh Dagur & Mukesh Kumar Gupta 2015), Buck–Boost topology is recommended.

Venkata Chalapathi et al. (2014) proposed an enhanced buck power factor correction (PFC) converter topology composed of auxiliary switches and diodes for obtaining high power factor. The proposed topology is operated in continuous conduction mode (CCM) for eliminating the diode loss and provides zero voltage switching. Furthermore, constant ON-time (COT) control is included in this topology to proportionate the switch current with input voltage to obtain high power factor.

Cong-Long Nguyen et al. (2014) introduced a simple grid-voltage-sensorless control scheme for single-phase power factor correction (PFC) boost converters. The grid waveform for this control is acquired relied on phase-lead compensator, DC output voltage and the switching duty ratio. The power in the converter is efficiently utilized to acquire unity power factor and low harmonics.

2.3 REVIEWS ON MULTI-LEVEL INVERTER AND PULSE WIDTH MODULATION (PWM) TECHNIQUES

An asymmetric cascaded multi-level inverter with variable frequency inverted sine PWM technique (VFISPWM) is proposed by Seyezhai & Mathur (2009). The VFISPWM technique incorporates the benefits of the inverted rectified sine wave and variable frequency carriers wave for harmonizing the switching operation in seven level inverter. Furthermore, this technique uses PI controller to the multi-level inverter for providing the output with low THD and switching loss.

Zhong Du et al. (2009) presented cascaded H-bridge multi-level inverter with fundamental frequency switching control. Cascaded H-bridge multi-level inverter is equipped with single DC power source and capacitors to provide a high-quality output power and more number of output levels. The fundamental frequency switching control scheme is used to produce the sinusoidal output with low thermal stress and high efficiency.

A hybrid phase disposition Pulse Width Modulation (PWM) technique is presented by Govindaraju & Baskaran (2009) for cascaded multi-level inverter. A hybrid PDPWM is created by the low frequency Pulse Width Modulation and high frequency Sinusoidal Pulse Width Modulation. The switching scheme obtained by the modulation technique balance the electromagnetic and electrostatic stress between the power devices so that switching losses and switching transitions are lowered. Moreover, the harmonic level is improved in the inverter than the conventional PWM counterpart.

Nasrudin A Rahim & Jeyraj Selvaraj (2010) presented a single-phase multistring five-level Photo-Voltaic (PV) inverter topology with new Pulse Width-Modulated (PWM) control scheme for grid-connected PV systems. Three PV strings are cascaded in parallel, is associated with a five-level inverter to generate the five level output. The switching signals for the switches are generated by the comparison of two identical reference signals with the triangular carrier signal. Moreover, this topology provides near-unity power factor and less Total Harmonic Distortion (THD).

Seyezhai (2011) focused on the asymmetric cascaded multi-level inverter using Carrier Overlapping PWM (COPWM) technique. The modulation technique uses a PIC microcontroller for generating the gating signals which are necessary for the switching pattern generation. As a result,

the root mean square of the output voltage is enhanced and the harmonic content, present at the output is reduced.

Two enhanced natural balancing approaches for FCMLI (flying capacitor multi-cell inverter) under PD (Phase Disposition) scheme proposed by Anshuma Shukla et al. (2011), utilizes the equal (n -1) carrier signals, as used in the typical PD scheme. In the first approach, the switching signals are generated by the verdicts of modulating signal sited in band, carrier waveform rising and falling edges and carrier wave period number. In the second approach, the switching signals are generated by the output voltage level selection relied upon preferential cell selection algorithm. For this five- level inverter topology is realized.

Manasa et al. (2011) proposed various novel pulse width modulation techniques for minimizing the harmonics and improving the output voltage in Cascaded multi-level inverters. Sub harmonic pulse width modulation strategy is used for reducing the total harmonic distortion, while the switching frequency optimal pulse width modulation strategy is used for improving the output voltages in the cascaded multi-level inverter.

Govindaraj et al. (2012) presented a single-phase, five-level inverter topology with a single-DC source.This topology is achieved by cascading three-level flying capacitor inverter with flying H-bridge power cell. Here, suitable switching state is selected from redundant switching states to balance the capacitor voltage regardless of the load power factor. Moreover, it has an important feature of operating as a three-level inverter at its full power rating even though H-bridge fails.

A novel topology of single phase five-level cascaded H-bridge multi-level inverter proposed by Kavitha et al. (2012) uses two DC power source and five switches for increasing the output level, free from any

difficulty in the circuit. Carrier pulse width modulation technique is utilized for reducing the total harmonic distortion, EMI (Electromagnetic interference) and enhancing the output voltage with optimal power factor.

Recently, Multi-level inverters are widely utilized for high voltage and power applications. Yet, it has some drawbacks such as voltage instability, difficult PWM Method and components augmentation. So, Najafi et al (2012) proposed a novel topology with reversing-voltage component for compensating the above mentioned shortcomings. This topology requires less components, fewer gate drives and carrier signals for generating high output voltage. Also, the proposed topology of seven-level Multi-level inverter was constructed and the performance is tested. Instead of using seven-level, Prasitha Prakash (2014) employed a topology proposed with nine levels. Distisha Stephen & Archan (2015) incorporated phase disposition (PD) Sinusoidal PWM (Pulse width Modulation) scheme with seven level inverter.

An asymmetrical five-level cascaded H-bridge multi-level inverter presented by Divya Subramanian & Rebiya Rasheed (2013) uses multi-carrier pulse width modulation technique for modulating the inverter switches. It was introduced to provide high quality output with reduced total harmonic distortion along with the number of switching device reduction, cost and power loss in the circuit.

The cascaded seven- level Inverter topology for converting the uncontrolled DC (Direct Current) into controlled AC (Alternating Current) is proposed by Uma Devi et al. (2013). Sinusoidal Pulse Width Modulation (SPWM) technique is used for generating the pulses for controlling the Induction Motor, Brushless D.C. Motor and is used for large power applications. Furthermore, rotated switching scheme using fundamental frequency switching technique is utilized for generating the switching patterns to balance DC voltage between the capacitors of the inverter. Both techniques

engaged in the integrated structure reduces the Total Harmonic Distortion (THD) and enhances the voltage magnitude of load.

Palleswari et al. (2013) proposed a static synchronous compensator (STATCOM) device for power factor correction and THD reduction in multi-level inverters. STATCOM is a shunt compensation device composed of a DC capacitor, step down transformer with a leakage reactance and voltage source inverter (VSI) for compensating the reactive power and generating multi-level output with less harmonic distortion.

Dhivya Balakrishnan et al. 2013) proposed a new modified H-bridge single-phase multi-level inverter for grid connected PV systems with a new pulse width modulated (PWM) technique. The inverter utilizes an H-bridge output stage with two bidirectional auxiliary switches for generating the seven output voltage levels. The PWM technique in this use three identical reference signals and triangular carrier signal for generating the switching signals for the power devices. By this topology, the number of power devices and also the number of capacitors in the asymmetrical configuration gets reduced. Moreover, the topology concerns a current-control algorithm and maximum-power-point tracker (MPPT) for grid-connected photovoltaic system.

Bharatiraja & Mohammad Shabin (2013) proposed a single source topology of multi-level inverter for enhancing the power quality and reducing the harmonics. This topology uses minimum switching devices, when compared to conventional multi -level inverter to generate the high AC output voltage. Additionally, the error correction block is incorporated in this topology to overcome the variable input voltage conditions to improve the efficiency and to reduce harmonic content in the output waveform.

A cross-switched multi-level inverter topology is proposed by Farhadi Kangarlu & Babaei (2013) with reduced number of switches. This type of topology does not have any high voltage switches, which can be prolonged for any number of voltage levels to generate high quality output voltage. Moreover, the harmonic content, cost, size are also reduced by the use of the proposed topology.

Mohan Reddy & Gowrimanohar (2013) proposed a cascaded multi-level inverter based on Dynamic Voltage Restorer (DVR) to reimburse voltage swell, voltage sags and interruption on power systems. The Synchronous Reference Frame theory (SRF) along with PI (Proportional and Integral) controller is used for generating a reference voltage for the Dynamic Voltage Restorer (DVR). Finally, along with PWM control the output voltage is regulated at the load terminals devoid of power quality issues.

A new Diode clamped Multi Level Inverter presented by Mohan Teja et al. (2014) is employed without the series connection of clamping diodes. This multi-level inverter topology was introduced to eradicate the unbalancing of the DC links, indirect clamping and DC rails turn on snubbing that prevails in conventional diode clamping inverter. In this, supplementary resistive clamping network is used for indirect clamping. Moreover, the Pulse width Modulation technique is employed for modulating the devices that are associated with the circuit topology. As a result, the newly introduced Diode clamped Multi Level Inverter has Total Harmonic Distortion of 12.45%, which is less than the conventional diode clamping inverter.

Xiaodong Yang et al. (2014) proposed a generalized Space Vector Pulse Width Modulation (SVPWM) with the digital realization method for generating a switching pattern of the power devices in the cascaded H-bridge multi-level inverters. The generalized SVPWM technique for the cascaded multi-level inverter is realized by the carrier phase shift strategy. The digital

realization method in generalized SVPWM avoids coordinate transformations, complex trigonometric function calculations, time duration calculations and space vector selections during modulation.

A simple space vector PWM method is proposed by Sirisha & Satishkumar (2014) for resolving the drawbacks such as redundant switching states and large space vector by space vector PWM in multi-level inverters. It efficiently defines the location of the reference voltage vector and estimate the dwell times, which can be directly applied to the cascaded H-bridge inverter of any voltage levels. The memory requirement, complexity and the voltage harmonic distortion gets reduced.

A power converter topology for PV applications is proposed by Vaishnavi & Seyezhai (2014). The converter topology is composed of DC/DC power converter and seven- level inverter equipped with capacitor selection circuit along with a full bridge converter with decreased number of switches. By this arrangement of inverter, the DC output from the converter is converted into seven level AC (Alternating Current) output voltage. Moreover, the single and dual carrier modulation strategies are included in this topology for enhancing the spectral quality of the output.

Giampaolo Buticchi et al. (2014) suggested a Nine-Level Grid-Connected Converter Topology to synthesize nine level output voltage for Single-Phase Transformer for PV Systems. The topology contains two cascaded full bridges with different DC-link voltages to generate the output with reduced harmonic distortion and electromagnetic interference. Furthermore, the switching strategy employed in this topology regulates the voltage and efficiency, while the transient circuit reduces the common-mode leakage current.

Sumit K Chattopadhyay & Chandan Chakra borty (2014) proposed a novel Multi-Level Inverter (MLI) topology based on Level Doubling Network (LDN) for enhancing the power quality and reducing the switching frequency. The topology uses symmetric cascaded H-bridge MLI along with half-bridge inverter (LDN circuit) for doubling the measure of the output voltage levels. Moreover, the LDN has the self-balancing capability during the positive and negative cycles devoid of control methods and power.

Md. Rabiul Islam et al. (2014) proposed a High-Frequency Link Multi-level Cascaded Medium-Voltage Converter for renewable generation systems and smart grid applications. For this, modular five-level cascaded converter is realized. The high-frequency link connected to the converter produces various unique and stable DC supplies for the converter to minimize the common mode problems and voltage imbalance.

A five-level inverter is presented by Sridhar et al. (2014) for inoculating the solar power into the grid, to eradicate the harmonic distortion, switching losses and EMI produced by the switching operation. The proposed five-level inverter is composed of two DC capacitors, associated with the dual-buck converter and single phase H-bridge converter. The output voltage from the dual-buck converter is fed to the full-bridge inverter, gets synchronized with the supply voltage to generate five level AC output voltage, which are then injected to the grid.

Satish Kumar et al. (2014) presented a Sequential Switching Hybrid-Modulation (SSHM) algorithm, which operates at low frequency for minimizing the loss in the cascaded multi-level inverters. It is the technique which embeds PWM switching and sequential switching techniques for balancing the power dissipation among the power devices. Furthermore, it is

applied to Multi-level sinusoidal-modulation (MSPWM) schemes such as Alternative Phase Opposition Disposition (APOD), Phase shifted carrier (PSC) to achieve fundamental voltage tracking and to obtain reduced switching loss and commutations.

Kishorbommassani & Ram Prasad (2015) proposed a new technique named Harmonic Reduction-Pulse width Modulation (HR-PWM) for obtaining high-power, less harmonics and high voltage. For this, cascaded multi-level Voltage Source Converters (VSC) composed of power devices (IGBT/diode) with equal DC voltage sources is realized. Genetic algorithm is employed for attaining optimal firing angles to trigger the power devices so as to observe 70-80% THD in the output.

Khounjahan et al. (2015) proposed a new cascaded transformer multi-level inverter topology to reduce the number of switching devices with modified selective harmonic elimination modulation. This topology has a DC source, two main power switches, bidirectional switching devices and single phase low-frequency transformers. Generally, four switching devices are required for each transformer of the inverter topology, but this requires only one bidirectional switch for transformers. Selective Harmonic Elimination (SHE) technique is used in the inverter to acquire a high quality output voltage. By this the switching losses are decreased along with component reduction.

BasemAlamri & Mohamed Darwish (2015) presented an online model for accurately estimating the switching and conduction losses in cascaded H-bridge multi-level inverter. For this purpose, single-phase 13-level cascaded H-bridge with switching device (IGBT's) is realized with Selective Harmonic Elimination (SHE) PWM technique for controlling the

inverter. Moreover, Genetic Algorithm (GA) is used for switching angle optimization in addition to the Curve fitting tool that is used to generate the equations comprehended in the model which relied upon power switch datasheet.

2.4 REVIEWS ON VARIOUS COMPENSATORS FOR DC-DC CONVERTERS

Mor Mordechai Peretz & Sam Ben-Yaakov (2007) proposed a Digital PID Compensator based on time domain for the PWM DC-DC converters namely Buck, Boost, Buck-boost converters. The main idea behind the design is that the closed-loop response of the system is mostly determined by the first few samples of the compensator. Moreover, the proposed compensator design is based on the discrete domain to provide exact specifications and to avoid errors in the system.

Sang Hwa Jung et al. (2007) described a technique of dual path internal frequency compensator for DC-DC converters. The proposed compensator is the integration of integral component composed of conventional voltage mode with miller capacitor and a proportional component composed of trans-conductance amplifier with a resistor load. This, dual path internal frequency compensated DC/DC converter can be used for mobile systems or systems which has small number of pins.

Kaithamalai Udhayakumar et al. (2008) presented a Posicast compensated hybrid controller for the DC-DC Buck converter in Continuous Conduction Mode (CCM) for eliminating the noise and sensitivity issues in the systems. It is a feed forward compensator which is independent of time delay, helps to eradicate the overshoot in step response of the system and to

reduce the undesirable sensitivity in the system. Instead of DC-DC Buck converter Kumar et al. (2011) utilized DC-DC Boost converter.

SEPIC (single ended primary inductor converter) is a non-inverting DC–DC converter which generates the output voltage greater or lesser or equal to input voltage .But this converter are sensitive to frequency variations and noise. In order to control, Kalantar & Mousavi (2010) proposed a Posicast control with feedback structure for eliminating and reducing the sensitivity issues.

A Hybrid Three Step Damping Compensator (HTSDC) presented by Sruthi & Raghavendar (2012) eliminates the overshoot problems in the DC-DC Boost converter. The proposed compensator along with an integral compensator is functioned with in the feedback loop of the system, to tune the system to eradicate the frequency variations for ensuring the steady state response.

The Ant Colony Optimization (ACO) by Mahendran & Kandaswamy (2013) is introduced for tuning the Proportional and Integral (PI) compensator which is used in Single Ended Primary Inductance Converter (SEPIC) for generating constant voltage from varying input voltage. The Proportional and Integral (PI) compensator is used in the converter for stabilizing the constant output voltage without changing the polarity of the voltage, while Ant Colony Optimization (ACO) is used in PI controller for obtaining optimal solution. Hence by this method, the ripples at the output are reduced along with minimum peak overshoot and thus provide constant voltage at the output.

Generally, pulse mode operation in DC-DC Converters has Electromagnetic Compatibility (EMC) issue due to high frequency EMI

currents introduced in them. In order to reduce this issue, Smolenski et al. (2013) proposed a new compensator named CM (Common Mode) voltage compensator. This compensator for the converter, reduces the EMI current amplitude and also eliminates the unnecessary accumulation of EMI current which are generated by the converter groups.

Nivya K Chandran & Mary P Varghese (2014) proposed two novel control strategies with PID compensator for controlling and improving the efficiency of Synchronous Rectifier (SR) Buck Converter. In the first strategy, SR technique is utilized for reducing the conduction losses under heavy load condition, whereas in the second strategy, ZVS technique is utilized for reducing the switching losses under light load conditions.

A Neuro Fuzzy Sliding Mode Control Technique is proposed by Gurumoorthy & Thirunavukkarasu (2014) for the Boost Converter. The proposed technique is the integration of Adaptive Neuro – Fuzzy Inference System (ANFIS) scheme and Total Sliding Mode Control (TSMC) Scheme. The Adaptive Neuro – Fuzzy Inference System (ANFIS) scheme is utilized in the converter for obtaining enhanced Total Harmonic Reduction (THD), current control, voltage control and maximum power at the system, whereas Total Sliding Mode Control (TSMC) is used for improving the strength of the system during the transient period.

2.5 CONCLUSION

This chapter provides a survey on Power Factor Correction topologies and techniques, multi-level inverters, PWM (Pulse Width Modulation) Schemes and Compensators. Initially, parallel-connected power flow technique, matrix converter topology, open loop Bridgeless PFC

converters topology, active filter approach and various PFC circuits which involves in power factor correction are discussed. Then, various Multi-level inverter topologies and the PWM (Pulse Width Modulation) schemes employed in those topologies (i.e.,Cascaded multi-level inverters with sub harmonic pulse width modulation scheme, Reverse voltage multi-level inverter) for harmonic reduction and high level AC voltage generation are discussed. Then, the various types of compensators like hybrid three step damping compensator, dual path internal frequency compensator, PID Compensator, CM (Common Mode) voltage compensator for eradicating the sensitivity issues and providing steady state output voltage in DC-DC converters are discussed.