ABSTRACT

The primary goal in a high speed digital system is maintaining signal integrity in the presence of crosstalk. Crosstalk is one of the major concerns for signal integrity issues and needs to be reduced for the better performance of circuit boards. Crosstalk arises due to electromagnetic coupling when the traces of a printed circuit board are in close proximity. Miniaturization of mixed signal systems demands that the traces are as close as possible and maintain signal integrity. Therefore, crosstalk is a challenging issue for the interconnect engineers and increases rapidly with the increase in rise and fall times. To avoid the crosstalk, traces can be routed with more spacing between them but it leads to the increase in the board area and cost associated with it. Hence, a tradeoff is needed between the signal integrity, crosstalk and board size (miniaturization) without affecting the data rate. In a closely coupled two line system, two types of crosstalk exist. Near-end crosstalk (NEXT), which is generated at the near-end of the victim line and far-end crosstalk (FEXT), produced at the far-end of the victim line due to the electromagnetic coupling. The far-end crosstalk is a major source to cause signal integrity problems by reducing the signal-to-noise interference ratio and it introduces crosstalk induced jitter. This affects the receiver's performance and the bit error rate thereby limiting the speed of the data transfer. The near-end crosstalk introduces a delay in the digital signal to cause data jitters.

The proposed work analyzes the crosstalk behavior with signal integrity and mitigation of crosstalk in the coupled lines of printed circuit boards. This is achieved by implementing metamaterial configurations in the form of complementary split-ring resonators (CSRRs). The proposed design provides embedded CSRRs ground to control the crosstalk in the coupled
lines of the PCBs. A new design of multi-ring CSRR is etched in the ground plane to achieve the reduction of crosstalk. The multi-ring CSRR structure is formed by combining two coupled CSRRs one within the other. Design simulations are carried out by considering individually the outer CSRRs, inner CSRRs and multi-ring CSRRs for the frequency range of 6 to 8 GHz. The greatest advantage of using CSRRs is that it can be implemented on the same circuit board without any additional circuit elements and can be etched by conventional techniques. In order to get compact effectiveness, square type of multi-ring CSRRs configurations is used in this analysis. The electromagnetic interaction of the coupled lines with the designed CSRRs are interpreted with the Maxwell’s equations and the governing equations.

The crosstalk can be modeled as a forward crosstalk and a backward crosstalk through the mutual coupling of capacitances and inductances between the lines. In the near-end of the victim line, the interferences caused due to these impedances are added together and at the far-end the difference between them exists. The driver current induces noise at both the ends of the victim line and is proportional to the speed of operation.

This dissertation analyzes the crosstalk behavior of the PCB by means of frequency domain scattering parameters and time domain eye diagrams with jitter performance. The total jitter expressed as probability density function of $3\sigma$ Gaussian distribution was analyzed for the solid ground and CSRR etched ground. The jitter histogram for solid ground gives a maximum of 4000 samples of pulses with 7 psec earlier to the ideal time and asymmetrically placed thereby increasing the timing jitter and phase jitter. But the CSRR designed ground gives 8000 samples of pulses are symmetrically placed with zero backlash. The crosstalk parameters are analyzed by developing the eye diagrams for a rise/fall time of 100psec with a
driver voltage of 1V NRZ pulses. The eye diagram of CSRR etched ground improves by an amount of 3.7% in the eye opening and 37% of increase in the signal to noise interference ratio. Single edge modeling techniques provides more insight to total jitter performance to understand the crosstalk behavior on high speed data to develop jitter budget.

The NEXT and FEXT values are obtained from the frequency domain S-Parameters. $S_{31}$ is the measure of near-end crosstalk and $S_{41}$ gives far-end crosstalk. The FEXT for the solid ground has an average value of -10 dB over the frequency of 6 GHz to 8 GHz. The NEXT has the oscillating behavior between -30 dB to -20 dB for the same frequency range. The reduction of FEXT is achieved through a novel design of multi-ring CSRRs in the ground plane. Parametric analysis is carried out for the multi-ring CSRRs in the ground plane with different positions. When a single unit of multi-ring CSRR is designed at the center of the ground plane, the FEXT is -20 dB at 8 GHz. When two unit cell of multi-ring CSRRs are designed at the two ends of the coupled lines in the ground plane, a reduction of -50 dB at the frequency 7.1 GHz and for three unit cells of one at centre and other at the two ends -44 dB at 6.88 GHz is achieved. The NEXT is also reduced over the frequency 7.2 GHz to 7.6 GHz by 3 dB. In addition to NEXT and FEXT analysis, single ended S-Parameters $S_{21}$ (insertion loss) and $S_{11}$ (return loss) are also analyzed for the effectiveness of the design.

The design analysis is carried out with individually coupled CSRR configurations of multi-ring CSRR structures by considering outer CSRR and inner CSRR separately for 6 GHz to 8 GHz. The outer CSRR gives a FEXT reduction of maximum value of -13.45 dB at 7.5 GHz when one unit cell is at center, -23.56 dB at 7.5 GHz. When two unit cell of CSRR considered at the two ends and with three units of CSRRs in the ground plane -24 dB at 6.8 GHz suppression is achieved. The inner CSRR of multi-ring configuration
gives an effective suppression of FEXT with a maximum of -25 dB at 6.13 GHz with three units at center. When single unit at center and two units at two ends are used the FEXT values are -14 dB and -16 dB reduction at 6 GHz respectively. The reduction of 5 dB is achieved in the NEXT with the inner CSRR design. From these discussions, implementing the CSRRs in the ground plane effectively reduces the crosstalk which occurs in the printed circuit boards. Finally the proposed design is fabricated and the $S_{41}$ and $S_{31}$ measurements are taken for the fabricated structures using network analyzer.

This thesis is made in a way to realize the crosstalk mechanisms generated due to the closely packed transmission lines of the printed circuit boards. The efficient and effective method of suppression is achieved using metamaterial configured complementary split-ring resonators. The proposed design implementing CSRRs in the ground has significant advantages in tackling the crosstalk problems and greatly reduces the cost. The methodologies and modeling used in this work gives a clear insight to the characterization of crosstalk and provides a useful tool for efficient analysis related to electromagnetic compatibility design of multilayered PCBs predicting the electromagnetic interferences in high speed systems for a noise free era.