Chapter 4

Influence of Different Structural Parameters on the Performance of a Tunnel FET

4.1 Introduction

In this chapter, we present a detailed investigation of the influence of different device structural parameters on the device characteristics of both n- and p-channel TFETs. Results of such investigation on n-TFET are presented first [97], followed by that on p-TFET. For both n- and p-channel TFETs, the effects of varying both the dielectric-constant and the width of a spacer and the source doping level are shown. Impact of a gate overlap/underlap on the TFET characteristics is also included. In addition, the effects of the fringing electric-field arising out of a high-k gate dielectric on the device performance are presented for a p-TFET [102].

4.2 Impact on the Performance of n-TFET

The device structure, as shown in Fig. 3.1, with a gate length $L_g$ of 50 nm, and a work function $\phi_m$ of 4.5 eV for the gate metal are used for the results presented in this section. Unless otherwise mentioned hafnium oxide of 1-nm equivalent oxide thickness (EOT) is used as the gate insulator. Unless otherwise mentioned, the source and the drain are made of highly doped ($1 \times 10^{20}$ atoms/cm$^3$) p-type and n-type regions, respectively. The intermediate channel region is made of a moderately doped ($1 \times 10^{17}$ atoms/cm$^3$) n-type layer. A uniform doping profile is used for all the regions, with an abrupt profile at the interfaces. It has been verified that the use of a quantum density-gradient model in the simulation has a very little impact on the results presented here.
4.2.1 Effects of Variation in the Spacer Dielectric Constant

The device performance is first studied for different values of the dielectric constant $\kappa$ of the spacer while keeping its width fixed at 50 nm. The $\kappa$-values of the spacer used are 2, 3.9, 7.5, and 21, which may correspond to the interlayer dielectric, silicon dioxide, silicon nitride, and hafnium oxide, respectively. The transfer characteristics for different values of $\kappa$ of the spacer are shown in Fig. 4.1. In addition to an increase in the threshold voltage $V_T$, it is observed in Fig. 4.1 that an increase in the $\kappa$-value results in corresponding degradation of the device performance in terms of both $I_{ON}$ and $S$, similar to that reported in [52]. The value of $V_T$ is extracted using the constant current ($10^{-7} \text{ A}/\mu\text{m}$) definition and found to be 0.45, 0.48, 0.5, and 0.6 V, respectively, for $\kappa = 2, 3.9, 7.5, \text{ and } 21$. The output characteristics for different values of $\kappa$ are shown in the inset in Fig. 4.1 for a gate overdrive voltage $V_{GT} = V_{DS} - V_T$ of 0.5 V from which it can be clearly seen that a decrease in the $\kappa$-value of the spacer makes a good improvement in $I_{ON}$ for the same gate overdrive voltage.

![Figure 4.1: Transfer characteristics for $V_{DS} = 1$ V for different values of $\kappa$ of the spacer dielectric. The inset shows the output characteristics for a gate overdrive voltage of 0.5 V.](image)

In order to get an insight of the above observations, the simulated energy band diagram around the tunneling junction of the device biased at $V_{GS} = V_{DS} = 1$ V at a distance of 1 nm below the top oxide–semiconductor interface is plotted in Fig. 4.2
for different values of $\kappa$ of the spacer. For a TFET, it may be recalled that the electrons from the valence band of the source, which is henceforth referred to as the tunnel-source, tunnel into the conduction band of the adjacent (normally the channel) region, which is henceforth referred to as the tunnel destination. The potential barrier formed by the band gap of the semiconductor across which the tunneling of electrons takes place is henceforth referred to as the tunneling junction. The tunneling junction for the device in Fig. 3.1 lies very close to the metallurgical source-channel junction, as can be verified in Fig. 4.2. It is evident in Fig. 4.2 that an increase in the $\kappa$-value of the spacer results in more band lowering of the tunnel-source region. For a given value of $\kappa$, the band lowering is more near the tunneling junction, and the same decreases as one move away from the tunneling junction toward the source. The fringing field in the device is shown in Fig. 4.3 for two different values of $\kappa$ of the spacer. It is evident in Fig. 4.3 that the fringing field in the source near the gate edge is larger for a device with a high-$\kappa$ spacer, as compared with that with a low-$\kappa$ spacer, which confirms that the band lowering, as seen in Fig. 4.2, is indeed due to the fringing field arising out of the spacer. This band lowering results in the formation of depletion zones in the source near the gate edge [52]. It has been suggested in [52] that due to the formation of depletion zones near the surface, the holes are pushed away from the surface toward the body. This causes carrier tunneling to occur in the body instead of near the surface that degrades $I_{ON}$ when a high-$\kappa$ spacer is used. It may be noted, however, that the current in a TFET depends upon the tunneling of the electrons from the valence band of the source to the conduction band of the channel and not upon the hole concentration in the source. Again, the device current depends upon the tunnel width and the electric field across the tunneling junction [103], and this has nothing to do with the hole concentration in the source. The fringing field arising out of the spacer dielectric that causes band lowering, as observed in Fig. 4.2, also results in a variation both in the minimum tunnel width and the maximum electric field at the tunneling junction, as can be seen in Fig. 4.4. The minimum value of the tunnel width and the maximum value of the electric field across the tunneling junction in Fig. 4.4 are extracted for $V_{GS} = V_{DS} = 1$ V at two different locations of the channel in the vertical direction: one at a depth of 1 nm below the top oxide—
semiconductor interface and the other at the middle of the channel. It is evident in Fig. 4.4 that the tunnel width and the electric field are, respectively, lower and higher near the surface, as compared with that in the middle of the channel for a low value of \( \kappa \) of the spacer. A crossover is observed for \( \kappa \approx 6 \) above which the tunnel width becomes lower, and the electric field becomes higher at the middle, as compared with that near the surface. This indicates that the tunneling occurs near the surface and at the middle (bulk) of the device, respectively, for the low \((< 6)\) and high \((> 6)\) values of \( \kappa \) of the spacer. It may also be seen in Fig. 4.4 that the minimum tunnel width is less for a low-\( \kappa \) spacer, as compared with that for a high-\( \kappa \) spacer, which explains why degradation of the device performance occurs due to the increasing fringing field arising out of the spacer when its \( \kappa \)-value is increased, as observed in Fig. 4.1.

![Simulated energy band diagram near the tunneling junction at a depth of 1 nm from the oxide-semiconductor interface as a function of the \( \kappa \)-value of the spacer for the device in Fig. 3.1 biased at \( V_{GS} = V_{DS} = 1 \) V.](image)

**Figure 4.2:** Simulated energy band diagram near the tunneling junction at a depth of 1 nm from the oxide–semiconductor interface as a function of the \( \kappa \)-value of the spacer for the device in Fig. 3.1 biased at \( V_{GS} = V_{DS} = 1 \) V.
Figure 4.4: Minimum tunnel width and maximum electric field across the tunneling junction for \( V_{DS} = V_{DS} = 1 \text{ V} \) for different \( K \)-values of the spacer for the device in Fig. 3.1 at two different locations of the channel in the vertical direction: one at a depth of 1 nm below the top oxide–semiconductor interface and the other at the middle of the channel.

We have also studied the spacer \( K \)-value dependence of the TFET characteristics for each of the following cases: when larger silicon body thickness (>10 nm) is used and when HfO\(_2\) is replaced by 1-nm-thick SiO\(_2\) as the gate dielectric. It is found for both cases that the trends of the spacer \( K \)-value dependence of the device characteristics are very similar to that observed in Fig. 4.1, although the impact of
varying the \( \kappa \)-value of the spacer is slightly less when either the silicon body thickness is increased or SiO\(_2\) is used as the gate dielectric instead of HfO\(_2\).

A high-\( \kappa \) spacer in a heterojunction TFET with a SiGe source has already been reported to improve both \( I_{ON} \) and SS, which seems to conflict with our aforementioned findings. To resolve this issue, the typical band diagram in the ON-state, indicating the relative positions of the tunnel-source, the tunnel destination, and the tunnel path, is shown in Fig. 4.5 for a heterojunction TFET with a Si\(_{0.6}\)Ge\(_{0.4}\) source. Both the tunnel-source and the tunnel destination for such a device are located in the narrow-band-gap source region, as evident in Fig. 4.5. A high-\( \kappa \) spacer in such a device therefore causes more band lowering of the tunnel destination adjacent to the gate edge, resulting in a reduction in the tunnel width and an increase in the electric field across the tunneling junction. This in turn causes an improvement in the device performance.

![Simulated energy band diagram near the tunneling junction at a depth of 1 nm from the oxide–semiconductor interface for a heterojunction TFET with a SiGe source biased at \( V_{GS} = V_{DS} = 1 \) V.](image)

**Figure 4.5**: Simulated energy band diagram near the tunneling junction at a depth of 1 nm from the oxide–semiconductor interface for a heterojunction TFET with a SiGe source biased at \( V_{GS} = V_{DS} = 1 \) V.

### 4.2.2 Effects of Variation in the Spacer Width

To study the effects of variation in the spacer width, the same is varied from 0 to 50 nm in steps of 10 nm for a fixed value of \( \kappa \) (corresponding to HfO\(_2\)) of the spacer.
dielectric. The device structure and all other parameters are kept as same as that in the previous case, with 1-nm SiO₂ as the gate dielectric. It is very clear from the transfer characteristics in Fig. 4.6 that \( V_T \) increases, and the device performance degrades with an increasing width of the spacer, although the dependence becomes weak for relatively large widths (≥ 30 nm). It is also observed in Fig. 4.6 that a 0-nm or no spacer results in a better performance. An increase in the width increases the coupling between the gate metal and the source through the spacer, thereby causing degradation in the device performance. After a certain width, the coupling does not increase significantly for further increase in width because of the physical distance, making the device performance less sensitive for larger widths (≥ 30 nm). Similar trends have been observed for a variation of the spacer width when HfO₂ is replaced by SiO₂ as the spacer dielectric, although the impact is much smaller in the case of SiO₂.

![Figure 4.6: Transfer characteristics for \( V_{DS} = 1 \) V for different spacer widths. The inset shows the output characteristics for a gate overdrive voltage of 0.5 V. Hafnium oxide (\( \kappa = 21 \)) as the spacer and 1-nm-thick silicon dioxide as the gate dielectric are used in this case.](image)

4.2.3 Effects of Variation in the Source Doping Concentration

The device structure, as mentioned earlier, with 1-nm-thick SiO₂ as the gate dielectric and a 50-nm-wide spacer is simulated for three different values of the source doping concentration as \( 3 \times 10^{20}, 1 \times 10^{20}, \) and \( 5 \times 10^{19} \) atoms/cm³. For each of
the source doping concentrations, the transfer characteristic is plotted in Fig. 4.7 for two different \( \kappa \)-values of the spacer corresponding to \( \text{SiO}_2 \) and \( \text{HfO}_2 \). In addition to a change in \( V_T \), as expected, it is observed in Fig. 4.7 that variation in the source doping concentration results in a difference in the \( \kappa \)-value dependence of the device characteristics. The dependence of the device characteristics on the \( \kappa \)-value of a spacer decreases with an increasing source doping concentration. Higher source doping causes less depletion of the source and, hence, less band lowering of the tunnel–source. As a result, less impact of the spacer dielectric on the device characteristics is observed for a higher source doping concentration. It may also be noted that the device with a source doping concentration of \( 3 \times 10^{20} \) atoms/cm\(^3\) shows an improved SS for the high-\( \kappa \) spacer, as compared with that for the low-\( \kappa \) spacer. It has been verified that, this is due to band narrowing of the source for such high doping concentrations that has, to some extent, a similar effect of using a lower band-gap material such as SiGe in the source, as discussed earlier.

![Figure 4.7: Transfer characteristics showing the impact of different source doping concentrations on the spacer \( \kappa \)-value dependence of the device characteristics.](image)

### 4.2.4 Effects of Gate-Source Overlap

The transfer characteristics for a device with a gate–source overlap of 5 nm are compared with that for a device without any gate–source overlap in Fig. 4.8 for two
different κ-values of the spacer corresponding to SiO₂ and HfO₂. Except the overlap, all other device parameters for both the devices are kept as same. Silicon dioxide of 1-nm thick is used as the gate insulator. It is observed from the transfer characteristics in Fig. 4.8 that the spacer dependence of the device characteristics is somewhat reduced for the device with a gate-source overlap, as compared with that without an overlap. Due to the overlap, the fringing field arising out of the spacer dielectric cannot significantly influence the band structure in the part of the source that is covered by the gate. It may be noted that the band lowering of this part of the source adjacent to the tunneling junction mainly influences the tunnel width and, hence, the device current. As the spacer covers the rest of the source, which is away from the tunneling junction, it has less influence on the tunneling parameters. As a result, a reduced dependence of the spacer on the device characteristics is observed for the overlap devices in Fig. 4.8.

![Figure 4.8: Transfer characteristics for Vds = 1 V showing the impact of gate-source overlap on the device characteristics.](image)

**Figure 4.8:** Transfer characteristics for V_{DS} = 1 V showing the impact of gate-source overlap on the device characteristics.

It also may be noted in Fig. 4.8 that for a given spacer, the device current is significantly degraded for the overlap devices, as compared with that without an overlap. The applied gate bias causes the band lowering of the tunnel destination that reduces the tunnel width, making the device-current gate bias dependent, as discussed earlier. For the overlap devices, the applied gate bias also causes the band lowering of
the part of the source that is covered by the gate. Such band lowering of the tunnel–source adjacent to the tunneling junction results in degradation of the device current for the overlap devices, as observed in Fig. 4.8.

4.2.5 Effects of Gate–Channel Underlap

The transfer characteristics for two different devices with 5- and 10-nm gate–channel underlaps are compared with that for a device without any underlap (i.e., for which the gate is exactly aligned with the metallurgical source–channel junction) for two different κ-values of the spacer in Fig. 4.9. All other device parameters are kept as same as that in the previous case. The figure shows that, although a high-κ spacer deteriorates the device performance for a device without an underlap, it actually improves the performance when there is a gate underlap in the device. The amount of improvement for the high-κ spacer over the low-κ spacer for the gate underlap devices increases with an increasing width of the underlap region. It is evident in Fig. 4.10(a) that a high-κ spacer causes more band lowering of the tunnel destination, than that of the tunnel–source, resulting in less tunnel width for such an underlap structure.

![Figure 4.9: Transfer characteristics for \( V_{DS} = 1 \) V showing the impact of gate–channel underlap on the device characteristics.](image)

It is also interesting to observe in Fig. 4.9 that a small gate–channel underlap of 5 nm improves the device performance for a given κ-value of the spacer, particularly
for $V_{OS} < 1$ V. A relatively large gate underlap of 10 nm, however, degrades the
device performance drastically. It is clear in Fig. 4.10(b) that the applied gate bias
causes band lowering not only for the channel region that lie exactly underneath the
gate but also for a part of the source, which is adjacent to the gate edge. The band
lowering of the tunnel–source increases the tunnel width and hence degrades the
device performance to some extent. For a relatively small gate underlap of 5 nm, no
such gate-bias induced band lowering of the tunnel–source is observed in Fig. 4.10(b)
that in turn results in a relatively small tunnel width and, hence, an improved device
performance, as compared with the previous case. No such gate-bias-induced band
lowering of the tunnel–source is also observed for the device with a relatively large
gate underlap of 10 nm. For such devices, however, the applied gate bias can induce
significant band lowering of the channel region, which is away from the tunneling
junction, as can be verified in Fig. 4.10(b). As a result, the tunnel width becomes
significantly larger, which drastically degrades the device performance for the 10-nm
overlap devices, as observed in Fig. 4.9.

Figure 4.10: (a) Simulated energy band diagram near the tunneling junction at a depth of 1
nm from the oxide–semiconductor interface for a 10-nm underlap device biased at $V_{OS} = 0.5$
V and $V_{DS} = 1$ V for two different $k$-values of the spacer. (b) Simulated energy band diagram
near the tunneling junction at a depth of 1 nm from the oxide–semiconductor interface for the
0-, 5-, and 10-nm underlap gate devices biased at $V_{OS} = 0.5$ V and $V_{DS} = 1$ V with the same
spacer dielectric ($k = 3.9$).
4.3 Impact on the Performance of p-TFET

Unless otherwise mentioned, the device structure with dimensions, as shown in Fig. 3.2, is used for the results presented in this section. Gaussian doping profiles with a peak concentration of $1 \times 10^{20}$ atoms/cm$^3$ for the source (n-type) and the drain (p-type) regions, followed by a doping gradient of 2 nm/decade, are used. The intermediate channel region is made of a moderately doped ($1 \times 10^{17}$ atoms/cm$^3$) p-type layer. The doping profile and the location of the metallurgical source-channel junction are shown in Fig. 3.3. The gate contact is made of a metal for which the work function is 5.41 eV. In addition to a nonlocal BTBT model and a band-gap-narrowing model, a quantum density-gradient model is also used.

4.3.1 Effects of Variation in the Gate Dielectric Constant

The purpose of using a high-$\kappa$ gate dielectric in CMOS technology is to achieve lower equivalent oxide thickness (EOT) without enhancing the gate leakage. This is achieved by increasing the $\kappa$ value of the gate dielectric while keeping its physical thickness constant. In doing so, a high-$\kappa$ dielectric induces a higher electrical field at the surface due to the increased oxide capacitance. The impact of such higher electric field at the surface is investigated by keeping the physical thickness of the gate dielectric constant, as done in [11] and [52] for an n-TFET. On the other hand, the fringing field arising out of a high-$\kappa$ gate dielectric causes FIBL [96]. Although such FIBL is known to degrade the performance of a conventional MOSFET [96], [104], it actually helps improve the performance of an n-TFET [50]. The impact of such fringing field arising out of a high-$\kappa$ gate dielectric in a p-TFET is studied by keeping the EOT of the gate dielectric constant, as done in [50] for an n-TFET.

(a) Impact of Fringing Field (Constant EOT)

We first investigate the impact of the fringing field arising out of a high-$\kappa$ gate dielectric by keeping the EOT of the gate dielectric constant. The effects of varying the $\kappa$ value of the gate dielectric on the transfer characteristics at drain-to-source voltage $V_{DS} = -1$ V of the p-TFET, as shown in Fig. 3.2, with a drawn gate length $L_g = 50$ nm and EOT = 2 nm, are shown in Fig. 4.11(a). No spacer is used in this case.
The \( k \) values of the gate dielectric used are 3.9, 7.5, 21, 50, 100, and 200. The values of threshold voltage \( V_T \) and \( I_{ON} \) for different \( k \) values of the gate dielectric are extracted from the transfer characteristics in Fig. 4.11(a) and are plotted in Fig. 4.11(b) as a function of the \( k \) value. In this section, the constant current \((10^{-7} \text{ A/\mu m})\) method is used for extracting \( V_T \), and \( I_{ON} \) is assumed to be the value of drain current \( I_D \) corresponding to a gate-to-source voltage \( V_{GS} \) swing of \(-1 \text{ V}\) from the point where the current changes from p-i-n leakage to tunneling. It is observed in Fig. 4.11 that increase in the \( k \) value, except from \( k = 100 \) to 200, results in corresponding degradation of device performance in terms of both \( V_T \) and \( I_{ON} \). An improvement in both \( V_T \) and \( I_{ON} \) is observed for \( k = 200 \), compared with that for \( k = 100 \). This is in contrast with that reported for an n-TFET, where an increase in the \( k \) value of the gate dielectric results in improvement of the device performance [50], except when \( k \) is relatively low. When \( k \) is increased from 3.9 to 21, a deterioration and improvement in \( I_D \) have been reported in [50] for relatively low and high values of \( V_{GS} \), respectively. We have verified that the contrast is not due to the difference in the type (n-channel/p-channel) of TFET structures, but due to the difference in the doping profile. We have also verified that the qualitative results for \( I_{ON} \) presented in this section do not change when the same is extracted at a constant gate overdrive voltage \( V_{OT} = V_{GS} - V_T \).

![Figure 4.11: Impact of varying the \( k \) value of the gate dielectric for the device in Fig. 3.2 with \( L_g = 50 \text{ nm} \) and EOT = 2 nm but without a spacer. (a) Transfer characteristics at \( V_{DS} = -1 \text{ V} \). (b) Variation of \( V_T \) and \( I_{ON} \) with the \( k \) value.](image-url)
The simulated electron energy band diagram for the p-TFET biased at \( V_{GS} = V_{DS} = -1 \text{ V} \) at a distance of 1 nm below the top oxide-semiconductor interface is shown in Fig. 4.12 for different \( \kappa \) values of the gate dielectric. The band diagram is shown only around the tunneling junction. In a p-TFET, the BTBT of holes occurs from the source to the channel, resulting in the drain current. This is equivalent to the BTBT of electrons from the valance band of the channel, which is henceforth referred to as the tunnel source, into the conduction band of the source, which is henceforth referred to as the tunnel destination. The potential barrier formed by the band gap of the semiconductor across which the tunneling takes place is henceforth referred to as the tunneling junction. The fringing field arising out of a high-\( \kappa \) dielectric causes fringe-induced barrier lowering for an n-channel device [96]. In contrast, it is observed in Fig. 4.12 that the bands are pushed up in energy when the \( \kappa \) value of the gate dielectric is increased in the case of a p-TFET, which is simply due to the use of opposite polarity (negative) of the gate bias in such devices. The fringing field in the device is shown in Fig. 4.13 for two different \( \kappa \) values of the gate dielectric, corresponding to SiO\(_2\) and HfO\(_2\). It is observed in Fig. 4.13 that the fringing field in the source near the gate edge is larger for a device with a high-\( \kappa \) gate dielectric, compared with that with a low-\( \kappa \) dielectric. As a result, as evident in Fig. 4.12, the impact of the fringing field is found to be larger near the gate edge than the rest of the device. It is also evident in Fig. 4.12 that, when the \( \kappa \) value is increased from 3.9 to 100, the amount by which the energy bands are pushed up, which is henceforth referred to as the impact of fringing field, becomes larger for the tunnel destination than that for the tunnel source. This results in a larger value of the minimum tunnel width and a correspondingly smaller value of the maximum electric field across the tunneling junction, when the \( \kappa \) value of the gate dielectric is increased from 3.9 to 100, as can be verified in Fig. 4.14. This, in turn, causes degradation of the device performance for increasing the \( \kappa \) value of the gate dielectric up to \( \kappa = 100 \), as observed in Fig. 4.11. It is also noticed in Fig. 4.12 that an increase in the \( \kappa \) value results in a corresponding shift in the location of the tunneling junction toward the source. Due to a significant shift in the location of the tunneling junction, when the \( \kappa \) value is increased from 100 to 200, the impact of fringing field, which is always
maximum at the gate edge, becomes larger on the tunnel source than that on the
tunnel destination. As a result, an improvement in the device performance is observed
in Fig. 4.11 when the $\kappa$ value is increased from 100 to 200.

Figure 4.12: Simulated energy band diagram near the tunneling junction at a depth of 1 nm
from the oxide–semiconductor interface as a function of the $\kappa$ value of the gate dielectric at
$V_{gs} = V_{ds} = -1$ V.

Figure 4.13: Fringing field plot for the p-TFET biased at $V_{gs} = V_{ds} = -1$ V for two different
$\kappa$ values of the gate dielectric of $\text{EOT} = 2$ nm. (a) $\kappa = 3.9$. (b) $\kappa = 21$. 

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Figure 4.14: Minimum tunnel width and maximum electric field across the tunneling junction for the p-TFET biased at $V_{GS} = V_{DS} = -1$ V for different $\kappa$ values of the gate dielectric of the same EOT.

(b) Impact of Varying the Source Doping

We now see the impact of varying the source doping concentration on the gate-dielectric dependence of the device performance. The device structure, as shown in Fig. 3.2, with $L_g = 50$ nm and EOT = 2 nm but without a spacer, as in the previous case, is simulated for two different values of the source doping concentration as $3 \times 10^{20}$ and $5 \times 10^{19}$ atoms/cm$^3$. For each of the source doping concentrations, the transfer characteristic is plotted in Fig. 4.15 for two different $\kappa$ values of the gate dielectric, corresponding to SiO$_2$ and HfO$_2$. The corresponding energy band diagrams at $V_{QS} = V_{DS} = -1$ V are shown in Fig. 4.16. For a given value of $\kappa$, it is observed in Fig. 4.15 that an increase in the source doping concentration results in corresponding improvement in the device performance, as expected. This is simply due to the fact that a relatively higher source doping not only causes more band lowering of the tunnel destination but it also reduces the source depletion and, hence, less depletion width, as evident in Fig. 4.16. As a result, the minimum value of the tunnel width is reduced, and the maximum electric field is increased across the tunneling junction. It is, however, interesting to note that, in Fig. 4.15, a relatively lower source doping reduces the gate-dielectric dependence of the device performance, which is in contrast to that intuitively expected. This can be attributed to the combined influence of the
following two: First, a decrease in the source doping concentration results in corresponding shift in the location of the tunneling junction toward the source, which is due to larger source depletion for lower source doping, as evident in Fig. 4.16. Second, a larger impact of the fringing field arising out of the gate dielectric is observed at the gate edge than the rest of the device, as can also be verified in Fig. 4.16. As a result, for a device with higher source doping, the impact of the fringing field across the tunneling junction is found to be much larger on the tunnel destination, compared with that on the tunnel source. This, in turn, results in significant widening of the tunnel width, thereby degrading the device performance drastically. In contrast, due to a shift in the location of the tunneling junction toward the source for a device with lower source doping, the impact of the fringing field on the tunnel source partly compensates its impact on the tunnel destination. As a result, the gate-dielectric dependence of the device characteristics is somewhat reduced when a relatively lower source doping concentration is used.

**Figure 4.15:** Transfer characteristics at $V_{DS} = -1$ V showing the impact of varying the source doping concentration on the gate-dielectric dependence of p-TFET characteristics. No spacer is used in this case. The EOT of the gate dielectric is kept constant at 2 nm.
Figure 4.16: Impact of varying the source doping concentration on the simulated energy band diagram near the tunneling junction of the p-TFETs with different gate dielectrics biased at $V_{GS} = V_{DS} = -1$ V.

(c) Impact of Device Scaling

The impact of device scaling on the gate-dielectric dependence of p-TFET characteristics is now investigated. For this purpose, device simulation is done for two different p-TFETs: one with $L_g = 100$ nm and $EOT = 4$ nm and the other with $L_g = 30$ nm and $EOT = 1$ nm. All other device dimensions and parameters are kept the same as in the previous case. Fig. 4.17 shows the plot of $V_T$ and $I_{ON}$ as a function of the $\kappa$ value of the gate dielectric for the device with $L_g = 30$ nm and $EOT = 1$ nm, whereas the inset of Fig. 4.17 shows the plot for the device with $L_g = 100$ nm and $EOT = 4$ nm. It is evident in Fig. 4.17 that the qualitative nature of the impact of fringing field does not change with dimension scaling. An increase in $\kappa$ value, except from $\kappa = 100$ to 200, results in corresponding degradation of the device performance in terms of both $V_T$ and $I_{ON}$ for both the devices, similar to that observed in Fig. 4.11(b) for a device with $L_g = 50$ nm and $EOT = 2$ nm. In addition, an improvement in both $V_T$ and $I_{ON}$ is observed for $\kappa = 200$, compared with that for $\kappa = 100$ in Fig. 4.17 for both the devices, similar to that observed in Fig. 4.11(b).

The TFET characteristics are known to be independent of the channel length down to about 20 nm [46], [51], [105]. A careful examination of $I_{ON}$ values in Fig.
4.17, however, reveals that $I_{ON}$ increases with decreasing channel length for a given $\kappa$ value of the gate dielectric. We have verified that such increase in $I_{ON}$ is due to the scaling of the EOT in our devices. $I_{ON}$ has been found to be less sensitive to channel length scaling when the EOT is kept at the same value, which is in consistence with the reported results.

![Figure 4.17: Plot showing the variations of $V_T$ and $I_{ON}$ with the $\kappa$ value of the gate dielectric for a p-TFET with $L_g = 30$ nm and EOT = 1 nm. The inset shows the plot for a p-TFET with $L_g = 100$ nm and EOT = 4 nm.](image)

**Figure 4.17:** Plot showing the variations of $V_T$ and $I_{ON}$ with the $\kappa$ value of the gate dielectric for a p-TFET with $L_g = 30$ nm and EOT = 1 nm. The inset shows the plot for a p-TFET with $L_g = 100$ nm and EOT = 4 nm.

(d) **Impact of Higher Electric Field (Constant Physical Thickness)**

We now investigate the impact of the higher electric field at the surface of a p-TFET, when a high-\(\kappa\) gate dielectric is used in it, by keeping the physical thickness of the gate dielectric constant. For this purpose, device simulation is done for a p-TFET, as shown in Fig. 3.2, with $L_g = 50$ nm, for varying $\kappa$ values of the gate dielectric with a physical thickness of 3 nm. The $\kappa$ values used in this case are 3.9, 7.5, 21, and 29. No spacer is used in this case also, as earlier. The values of $V_T$ and $I_{ON}$ are extracted for different $\kappa$ values of the gate dielectric from the simulated transfer characteristics. Fig. 4.18 shows the plot of $V_T$ and $I_{ON}$ as a function of the $\kappa$ value of the gate dielectric. It is observed in Fig. 4.18 that the device performance is improved, both in terms of $I_{ON}$ and $V_T$, when a high-\(\kappa\) gate dielectric of the same physical thickness is used in a p-TFET. A high-\(\kappa\) gate dielectric of the same physical thickness has larger
oxide capacitance that is expected to increase the tunneling probability as per [11, eq. (4)], which was originally derived in [106] for silicon-on-insulator MOSFETs. To verify it, we plot in Fig. 4.19 the simulated electron energy band diagram around the tunneling junction for the p-TFET biased at $V_{GS} = -0.6$ V and $V_{DS} = -1$ V at a distance of 1 nm below the top oxide–semiconductor interface for different $\kappa$ values of the gate dielectric of the same physical thickness. Increasing the $\kappa$ value of the gate dielectric, of the same physical thickness, results in higher surface electric field under the gate. As a result, a larger impact of the high-$\kappa$ gate dielectric is observed in Fig. 4.19 for the tunnel source, compared with that for the tunnel destination. This results in better device performance for higher $\kappa$ value of the gate dielectric of the same physical thickness, as observed in Fig. 4.18. It may also be noted that, when the $\kappa$ value of the gate dielectric is increased while keeping its physical thickness constant, the impact of the higher electric field due to increased oxide capacitance, which results in improved device performance, dominates over that of the fringing field, which results in degraded performance, as observed earlier.

![Figure 4.18: $V_T$ and $I_{ON}$ as a function of the $\kappa$ value of the gate dielectric of 3-nm physical thickness for a p-TFET with $L_g = 50$ nm but without a spacer.](image-url)
4.3.2 Effects of Variation in the Spacer Dielectric Constant

The impact of a spacer on the device performance of a p-TFET is studied by varying the $k$ value of the spacer while keeping its width fixed at 50 nm for the device structure, as shown in Fig. 3.2, with $L_s = 50$ nm. A silicon dioxide of 1-nm thickness is used as the gate insulator in this case. The $k$ values of the spacer used are 3.9, 7.5, 21, and 50. The effects of varying the $k$ value of the spacer on the transfer characteristics of the p-TFET are shown in Fig. 4.20. The device characteristic for a p-TFET without a spacer is also shown in Fig. 4.20 for comparison. The values of $V_T$ and $I_{ON}$ are extracted from the transfer characteristics in Fig. 4.20, and plotted in the inset of Fig. 4.20 as a function of the $k$ value of the spacer. It is evident in Fig. 4.20 that an increase in the $k$ value of the spacer results in a corresponding degradation of the device performance, in terms of both $V_T$ and $I_{ON}$, of a p-TFET. This is very similar to that reported in [97] for an n-TFET of similar structure. The simulated electron energy band diagram around the tunneling junction of the p-TFET biased at $V_{GS} = V_{DS} = -1$ V at a distance of 1 nm below the top oxide-semiconductor interface for different $k$-values of the spacer is shown in Fig. 4.21. The impact of the fringing...
field arising out of the spacer is expected to be larger for the source (tunnel
destination) than that for the channel (tunnel source) for such a p-TFET structure. So,
a careful look across the tunneling junction of Fig. 4.21 reveals that the amount by
which the energy bands are pushed up becomes larger for the tunnel-destination, as
compared with that for the tunnel-source, when the $K$-value of the spacer is increased.
This results in larger value of the minimum tunnel width across the tunneling
junction. This in turn causes degradation of the device performance when the $K$-value
of the spacer is increased, as observed in Fig. 4.21. It may also be noticed in Fig. 4.21
that, for increasing the $K$-value of the spacer, the source depletion increases, which
shifts the location of the tunneling junction more towards the source.

Figure 4.20: Impact of varying the $K$ value of the spacer on the transfer characteristics for the
device in Fig.3.2 with $L_g = 50$ nm. The inset shows the variations of $V_T$ and $I_{OX}$ with the $K$
value of the spacer. Silicon dioxide of 1-nm thickness is used as the gate dielectric in this
case.
Figure 4.21: Simulated energy band diagram near the tunneling junction at a depth of 1 nm from the oxide-semiconductor interface as a function of the $k$-value of the spacer for $V_{GS} = V_{DS} = -1$ V.

The impact of varying the source doping concentration on the spacer dependence of the device performance is also investigated. The device structure, as shown in Fig. 3.2 with 1-nm-thick SiO$_2$ as gate insulator, is simulated for two different values of the source doping concentration as 3x10$^{20}$ and 5x10$^{19}$ atoms/cm$^3$. For each of the source doping concentrations, the transfer characteristic is plotted in Fig. 4.22 for two different $k$-values of the spacer, corresponding to SiO$_2$ and HfO$_2$. The corresponding energy band diagrams for $V_{GS} = V_{DS} = -1$ V are shown in Fig. 4.23. It is evident in Fig. 4.22 that a relatively higher source doping reduces the spacer dependence of the device characteristics, which is in consistent with that reported for an n-TFET [97]. This is, however, in contrast with the impact of source doping on the gate-dielectric dependence of the p-TFET characteristics, as observed in the previous sub-section. It is evident in Fig. 4.23 that the impact of the fringing field is more on the tunnel-destination than that on the tunnel-source. A relatively higher source doping not only causes correspondingly less source depletion, but it also reduces the impact of fringing field. Hence, a reduced dependence of the device characteristics on the spacer is observed for a device with higher source doping concentration, as observed in Fig. 4.22.
Figure 4.22: Transfer characteristics for $V_{DS} = -1V$, showing the impact of varying the source doping concentrations on the spacer dependence of p-TFET characteristics. Silicon dioxide of 1-nm thickness is used as the gate dielectric in this case.

Figure 4.23: Impact of varying the source doping concentration on the simulated energy band diagram near the tunneling junction of the p-TFETs with different spacers biased at $V_{DS} = V_{DS} = -1V$. 

$\text{Energjr (eV)}$

$-1.0 \quad -0.8 \quad -0.6 \quad -0.4 \quad -0.2 \quad 0.0 \quad 0.2$ 

Gate voltage (V)

$1 \times 10^{-4}$

$1 \times 10^{-6}$

$1 \times 10^{-8}$

$1 \times 10^{-10}$

$1 \times 10^{-12}$

$1 \times 10^{-14}$

$1 \times 10^{-16}$

$1 \times 10^{-18}$

Drain current (Amp/\mu m)

$V_{DS} = -1V$

$-k=3.9, N_D=3 \times 10^{20}$

$-k=3.9, N_D=5 \times 10^{19}$

$-k=21, N_D=3 \times 10^{20}$

$-k=21, N_D=5 \times 10^{19}$

$L=3.9, N_D=3 \times 10^{20}$

$L=3.9, N_D=5 \times 10^{19}$

$L=21, N_D=3 \times 10^{20}$

$L=21, N_D=5 \times 10^{19}$

$L=0.08 \quad 0.09 \quad 0.10 \quad 0.11 \quad 0.12$

Lateral distance (\mu m)

$0.12$

$1x10
1x10
1x10
lxlO"lo'i
1x10
lx 10"161
1x10
IxlO"121 

$\text{Energy (eV)}$

$-1.0 \quad -0.5 \quad 0.0 \quad 0.5 \quad 1.0 \quad 1.5 \quad 2.0$

$\text{Metalurgical junction}$

$\text{Transfer characteristics for $V_{DS} = -1V$, showing the impact of varying the source doping concentrations on the spacer dependence of p-TFET characteristics. Silicon dioxide of 1-nm thickness is used as the gate dielectric in this case.}$

$\text{Impact of varying the source doping concentration on the simulated energy band diagram near the tunneling junction of the p-TFETs with different spacers biased at $V_{DS} = V_{DS} = -1V$.}$
4.3.3 Effects of Gate-Source Overlap

In order to study the impact of a gate-source overlap on the device performance of a p-TFET, the device simulation is done for two different devices, which are very similar to that shown in Fig. 3.2, except with gate-source overlaps of 5- and 10-nm. The doping profile and the location of the metallurgical junction are kept as same, as shown in Fig. 3.3. Silicon dioxide is used both as the gate dielectric and the spacer in this case. Their transfer characteristics are compared with that for a device without an overlap in Fig. 4.24. Except the overlap, all other device parameters for all the devices are kept as same. It is observed from the transfer characteristics in Fig. 4.24 that the device performance is degraded for the devices with gate-source overlaps, as compared with that without an overlap. The amount of degradation is, however, smaller for the 10-nm overlap device than that for the 5-nm overlap one. In order to get an insight, the simulated energy band diagram for \( V_{GS} = V_{DS} = -1 \) V is shown in Fig. 4.25 for all the three devices. It is clearly seen in Fig. 4.25 that a gate overlap causes a step-like change in energy around the gate edge, which is due to the depletion of holes in the part of the source that is covered by the gate. Such source depletion increases the tunnel width that in turn degrades the device performance for the overlap devices as observed in Fig. 4.24. Also, as the fringing field has maximum impact at the gate edge, and, as the physical distance of the gate edge from the tunneling junction increases for increasing the gate-source overlap, the impact of the fringing field on the tunnel destination is found to be reduced for the 10-nm overlap device, as compared with that for the 5-nm overlap device, as can be clearly seen in Fig. 4.25. This results in less degradation of the device performance when the gate-source overlap is increased, as observed in Fig. 4.24.
4.3.4 Effects of Gate-Channel Underlap

The transfer characteristics for three different p-TFETs with 2-, 5-, and 10-nm gate-channel underlaps are compared with that for a device without any underlap in...
Fig. 4.26. The doping profile and the location of the metallurgical junction for all the devices have been kept as same, as shown in Fig. 3.2. Silicon dioxide is used both as the gate dielectric and the spacer in this case also. It is evident in Fig. 4.26 that a small gate-channel underlap of 2 nm improves the device performance in terms of both $S$ and $I_{ON}$. Performance is, however, degraded for relatively large gate underlaps; with a drastic degradation for the 10-nm underlap device. In order to get an insight, the energy band diagram is shown in Fig. 4.27 for the 0-, 2-, 5-, and 10-nm gate underlap devices for $V_G = V_D = -1V$. It is clear in Fig. 4.27 that the source depletion decreases for increasing the gate underlap resulting in reduction in the amount by which the energy bands are pushed up for the tunnel destination. This reduces the tunnel width for a device with a small underlap of 2 nm, which in turn results in improvement in the device performance, as observed in Fig. 4.26. Also, a corresponding shift in the location of the tunneling junction towards the channel for increasing the underlap is observed in Fig. 4.27. Due to this, the amount by which the energy bands of the tunnel-source are pushed up decreases for increasing the gate underlap. As a result, the tunnel width becomes larger for the devices with relatively large gate underlap resulting in degradation of the device performance, as observed in Fig. 4.26. It may be mentioned here that a similar trend in results of the gate underlap has been observed for a p-TFET in which no spacer is used.

![Figure 4.26: Transfer characteristics for $V_{DS} = -1V$, showing the impact of a gate-channel underlap on the p-TFET characteristics. Silicon dioxide is used both as the gate dielectric and the spacer.](image-url)
4.4 Summary

For an n-TFET, it is found [97] that a low-κ dielectric as a spacer with minimum possible width produces the best device performance. High source doping or a gate-source overlap reduces the spacer dependence of the device characteristics for n-TFET. A gate underlap n-TFET structure with a high-κ spacer in it shows improved performance. For a given spacer, although a gate overlap or a relatively large gate underlap degrades the device performance of n-TFET, a small gate underlap shows an improvement in it.

The fringing field arising out of a high-κ gate dielectric has been found [102] to deteriorate the performance of a p-TFET. It has also been found [102] that the fringing field arising out of a high-κ gate dielectric has greater impact for a p-TFET with higher source doping concentration. The qualitative nature of the impact of fringing field has been found to be independent of dimension scaling. The impact of a spacer on a p-TFET, however, has been found to be very similar to that on an n-TFET of similar structure. It is also found that, although a gate overlap or a relatively large...
gate underlap degrades the device performance, a small gate underlap shows an improvement in it for a p-TFET, very similar to that for an n-TFET of similar structure.

Recently, Vandooren et al. [107] have reported that existence of defects/traps at the tunneling junction deteriorates the performance, particularly for Si TFETs. Non-incorporation of trap-assisted tunneling (TAT) model may, therefore, overestimate the current levels. But, this should not have much impact on our findings, as the focus of our whole work is not on the exact values of either the current or the device performance parameters but more on the general trends and relative results due to different device electrostatics arising out of the variation in different structural parameters of the device.