Chapter-7

Reduced Common Mode Voltage PWM Algorithms for Direct Torque Controlled Induction Motor Drives

7.1 Introduction:

Though the SVPWM algorithm reduces harmonic distortion in line current of the induction motor, it generates large common mode voltage variations, which is also known as electromagnetic interference (EMI). The PWM algorithm requires high speed switching devices like IGBTs to increase the switching frequency of VSI-PWM inverters, which in turns leads to better performance characteristics. However, the high speed of variation of the voltage (dv/dt) exerted by such power devices produces high frequency oscillatory common mode voltages (common mode currents) at every switching instant.

These oscillatory currents radiate electromagnetic interference (EMI) noises throughout producing a bad effect on electronic devices such as amplitude modulation (AM) radio receivers, medical equipments communication systems. Steep voltage pulses also pose threats to the motor. Because of the transmission line effect in the motor cable, voltage and current waves propagate at a finite velocity in the cable, and reflect from the impedance discontinuities at the motor terminals and the
converter output. A superposition of the reflected voltages at the motor terminals may result in over voltages possibly causing a failure in the stator winding insulation of the motor. A common-mode voltage is present in the output voltage of the frequency converter. This voltage may cause bearing currents in the motor. Bearing currents generate bearing wear in the form of pitting, frosting, and spark tracks at the surfaces of the bearing balls and races. The bearings may fail prematurely because of the additional friction and the polluted lubricant in the bearing.

Moreover, an increase in the carrier frequency of PWM inverters results in a non negligible amount of high frequency leakage current which may cause a serious problem. It would flow through stray capacitors between stator windings and a motor frame due to a large step change of the common mode voltage produced by a PWM inverter. The peak value may reach the rated current in the worst case. It may have an undesirable influence on the motor current control and may result in incorrect operation of residual current operated circuit breakers. Many studies for reducing the common mode voltage have been made. These studies, however, have focused on the utilization of additional hardware such as various types of inverter output filters and an active cancellation using switching devices. Since these methods require extra hardware, the drawbacks of an increase in inverter weight and volume or complexity in its control are unavoidable.
Recently various common mode voltage reduction methods using a PWM scheme have been proposed in the literature. The PWM schemes are based on space vector approach and can be of symmetrical or asymmetrical. Moreover, they do not use any zero voltage vectors which are cause of high common mode voltage. In case of asymmetrical PWM technique the switching number inside the sector is not the same and switching pattern is not symmetrical as in conventional SVPWM method and hence increases current disturbance. In case of symmetrical space vector based PWM technique though the switching pattern is symmetrical and number of switchings within the sector remains the same as in conventional SVPWM, but the number of switchings from one sector to the next is more and hence switching losses increases.

In this chapter, few simplified space vector based PWM algorithms have been proposed for direct torque controlled induction motor drives to reduce the common mode voltage. These PWM algorithms are also known as reduced common mode voltage PWM (RCMVPWM) algorithms. As the proposed RCMVPWM algorithms are developed based on the concept of imaginary switching times, the computational burden involved in the algorithms can be decreased.

**7.2 Common Mode Voltage:**

The common mode voltage is the potential of the star point of the load with respect to the center of the dc bus of the VSI. Fig 7.1 shows a
VSI fed induction motor. A set of phase voltage equations can be written as given in (7.1).

\[
\begin{align*}
V_{an} &= V_{so} - V_{ao} \\
V_{bn} &= V_{so} - V_{bo} \\
V_{cn} &= V_{so} - V_{co}
\end{align*}
\] (7.1)

where \( V_{ao}, V_{bo}, V_{co} \) are inverter pole voltages and \( V_{so} \) is common mode voltage.

Adding the set of equations of (7.1) and since \( V_{an} + V_{bn} + V_{cn} = 0 \), the common mode voltage in the motor is given by

\[
V_{com} = V_{so} = \frac{V_{ao} + V_{bo} + V_{co}}{3}
\] (7.2)

Hence, if the drive is fed by balanced three phase supply, the common mode voltage is zero. But, the common mode voltage exists inevitably when the drive is fed from an inverter employing PWM technique because the VSI cannot produce pure sinusoidal voltages and has discrete output voltages. It can be shown that the switching state and dc bus voltage
decides the common mode voltage. There are eight available output voltage vectors in accordance with the eight different switching states of the inverter as depicted in Fig. 7.2.

\[ V_{com} = V_{so} = \frac{V_{dc}}{3} (S_a + S_b + S_c) - \frac{V_{dc}}{2} \]  

(7.3)

where \( S_a \), \( S_b \) and \( S_c \) denotes the switching states of each phase.

The common mode voltage for each inverter state is given in Table 7.1, which shows that, if only even or only odd voltage vectors are used, no common mode voltage variation is generated. If a transition occurs from an even voltage vector to an odd one (or vice versa), a common mode variation of amplitude \( V_{ac}/3 \) is generated. If a transition from an odd (even) voltage vector to the zero (seventh) voltage vector occurs, a
common variation $V_{dc}/3$ is generated. If a transition from an odd (even) voltage vector to the seventh (zero) voltage occurs, a common-mode variation of amplitude $2V_{dc}/3$ is generated. Finally, if a transition occurs from zero to seventh or vice versa, a common mode variation of amplitude $V_{dc}$ is generated.

**Table 7.1 Common mode voltage and output voltage generated by a switching state**

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Inverter pole voltages</th>
<th>$V_{com}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{ao}$</td>
<td>$V_{bo}$</td>
</tr>
<tr>
<td>$V_0 (0\ 0\ 0)$</td>
<td>$-\frac{V_{dc}}{2}$</td>
<td>$-\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_1 (1\ 0\ 0)$</td>
<td>$\frac{V_{dc}}{2}$</td>
<td>$-\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_2 (1\ 1\ 0)$</td>
<td>$\frac{V_{dc}}{2}$</td>
<td>$\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_3 (0\ 1\ 0)$</td>
<td>$-\frac{V_{dc}}{2}$</td>
<td>$\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_4 (0\ 1\ 1)$</td>
<td>$-\frac{V_{dc}}{2}$</td>
<td>$\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_5 (0\ 0\ 1)$</td>
<td>$-\frac{V_{dc}}{2}$</td>
<td>$-\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_6 (1\ 0\ 1)$</td>
<td>$\frac{V_{dc}}{2}$</td>
<td>$-\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>$V_7 (1\ 1\ 1)$</td>
<td>$\frac{V_{dc}}{2}$</td>
<td>$\frac{V_{dc}}{2}$</td>
</tr>
</tbody>
</table>

Therefore, from the point of view of common mode emissions, the worst case is transition between two zero voltage vectors. For this reason whatever inverter control technique is devised, to minimize the generated common mode emissions of the drive, the exploitation of both the null voltage vectors (zero and seventh) should be avoided.
7.3 Reduced Common Mode Voltage PWM Algorithms:

In the application field the problems related to common mode voltage are increasing due to increased PWM switching frequencies aimed at higher efficiency, increased bandwidth, etc. Hence, common mode voltage reduction techniques have been gaining importance. The effect of common mode voltage can be reduced actively or passively. The active common mode voltage reduction method that involves controlling the PWM pulse patterns is the most economical method as it requires no extra components. Recently, several PWM pulse patterns that yield reduced common mode voltage termed as reduced common mode voltage PWM (RCMVPWM) methods have been reported [93-96]. In all these methods, the zero states of the inverter are avoided and results in a common mode voltage of $\pm V_{dc}/6$. All these methods are described using space vector approach.

Based on the choice of the voltage vectors, the RCMVPWM methods will be sub grouped in three types, these include active zero state PWM (AZSPWM) algorithms, remote state PWM (RSPWM) algorithms and near state PWM (NSPWM) algorithm. In the AZSPWM algorithms, the conventional active (adjacent) voltage vectors are complemented with either two near opposing active vectors or one of the adjacent states and its opposite vector with equal time to effectively create a zero-voltage vector. The RSPWM methods synthesize the output voltage from three inverter voltage vectors that are 120° apart from each other (most remote
vectors). The NSPWM method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. But, this thesis mainly deals with only AZSPWM and NSPWM algorithms.

In the AZSPWM algorithms, the vector transformation yields six active and two zero vectors for the inverter, and as shown in Fig. 7.3 (a), the vectors divide the space into six segments as in SVPWM algorithm. These regions are utilized in programming the PWM pulses. But, in the NSPWM algorithm 30° phase-shifted regions are utilized as shown in Fig. 7.3 (b).

In the space vector approach, the duty cycles of the voltage vectors are calculated according to the vector volt-seconds balance rule. The voltage vectors and their sequences are selected based on a specified performance criterion such as the minimum output voltage ripple and switching count and the vectors are programmed accordingly. The formation of AZPWM and NSPWM algorithms is illustrated in Fig. 7.4 – Fig. 7.5. In each PWM method, with a specific performance optimization criterion, the voltage vectors are selected, and their sequences depend on the region of the reference voltage vectors defined in Fig. 7.3(a) and (b). The utilized voltage vectors and their sequences for the conventional SVPWM and RCMVPWM methods are given in Table 7.2.
Fig. 7.3 Voltage space vectors and 60° sector definitions

Fig. 7.4 Voltage space vectors and formation of AZSPWM algorithms
In the conventional SVPWM method, two adjacent states with two zero voltage vectors are utilized to program the output voltage. Every 60° degrees the active voltage vectors change, but the zero state locations are retained. In the AZSPWM methods, the choice and the sequence of active voltage vectors are the same as in conventional SVPWM. However, instead of the real zero voltage vectors ($V_0$ and $V_7$), two active opposite voltage vectors with equal duration are utilized. Here, three choices exist. For AZSPWM algorithms, any of the pairs $V_1$-$V_4$, $V_2$-$V_5$, or $V_3$-$V_6$ can be
utilized.

The NSPWM employs only three neighbor voltage vectors and sequences them in the order that the minimum switching count is obtained. Thus, one of the phases is not switched within each PWM cycle. The resulting vector sequence is shown in Table 7.2. For example, for the region between -30° and +30° (sector B₁), the applied voltage vectors are $V_1$, $V_2$, and $V_6$ with the sequence $V_6-V_2-V_1-V_1-V_2-V_6$. In the NSPWM algorithm, in each sector any one of the phases is clamped to either positive or negative DC bus for a total of 120° over a fundamental cycle. Hence, it reduces the switching losses of the inverter and switching frequency of the inverter by 33.33%.

For each one of the above described PWM methods and its pulse pattern, a unique common mode voltage pattern results. The conventional SVPWM method has common mode voltage (CMV) that can be as high as ±Vdc/2. On the other hand, all the RCMVPWM methods have ±Vdc/6 CMV magnitude value. The frequency and polarity of CMV of each RCMVPWM method is unique and each of these pulse patterns may be attractive for a specific application. All the above existing RCMVPWM algorithms use the conventional space vector approach, which requires angle and sector information. Hence, to reduce the complexity involved in the existing RCMVPWM algorithms, the proposed RCMVPWM algorithms have been proposed by using the concept of imaginary switching times.
7.3.1 Calculation of Switching Times for AZSPWM Algorithms:

To reduce the complexity involved in the existing AZSPWM algorithms, in this chapter, the proposed AZSPWM have been developed by using the notion of imaginary switching times. The concept of imaginary switching times has already explained in chapter 3 in detail. In this approach, the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages are calculated as given in (7.4)

\[
T_{an} = \left( \frac{T_s}{V_{dc}} \right) V_{an} ; \quad T_{bn} = \left( \frac{T_s}{V_{dc}} \right) V_{bn} ; \quad T_{cn} = \left( \frac{T_s}{V_{dc}} \right) V_{cn} \quad (7.4)
\]

To calculate the active vector switching times, the maximum, middle and minimum values of imaginary switching times are calculated in every sampling time as given in (7.5) – (7.7).

\[
T_{\text{max}} = \text{Max}(T_{an}, T_{bn}, T_{cn}) \quad (7.5)
\]
\[
T_{\text{mid}} = \text{Mid}(T_{an}, T_{bn}, T_{cn}) \quad (7.6)
\]
\[
T_{\text{min}} = \text{Min}(T_{an}, T_{bn}, T_{cn}) \quad (7.7)
\]

Then the active vector switching times \( T_1 \) and \( T_2 \) may be expressed as

\[
T_1 = T_{\text{max}} - T_{\text{mid}} \quad ; \quad T_2 = T_{\text{mid}} - T_{\text{min}} \quad (7.8)
\]

The zero voltage vectors switching time is calculated as

\[
T_z = T_s - T_1 - T_2 \quad (7.9)
\]

Then, the zero voltage vector time is shared equally among the two opposite active voltage vectors to create effectively a zero voltage vector. Then, by utilizing the space vector approach, the possible switching
sequences, can be derived. However, this thesis presents two cases of AZSPWM algorithms for which the sequences are illustrated in Table 7.2.

### 7.3.2 Generation of Pulse Pattern for NSPWM Algorithm:

#### 7.3.2.1 Conventional Approach:

The near state PWM (NSPWM) algorithm uses a group of three neighbor voltage vectors to construct the reference voltage vector. In order to reduce the common mode voltage variations, the proposed NSPWM algorithm did not use the zero voltage vectors. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors are utilized in each sector as shown in Fig 7.5. Hence, the utilized voltage vectors are changed in every sector. As shown in Fig. 7.5, to apply the method, the voltage vector space is divided into six sectors. Here also, as all six sectors are symmetrical, the discussion is limited to the first sector only. For the required reference voltage vector, the active voltage vectors ($V_1$, $V_2$ and $V_6$) times can be calculated as in (7.10), (7.11) and (7.12) [93-96].

\[
T_1 = \left\{-1 + \frac{3}{\pi} M_i \cos(\alpha + \frac{\pi}{3}) + \frac{3\sqrt{3}}{\pi} M_i \sin(\alpha + \frac{\pi}{3})\right\} T_s \tag{7.10}
\]

\[
T_2 = \left\{1 - \frac{3}{\pi} M_i \cos(\alpha + \frac{\pi}{3}) - \frac{3\sqrt{3}}{\pi} M_i \sin(\alpha + \frac{\pi}{3})\right\} T_s \tag{7.11}
\]

\[
T_6 = T_s - T_1 - T_2 \tag{7.12}
\]

But, in the NSPWM algorithm, the (7.10), (7.11) and (7.12) have a valid solution when the modulation index is varying between 0.61 and 0.906
In order to get minimum switching frequency and reduced common mode voltage the NSPWM algorithm uses 216-612 in sector-I, 321-123 in sector-II and so on.

**7.3.2.2 Proposed Approach:**

As the existing NSPWM algorithm uses conventional space vector approach, the complexity involved in the algorithm is more. To simplify the algorithm, proposed NSPWM algorithm is developed by using the notation of imaginary switching times. The modulating waveform of NSPWM algorithm is similar to the discontinuous PWM 1 (DPWM1) algorithm as explained in [93-96]. The modulating waveform can be generated by using the concept of imaginary switching times as given below:

The imaginary switching time periods, which are proportional to the instantaneous values of the reference phase voltages, are calculated from (7.4). Then the maximum and minimum values can be calculated by using (7.5) and (7.7). Then, the effective time during which the induction motor is effectively connected to the source (that is the power will be transferred to the motor from source) can be calculated as given in (7.13).

\[ T_{\text{eff}} = T_{\text{max}} - T_{\text{min}} \]  

(7.13)

When the actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which the effective time can be relocated anywhere within the sampling time period.
Therefore, the actual switching times for each inverter leg can be obtained by the time shifting operation as follows:

\[ T_{ga} = T_{an} + T_{offset} \]  
\[ T_{gb} = T_{bn} + T_{offset} \]  
\[ T_{gc} = T_{cn} + T_{offset} \]  

(7.14) \hspace{1cm} (7.15) \hspace{1cm} (7.16)

To guarantee the full utilization of dc-link voltage of the inverter, the actual switching times should be restricted to a value from 0 to \( T_s \).

To generate the modulating waveforms of NSPWM algorithm, the procedure is as follows:

If the A-phase reference voltage is positive (or negative) and has maximum magnitude, the A-phase switch should be fixed to the ON (or OFF) state. That is to say,

\[
\begin{align*}
\text{if } T_{\text{max}} + T_{\text{min}} < 0 & \Rightarrow T_{\text{max}} + T_{\text{offset}} = T_s \\
\text{if } T_{\text{max}} + T_{\text{min}} \geq 0 & \Rightarrow T_{\text{min}} + T_{\text{offset}} = 0
\end{align*}
\]  

(7.17)

Therefore, the time shifting value \( T_{\text{offset}} \) is

\[
\begin{align*}
\text{if } T_{\text{max}} + T_{\text{min}} < 0 & \Rightarrow T_{\text{offset}} = -T_{\text{min}} \\
\text{if } T_{\text{max}} + T_{\text{min}} \geq 0 & \Rightarrow T_{\text{offset}} = T_s - T_{\text{max}}
\end{align*}
\]  

(7.18)

Then, the modulating waveforms of NSPWM algorithm can be synthesized using the calculated gating times by using (7.19).

\[ V_{in}^* = \frac{V_{dc}}{2} \left( \frac{2 \cdot T_{gi}}{T_s} - 1 \right) \quad i = a, b, c \]  

(7.19)

The modulating waveforms of NSPWM and DPWM1 algorithm are
exactly the same [93-96] and Fig 7.6 shows the waveforms of offset time, gating time and modulating signal of NSPWM algorithm.

![Waveform Diagrams](image)

Fig 7.6 waveforms of (a) actual gating time ($T_{ga}$) and offset time ($T_{offset}$) (b) Modulating wave

The total number of commutations in SVPWM algorithm is three in a sampling time interval, where as the number of commutations in NSPWM algorithm is two. Moreover, from the modulating waveform of NSPWM algorithm, it can be observed that any one of the phases is clamped to the either positive or negative DC bus for utmost a total of
120° over a fundamental cycle. Hence, the switching losses of the associated inverter leg are eliminated. Hence, the switching frequency of the NSPWM algorithms is reduced by 33% compared with SVPWM algorithm. This implies that if one wants to keep the average switching frequency constant, whenever NSPWM algorithm is used, sampling frequency must be increased by \( \frac{3}{2} \) times. However, in NSPWM algorithm instead of one carrier wave, two carrier waves \( (V_{\text{tri}} \text{ and } -V_{\text{tri}}) \) must be utilized. The choice of the triangle to be compared with the modulation signals is region dependent. If slope of the reference phase voltage is positive then the modulating waveform is compared with \( V_{\text{tri}} \) and if slope of the reference phase voltage is negative then the modulating waveform is compared with \( -V_{\text{tri}} \). General switching rule is that if the modulating waveform is larger than the carrier signal (triangular wave), the upper switch associated with the specific phase is set “on”. The reference phase voltages are as shown in Fig 7.7 in all the six sectors.

From Fig 7.7, it can be observed that in the first sector the slope of a- and b-phase voltages is positive, whereas the slope of c-phase voltage is negative. Hence, in the first sector, the modulating waveforms of a-phase and b-phase are compared with \( V_{\text{tri}} \) and modulating wave of c-phase is compared with \( -V_{\text{tri}} \) as shown in Fig 7.8. The possible pulse pattern for the first sector is also shown in Fig 7.8.
7.4 Proposed RCMVPWM Algorithms Based Direct Torque Controlled Drive:

The reference voltage space vector can be constructed in many ways. But, to reduce the complexity of the algorithm, in this thesis, the required reference voltage vector, to control the torque and flux cycle-by-cycle basis is constructed by using the errors between the reference d-
axis and q-axis stator fluxes and d-axis and q-axis estimated stator fluxes sampled from the previous cycle. The block diagram of the proposed RCMVPWM based DTC is as shown in Fig. 7.9. From Fig. 7.9, it is seen that the proposed RCMVPWM based DTC scheme retains all the advantages of the CDTC, such as no coordinate transformation, robust to motor parameters, etc. However, a space vector modulator is used to generate the pulses for the inverter, therefore the complexity is increased in comparison with the CDTC method.

In the proposed method, the position of the reference stator flux vector $\tilde{\psi}_s^*$ is derived by the addition of slip speed and actual rotor speed. The actual synchronous speed of the stator flux vector $\tilde{\psi}_s$ is calculated from the adaptive motor model.

After each sampling interval, actual stator flux vector $\tilde{\psi}_s$ is corrected by the error and it tries to attain the reference flux space vector $\tilde{\psi}_s^*$. Thus the flux error is minimized in each sampling interval. The d-axis and q-axis components of the reference voltage vector can be obtained as follows:

Reference values of the d-axis and q-axis stator fluxes and actual values of the d-axis and q-axis stator fluxes are compared in the reference voltage vector calculator block and hence the errors in the d-axis and q-axis stator flux vectors are obtained as in (7.20)-(7.21).
Fig. 7.9 Block diagram of proposed RCMVPWM based DTC.

\[
\Delta \psi_{ds} = \psi_{ds}^* - \psi_{ds} \tag{7.20}
\]

\[
\Delta \psi_{qs} = \psi_{qs}^* - \psi_{qs} \tag{7.21}
\]

The knowledge of flux error and stator ohmic drop allows the determination of appropriate reference voltage space vectors as given in (7.22)-(7.23).

\[
V_{ds}^* = R_s i_{ds} + \frac{\Delta \psi_{ds}}{T_s} \tag{7.22}
\]

\[
V_{qs}^* = R_s i_{qs} + \frac{\Delta \psi_{qs}}{T_s} \tag{7.23}
\]

Where, \( T_s \) is the duration of subcycle or sampling period and it is a half of period of the switching frequency. This implies that the torque and flux are controlled twice per switching cycle. Further, these d-q components
of the reference voltage vector are fed to the SVPWM block from which, the actual switching times for each inverter leg are calculated.

7.5 Simulation Results and Discussions:

To verify the proposed algorithms, numerical simulation studies have been carried out on a v/f controlled induction motor drive by using Matlab/Simulink. For the simulation, the average switching frequency of the inverter is taken as 3 kHz. The parameters of the induction motor are given in Appendix - I.

The simulation results of common mode voltage variations for SVPWM and RCMVPWM algorithms are given from Fig.7.10 to Fig.7.13. From Fig.7.10 it can be observed that as the SVPWM algorithm uses two zero voltage vectors i.e, \( V_0(000) \) and \( V_7(111) \) in each sampling time interval, the common mode voltage varies from \(-V_{dc}/2\) to \(+V_{dc}/2\). Hence, to reduce the common mode voltage variations, AZSPWM and

![Fig.7.10 Variation of common mode voltage for SVPWM](image-url)
NSPWM algorithms have been proposed in this chapter. As the proposed AZSPWM and NSPWM algorithms do not use the zero voltage vectors, the common mode voltage will vary from $+V_{dc}/6$ to $-V_{dc}/6$ as shown in Fig. 7.11 – Fig. 7.13.

Fig. 7.11 Variation of common mode voltage for AZSPWM1

Fig. 7.12 Variation of common mode voltage for AZSPWM2
Fig. 7.13 Variation of common mode voltage for NSPWM

The simulation results of SVPWM and RCMVPWM based v/f controlled induction motor drive are shown in Fig 7.14 - Fig. 7.17. The harmonic spectra of line currents are also shown in Fig. 7.14 - Fig. 7.17.

From the simulation results, it can be observed that the SVPWM algorithm gives less harmonic distortion with more common mode voltage variations. Whereas, the RCMVPWM algorithms (both AZSPWM and NSPWM) will give reduced common mode voltage variations with increased harmonic distortion.
Fig. 7.14 (a) Steady state plots  (b) Harmonic spectra of line current

for SVPWM at $M_i=0.815$ ($f=45\text{Hz}$)
Fig. 7.15 (a) Steady state plots (b) Harmonic spectra of line current for AZSPWM1 at $M_i=0.815$ (f=45Hz)
Fig. 7.16 (a) Steady state plots (b) Harmonic spectra of line current
for AZSPWM3 at $M_i=0.815$ (f=45Hz)
Fig. 7.17 (a) Steady state plots (b) Harmonic spectra of line current for NSPWM at $M_i=0.815$ (f=45Hz)
The simulation results of proposed AZSPWM1 algorithm based direct torque controlled induction motor drive are shown from Fig 7.18 to Fig 7.29. Fig 7.18 shows the starting transients of speed, torque stator currents and flux in proposed AZSPWM1 algorithm based drive, from which it can be observed that the AZSPWM1 algorithm gives more ripple in starting torque when compared with the SVPWM algorithm. Fig 7.18 shows the no-load starting transients of speed, currents, torque and flux. Fig. 7.19 shows the starting transients in phase and line voltages for AZSPWM1 algorithm based DTC-IM drive. The no-load steady state plots of speed, torque, stator currents, flux, phase and line voltages at 1200 rpm are given in Fig 7.20 -Fig. 7.21. The harmonic distortion in the steady state stator current along with THD value is shown in Fig 7.22. From Fig 7.20 to Fig 7.22, it can be observed that the steady state ripple in torque, flux and current is increased when compared with SVPWM based DTC. The locus of the stator flux is given in Fig 7.23, from which it can be observed that the locus is almost a circle of constant radius. The transients in speed, torque, currents and flux during the step change in load torque and corresponding phase and line voltages are shown in Fig. 7.24 -Fig. 7.25. Also, the transients in speed, torque, currents, flux, and voltages during the speed reversals (from +1200 rpm to -1200 rpm and from -1200 rpm to +1200 rpm) are shown from Fig. 7.26 to Fig. 7.29. The four-quadrant speed-torque characteristic of the proposed drive is shown in Fig. 7.30.
Fig. 7.18 Simulation results of AZSPWM1 based DTC: starting transients.

Fig. 7.19 Starting transients in phase and line voltages for AZSPWM1 algorithm based DTC drive.
Fig. 7.20 Simulation results of AZSPWM1 based DTC: steady-state plots at 1200 rpm.

Fig. 7.21 The phase and line voltages of AZSPWM1 based DTC drive during the steady state operation.
Fig. 7.22 Harmonic Spectrum of stator current along with THD for AZSPWM1 based DTC-IM drive.

Fig. 7.23 locus of stator flux in AZSPWM1 based DTC-IM drive.
Fig. 7.24 Transients during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).

Fig. 7.25 The phase and line voltages of AZSPWM1 based DTC during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).
Fig. 7.26 Transients in speed, torque, current and flux during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).

Fig. 7.27 Transients in phase and line voltages during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).
Fig. 7.28 Transients in speed, torque, current and flux during speed reversal (speed is changed from -1200 rpm to +1200 rpm at 1.35 s).

Fig. 7.29 Transients in phase and line voltages during speed reversal (speed is changed from -1200 rpm to 1200 rpm at 1.35 s).
Fig. 7.30 Speed-torque characteristic of AZSPWM1 based DTC drive in four-quadrants.

Fig. 7.31 Simulation results of AZSPWM2 based DTC: starting transients.
Fig 7.31 shows the no-load starting transients of speed, currents, torque and flux. Fig. 7.32 shows the starting transients in phase and line voltages for AZSPWM2 algorithm based DTC-IM drive.

![Fig. 7.32 Starting transients in phase and line voltages for AZSPWM2 algorithm based DTC drive.](image)

The no-load steady state plots of speed, torque, stator currents, flux, phase and line voltages at 1200 rpm are given in Fig 7.33 - Fig.7.34. The harmonic distortion in the steady state stator current along with THD value is shown in Fig 7.35. From Fig 7.31 to Fig 7.35, it can be observed that the steady state ripple in torque, flux and current is more when compared with SVPWM based DTC. The locus of the stator flux is given in Fig 7.36, from which it can be observed that the locus is almost a circle of constant radius.
Fig. 7.33 Simulation results of AZSPWM2 based DTC: steady-state plots at 1200 rpm.

Fig. 7.34 The phase and line voltages of AZSPWM2 based DTC drive during the steady state operation.
The transients in speed, torque, currents and flux during the step change in load torque and corresponding phase and line voltages are shown in Fig. 7.37 - Fig. 7.38. Also, the transients in speed, torque, currents, flux, and voltages during the speed reversals (from +1200 rpm
Fig. 7.37 Transients during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).

Fig. 7.38 The phase and line voltages of AZSPWM1 based DTC during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).
Fig. 7.39 Transients in speed, torque, current and flux during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).

Fig. 7.40 Transients in phase and line voltages during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).
Fig. 7.41 Transients in speed, torque, current and flux during speed reversal (speed is changed from -1200 rpm to +1200 rpm at 1.35 s).

Fig. 7.42 Transients in phase and line voltages during speed reversal (speed is changed from -1200 rpm to 1200 rpm at 1.35 s).
Fig. 7.43 Speed-torque characteristic of AZSPWM2 based DTC drive in four-quadrants.

Fig 7.43 shows the no-load starting transients of speed, currents, torque and flux. Fig. 7.45 shows the starting transients in phase and line voltages for NSPWM algorithm based DTC-IM drive. The no-load steady state plots of speed, torque, stator currents, flux, phase and line voltages at 1200 rpm are given in Fig. 7.46 - Fig. 7.47. The harmonic distortion in the steady state stator current along with THD value is shown in Fig 7.48. From Fig 7.44 to Fig 7.48, it can be observed that the steady state ripple in torque, flux and current is less compared with AZSPWM based DTC and slightly more when compare with the SVPWM based DTC.
Fig. 7.44 simulation results of NSPWM based DTC: starting transients.

Fig. 7.45 starting transients in phase and line voltages for NSPWM algorithm based DTC drive.
Fig. 7.46 Simulation results of NSPWM based DTC: steady-state plots at 1200 rpm.

Fig. 7.47 the phase and line voltages of NSPWM based DTC drive during the steady state operation.
The locus of the stator flux is given in Fig. 7.49, from which it can be observed that the locus is almost a circle of constant radius. The transients in speed, torque, currents and flux during the step change in load torque and corresponding phase and line voltages are shown in Fig.
7.50 - Fig. 7.51. Also, the transients in speed, torque, currents, flux, and voltages during the speed reversals (from +1200 rpm to -1200 rpm and from -1200 rpm to +1200 rpm) are shown from Fig. 7.52 to Fig. 7.55. The four-quadrant speed-torque characteristic of the proposed drive is shown in Fig. 7.56.

**Fig. 7.50** Transients during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).
Fig. 7.51 The phase and line voltages of NSPWM based DTC during step change in load torque (a 30 N-m load torque is applied at 0.5 s and removed at 0.6s).

Fig. 7.52 Transients in speed, torque, current and flux during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).
Fig. 7.53 Transients in phase and line voltages during speed reversal (speed is changed from +1200 rpm to -1200 rpm at 0.7 s).

Fig. 7.54 Transients in speed, torque, current and flux during speed reversal (speed is changed from -1200 rpm to +1200 rpm at 1.35 s).
Fig. 7.55 Transients in phase and line voltages during speed reversal (speed is changed from -1200 rpm to 1200 rpm at 1.35 s).

Fig. 7.56 Speed-torque characteristic of NSPWM based DTC drive in four-quadrants.
The common mode voltage variations of SVPWM, AZSPWM and NSPWM base DTC are shown in Fig. 7.57- Fig. 7.60, from which it can be observed that the proposed RCMVPWM algorithms will give reduced common mode voltage variations and hence reduce EMI.

Fig. 7.57 Common mode voltage variations in SVPWM base DTC drive

Fig. 7.58 Common mode voltage variations in AZSPWM1 base DTC drive
Fig. 7.59 Common mode voltage variations in AZSPWM2 base DTC drive

Fig. 7.60 Common mode voltage variations in NSPWM base DTC drive
7.6 Summary:

Though the SVPWM based DTC gives less harmonic distortion and steady state ripple, it gives large common mode voltage variations. This will cause EMI problems in the drive systems. Hence, to reduce the EMI problems and to reduce the common mode voltage variations, simplified RCMVPWM algorithms are presented in this thesis. From the results, it can be observed that the proposed RCMVPWM algorithms will give reduce common mode voltage variations with slightly increased ripple and THD. Moreover, among the presented RCMVPWM algorithms, the NSPWM algorithm gives superior performance and also it gives less switching losses of the inverter when compared with the remaining RCMVPWM algorithms.