3.1. Introduction:

It is well known [R-1], [R-2], [S-20] that in a very few restricted class of combinational networks function independent test sets for stuck-at faults exist. For example, AND-EXOR arrays based on the Reed-Muller Canonic (EMC) expansions of switching functions possess universal test sets for detecting stuck-at faults [R-2], [S-20]. Reddy first derived universal test set for detecting single stuck-at faults in such networks [R-2]. One important advantage of this test set is that it has a simple algebraic structure and hence can be generated easily, unlike other combinational circuits in which the process of generating test sets for stuck-at faults is itself very much complex. However, the problem of detecting bridging faults in such networks is yet to be explored. Since, as mentioned earlier, the problem of generating test patterns for detecting bridging faults is highly dependent on circuit topology and is indeed very complex, hence testable designs of logic circuits incorporating bridging faults is always welcome. In this chapter we have proposed easily testable realization of EMC network in which all single stuck-at faults and all bridging faults can be detected by the existing function independent test set for stuck-at faults [R-2].

Before presenting the contribution of this chapter let us discuss a little more about the effect of bridging faults in logic circuits.

As mentioned earlier Mei [M-1] has not considered any bridging fault which involves fanout stem lines or fanout branch lines in a network. Later, Friedman has shown [F-1] that if a bridging fault involves some fanout stem or branch line(s), then the effect of the fault propagates to the other fanout branch lines also through the common parent stem line. In order to explain
Friedman's observation let us consider the network as shown in Fig. 3.1a. Let the two lines k' and l' be shorted. Note that the lines k' and l' are both fanout branch lines connected to the stem lines k and l respectively. Let the other branch line of the stem line k be k" and that of the line l be l". The fault free outputs at 0_1, 0_2 and 0_3 are respectively x, xyz and y, whereas the faulty outputs at 0_1, 0_2 and 0_3 are xy, xyz and xy respectively for AND-type bridging. Thus we see that the effect of the bridging fault propagates also to the output points 0_1 and 0_3 through their respective stem lines k and l. The equivalent faulty network is shown in Fig. 3.1b. The case of OR-type bridging faults can also be explained similarly.

So far, the effect of bridging faults is concerned, one can observe one very interesting effect: faulty acyclic circuits may become sequential due to bridging. This class of bridging faults are called feedback bridging faults. In fact, a feedback bridging fault occurs when both involved lines lie on the same path in the circuit. An example is shown in Fig. 3.1c. Feedback loops are formed by these bridging connections. The resulting circuit may become, therefore, sequential. In some cases, the signal being fed back forces the output to invert its logic level and thus starts oscillation.

However, since in the present thesis we do not consider feedback bridging faults, hence we will not go any further to study the sequential and oscillatory behaviors of combinational circuits under feedback bridge faults.

3.2. Some properties of Reed-Muller Canonical (RMC) expansions of switching functions:

The RMC expansion of any switching function \( f(x_1, x_2, \ldots, x_n) \) is expressed as

\[
f(x_1, x_2, \ldots, x_n) = a_0 \oplus a_1 x_1 \oplus a_2 x_2 \oplus \cdots \oplus a_j x_j \oplus \cdots \oplus a_{2^{n-1}} x_1 x_2 \cdots x_n,
\]
where
1) \( x_j^* = x_j \) or \( \bar{x}_j \) and is fixed for a particular expansion.
2) \( a_o \) = constant term in the expansion; it may be 0 or 1.
3) \( a_j = 0 \) or 1, for \( 1 \leq j \leq 2^{n-1} \)
4) \( j = 2^{j_{1-1}} + 2^{j_{2-1}} + \ldots + 2^{j_{m-1}} \)
5) There are \( 2^n \) possible expansions corresponding to \( 2^n \) possible combinations of \( x_1^*, x_2^*, \ldots, x_n^* \). These expansions are unique for any given function.

The realizations of such expansions of switching functions are known as AND-EXOR arrays based on HMC expansions or simply HMC networks. These arrays may be two dimensional cellular cascades. The vertical cascades consist of a set of AND gates and the horizontal cascade (collector row) consists of a set of EXOR gates. One such realization for a function \( F_o = x_1 \oplus x_1 x_2 \oplus x_2 x_3 x_4 \oplus x_2 x_3 x_4 x_5 \) is shown in Fig. 3.2. A significant saving in logic levels can be achieved if the restriction over the number of inputs to the AND gates is withdrawn. In other words, all the AND gates need not necessarily have the same number of inputs and this number may vary from 2 to \( n \) where \( n \) is the number of variables present in the function realized. This type of realization has notionally two levels only. However, from the point of view of single stuck-at fault detection, the same function independent test set is sufficient in each of the above two realizations. In this chapter we are interested in detecting bridging faults that can occur involving lines in the same level of the network and hence the two level realization described above is the circuit of choice because of its smaller number of levels compared to that of two dimensional cellular cascade realization. Fig. 3.3 shows such a realization for the function \( F_o \).

The following two lemmas follow from some simple observations regarding HMC expansions of switching functions.
Lemma 5.1: Let $P_i$ and $P_j$ be any two product terms in an EMC expansion of a switching function $F_0$. Then there must always be at least one literal which will be present either in $P_i$ but not in $P_j$ or in $P_j$ and not in $P_i$.

Proof: Suppose the claim is not true. Then $P_i$ ($P_j$) has no literal which is present in $P_i$ ($P_j$) only but not in $P_j$ ($P_i$). In other words, $P_i$ and $P_j$ have the same number of literals as well as all the literals in $P_i$ are present in $P_j$ and vice-versa. This leads to the conclusion that $F_0$ is devoid of $P_i$ and $P_j$, since they cancel each other in the EMC expansion, contradicting the assumption that $P_i$ and $P_j$ are two product terms of the EMC expansion of $F_0$. Hence the lemma follows. Q.E.D.

Lemma 5.2: Any two product terms $P_i$ and $P_j$ of an EMC expansion are related to each other by one of the following two relations $R_1$ and $R_2$.

$$R_1: \text{Either } P_i \supseteq P_j, \text{ or } P_i \subseteq P_j$$

$$R_2: P_i \not\equiv P_j, P_i \not\equiv P_j \text{ and } P_i \cap P_j \not\equiv \emptyset \text{ (null)}$$

Proof: Suppose that none of the two relations $R_1$ and $R_2$ holds good in the case of the two product terms $P_i$ and $P_j$ taken. So the only possible relations left are $P_i = P_j$ and $P_i \cap P_j = \emptyset$ (null). The first one is immediately ruled out because otherwise the EMC expansion will be devoid of $P_i$ and $P_j$, contradicting our assumption that $P_i$ and $P_j$ are two of its product terms. The second one can never exist because in any EMC expansion the polarity of the variables is fixed. Hence the lemma follows. Q.E.D.

Definition 5.1: Consider two product terms $P_i$ and $P_j$ in an EMC expansion of an $n$-variable function $F_0$. Then the literal/literals present in $P_i$ and not in $P_j$ and vice-versa is/are called the control literal/literals with respect to $P_i$ and $P_j$. 

We now state the following function independent test set $T$ for detecting single stuck-at faults in an AND-EXOR array realizing an EMC expansion of an $n$-variable function $F$. This was originally derived by Reddy [R-2]. He has shown that this test set $T$ fails to detect single stuck-at faults at the primary inputs if the corresponding input variables appear in an even number of product terms of the EMC expansion. However, he has proposed testable designs [R-2] in which all such stuck-at faults can be detected at the augmented output. The test set $T$ is given by

$$T = T_1 \cup T_2,$$

where,

$$T_1 = \begin{bmatrix} a_0 & x_1 & x_2 & x_3 & \cdots & x_n \\ 0 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 1 & 1 & \cdots & 1 \\ 1 & 1 & 1 & 1 & \cdots & 1 \end{bmatrix}$$

and

$$T_2 = \begin{bmatrix} a_0 & x_1 & x_2 & x_3 & \cdots & x_n \\ d & 0 & 1 & 1 & \cdots & 1 \\ d & 1 & 0 & 1 & \cdots & 1 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ d & 1 & 1 & 1 & \cdots & 0 \end{bmatrix}$$

where $d$ can be taken as 0 or 1 and the cardinality of the test set $T$ is

$$|T| = |T_1| + |T_2| = 4 + n.$$

We will show in the later sections that this universal test set $T$ is sufficient to detect any bridging fault included in our proposed fault model in the network, provided the fault is OB-type and we will also show that some more function independent tests are necessary in case the fault is AND-type. However, in either case it requires augmentation of the network.

3.3. Bridging faults in EMC network

Before going to the detection problem of bridging faults in such networks, we first present some definitions and auxiliary results in the following subsection.
3.3.1. Some definitions and results:

Definition 3.2: Any bridging fault involving two lines \( h \) and \( m \) in a logic network is said to be a single bridging fault if none of the lines \( h \) and \( m \) is a fanout stem or a fanout branch line.

Definition 3.3: Any bridging fault involving more than two lines either physically or logically (by the term 'logical' we mean to incorporate the fact that if a line say \( h \), is involved in a bridging fault and if \( h \) happens to be a fanout stem or fanout branch line, then all the lines emanating from the parent stem line would also be logically involved in the fault) is called a multiple bridging fault.

Definition 3.4: Let \( f_{m_1} \) and \( f_{m_2} \) be two bridging faults denoted by \( (h_1, h_2, \ldots, h_{k_1}) \) involving lines \( h_1, h_2, \ldots, h_{k_1} \) and \( (l_1, l_2, \ldots, l_{k_2}) \) involving lines \( l_1, l_2, \ldots, l_{k_2} \) respectively. Note that if any of the lines involved in \( f_{m_1} \) (\( f_{m_2} \)) happens to be a fanout stem or branch line, then all the lines emanating from the parent stem line would be automatically involved in \( f_{m_1} \) (\( f_{m_2} \)), so far as the logical effect of the bridging fault is concerned and thereby an augmented set \( f'_{m_1} (f'_{m_2}) \) of involved lines is created. If \( f'_{m_1} \cap f'_{m_2} = \emptyset \) (null), then the fault instance defined by the simultaneous occurrence of \( \{f'_{m_1}, f'_{m_2}\} \) is called a multiple group bridging fault of multiplicity 2. Similarly the idea can be extended to define a multiple group bridging fault of higher multiplicity, say \( n : \{f'_{m_1}, f'_{m_2}, \ldots, f'_{m_n}\} \) such that

\[
\forall i, j, i, j \in \{m_1, m_2, \ldots, m_n\}, i \neq j, \quad f'_i \cap f'_j = \emptyset \text{ (null)}.
\]

Definition 3.5: Any bridging fault involving the input lines of a logic gate in a logic network is said to be an intragate bridging fault.
Definition 3.6: Any bridging fault involving input lines to different logic
gates in a logic network is said to be an intergate bridging fault.

Definition 3.7: Any bridging fault involving lines of the same logic level in
a logic network is said to be an intralevel bridging fault.

Definition 3.8: Let \( f_b \) be an AND/OR bridging fault between two lines \( h \) and \( m \).
Then it is symbolically represented as \( f_b = *(h/m)/+(h/m) \).

Definition 3.9: Let \( N \) be the network realizing a function \( F_0 \). Let due to some
fault 'f' in it, the faulty function be \( F_f \). Then it is symbolically represented
as \( F_f \rightarrow \leftarrow N \rightarrow F_o \).

Definition 3.10: Let \( h \) be a line in a logic network. Then the functional
value at line \( h \) is referred to as the line function of \( h \) and it is denoted by \( f(h) \).

Lemma 3.3: All detectable bridging faults in an EXOR gate are always detected
by the four function independent stuck-at fault tests of the gate.

Theorem 3.1: Let \( F_0 \) be a linear function of \( n \)-variables, say, \( x_1, x_2, \ldots, x_n \)
and let it be realized by an one-dimensional EXOR array. Then any OR bridging
fault, whether it is single, multiple or multiple group bridging, involving the
primary input lines is always detected by some test belonging to a function
independent test set \( T \), under the assumption that no bridging fault causes the
network to oscillate or to behave as an asynchronous machine. The test set \( T \)
is given by,

\[
T^* = \begin{bmatrix}
x_1 & x_2 & x_3 & \cdots & x_n & \cdots \\
0 & 1 & 1 & \cdots & 1 \\
1 & 0 & 1 & \cdots & 1 \\
1 & 1 & 0 & \cdots & 1 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
1 & 1 & 1 & \cdots & 0 \\
\end{bmatrix}
\]

n input vectors.
Proof: The proof is constructive.

First of all, we consider single bridging fault. Let it be $f_b = \frac{h}{m}$ and the line functions of the primary input lines $h$ and $m$ be $f(h)$ and $f(m)$, where $f(h) = x_h$ and $f(m) = x_m$. It is clear that in presence of $f_b$, $f(h) = f(m) = x_h + x_m$. To detect the fault, an input vector is to be applied that makes either $f(h)$ as 1, $f(m) = 0$, or, $f(h) = 0$, $f(m) = 1$ in the fault free condition. The following two input vectors are able to produce the above assignments of values of lines $h$ and $m$. These are,

1. $x_h = 0$, and all other $x_i$'s = 1, for $1 \leq i \leq n$, $i \neq h$,
2. $x_m = 0$, and all other $x_i$'s = 1, for $1 \leq i \leq n$, $i \neq m$.

In any case, in presence of $f_b$, $f(h) = f(m) = 1$. Thus it is seen that $f(h)$ and $f(m)$ are of opposite values in absence of $f_b$ and of same values when $f_b$ is present. This causes a logic value at the network output different from an expected one. Hence $f_b$ is detected. Clearly the two input vectors considered above belong to the set $T^*$.

Next, we consider multiple bridging fault. Let it be $f_b$ involving the primary input lines $h$, $m$, ..., $l$, the corresponding line functions being $f(h) = x_h$, $f(m) = x_m$, ..., $f(l) = x_l$ in the fault free condition. In presence of $f_b$ all the above line functions become identical and each of them becomes equal to $(x_h + x_m + ... + x_l)$. To detect the fault an input vector 't' is chosen that fixes only one of the bridged lines, say $h$, at 0 and all other lines at 1 in the fault free condition. In other words, it sets $x_h = 0$ to make $f(h) = 0$ and all other $x_i$'s = 1, for $1 \leq i \leq n$, $i \neq h$. Under the application of this input vector, $f(h)$ becomes 1 due to the bridging fault, which is otherwise zero in absence of the fault. This in turn causes a logic value at the network output different from an expected one, meaning thereby that $f_b$ is detected. Evidently
Lastly we consider multiple group bridging fault. Let it be $f_b = \{f_{b_1}, f_{b_2}, \ldots, f_{b_m}\}$. To detect the fault, we select one of the component faults, say $f_{b_1}$, and excepting only one line, say $h$, involved in the bridging $f_{b_1}$, all other primary input lines involved in the bridging fault $f_b$ are fixed at logic value 1 as well as all other primary input lines not involved in the bridging are also fixed at 1. In other words, an input vector is chosen that sets $x_h = 0$, where $f(h) = x_h$ and all other $x_i$'s = 1, for $1 \leq i \leq n$, $i \neq h$. As in the previous two cases $f(h)$ becomes 1 due to $f_b$ causing a change in logic value at the network output line. Thus $f_b$ is detected. Clearly this test also belongs to the set $T^*$.

Hence we conclude that $T^*$ is sufficient for detecting the different OR-bridging faults considered in the theorem. Q.E.D.

Extension of theorem 1 to the case of AND-bridging faults reveals the fact that the universal test set $T^*$ is not sufficient to detect all the AND-bridging faults considered in theorem 3.1. One such case where the test set $T^*$ fails to detect is the presence of any multiple bridging fault that involves odd number of input lines. Reason behind this failure is quite obvious. But it can be shown in an identical way as in the case of OR-bridging faults that another function independent (universal) test set $T^{**}$ of cardinality $n$ is sufficient to detect different single, multiple and multiple group AND-bridging faults involving the primary input lines in the EXOR array realizing a linear function, $F_o = x_1 \oplus x_2 \oplus \ldots \oplus x_n$. The test set $T^{**}$ is given by,
3.3.2. Fault model:

We now state the fault model which we consider here. It includes the following considerations:

1) Only intralevel bridging faults will be dealt with. These are mainly:

a) bridging faults involving only two lines in the $L_1$-level. These lines may be those that are directly connected to the collector row EXOR gates from the primary input stems. This type of bridging also includes bridging between two inputs of the same EXOR gate in the collector row.

b) The following different types of bridging faults are considered in $L_0$-level. These are:

Bridging involving only primary input lines, intragate and intergate bridging faults and any bridging fault involving some input lines of AND gates and some lines that are directly connected to the collector row EXOR gates from their primary input stems.

2) All single stuck-at faults are considered.

3) Feedback bridging faults are not considered.
Without any loss of generality we first assume OR-bridging faults in the network in the following section.

3.3.3. Consideration of OR-bridging faults:

We consider each intralevel bridging separately in the following way.

3.3.3.1. Bridging faults in $L_1$-level:

We classify the different cases of bridging faults in this level in the following subclasses.

Class A: Let the bridging fault be $f_b = + (i/j)$. The line functions of lines $i$ and $j$ are $f(i) = P_i$ and $f(j) = P_j$ respectively, where $P_i$ and $P_j$ are product terms. According to Lemma 2, $P_i$ and $P_j$ are related to each other either by relation $R_1$ or by $R_2$. We consider each case separately.

Case 1: When relation $R_1$ holds good, then either $P_i \supset P_j$ or $P_i \subseteq P_j$. To detect the fault an input vector is to be applied that sets opposite logic values at the lines $i$ and $j$ in absence of the fault. In other words, it will set either $P_i = 1$, $P_j = 0$, or $P_i = 0$ and $P_j = 1$. According to Lemma 1 the product term covered by the other whenever relation $R_1$ exists between them always has at least one control literal in it. Then clearly an input vector that sets this control literal at 0 and all other $(n-1)$ literals in the binary $n$-vector at 1 with $a_0 = 0$ or 1 is a test. Under this input assignment in absence of the fault $f(i) = 1$, $f(j) = 0$ if $P_i \supset P_j$ and vice-versa if $P_i \subseteq P_j$. But in either case, presence of the fault makes both $f(i) = 1$ and $f(j) = 1$. The effect of this change of logic value of either line $i$ or line $j$ will propagate to the network output causing there a change of logic value. Thus the fault is seen to be detected and this input vector is clearly a member of the universal test set $T$, described earlier.
Case 2: When relation $R_2$ holds good, i.e., when $P_i \not\supset P_j$, $P_i \not\subset P_j$ and $P_i \cap P_j \neq \emptyset$ (null), then each of $P_i$ and $P_j$ has at least one control literal in it. In this case we start with either $P_i$ or $P_j$, say $P_i$ and an input vector 't' is chosen that sets one of the control literals in $P_i$ at 0 to make $P_i = 0$ and all other $x_i$'s in the binary $n$-vector at 1 to make $P_j = 1$ with $a_o = 0$ or 1. As in the previous case this input vector detects the fault at the network output. Here also $t \in T$.

Class B: Here we consider bridging between two lines $h$ and $m$ such that $f(h) = x_h$ and $f(m) = P_m^*$, a product term. The line $h$ may be a fanout branch line. To detect the fault, we design a test vector $t$ such that $f(h) = x_h = 1$ and one of the control literals in $P_m^*$, say $x_k = 0$ to make $P_m = 0$ and all other $(n-2)$ variables in the test vector are set at 1 with $a_o = 0$ or 1. In presence of the bridging fault, $f(m)$ becomes 1 and this change in value of line $m$ produces a change in value at the network output. This test vector $t$ is also included in the set $T$. In fact by making $x_h = 1$, the propagation of the effect of the bridging fault to the parent stem line of line $h$, if it is a fanout branch line has been stopped.

Class C: Let us consider a bridging fault $f_b = + (h/m)$, where $f(h) = x_h$ and $f(m) = x_m$. Unless both of the lines $h$ and $m$ are fanout branches, tests can be found included in the set $T$ to detect $f_b$ like the previous two cases. But problems arise when both $h$ and $m$ are fanout branches. Because any input vector chosen from the set $T$ that has a chance to detect $f_b$ at network output must fix either $x_h = 0$, $x_m = 1$ or $x_h = 1$, $x_m = 0$. In either case in presence of $f_b$, $x_h = x_m = 1$ and this change of logic value at line $h$ or $m$, which can be considered as the effect of the bridging fault, propagates to the corresponding stem line and hence to all other fanout branch lines emanating from this stem line. In effect all these lines will have a logic value 1 instead of the applied value 0. This
may cause the logic value at the output to remain same. Thus $T$ may fail to
detect $f_b$. In fact, the detection of such faults by the set $T$ depends on how
many times $x_h$ and $x_m$ appear in the EMC expansion and in what way they appear.
However, we will show later that a proper augmentation of the network will
enable $T$ to detect such faults.

**Class D**: Here we consider a bridging fault $f_b = + (h/m)$, where the lines $h$ and
$m$ are the two inputs of a collector row EXOR gate. Since the test set $T$ is always
able to bring a 1 at line $h$ and a 0 at line $m$ or vice-versa, hence this type of
bridging faults is always detectable by the test set $T$.* If one of the input
lines is the control line, then also $T$ detects the fault. The test vector
simply sets $a_0 = 0$ and all $x_i's = 1$ for $1 \leq i \leq n$.

3.3.3.2. **Bridging faults in Level 2**

We consider the different cases of bridging faults in this level in the
following way.

**Intragate bridging faults**:

Unless all the lines involved in the bridging are fanout branches, the
test set $T$ is able to detect such faults. Let us assume an intragate bridging
fault $f_b$ and let the involved lines be $(h, k, ..., l)$ such that at least one of
them, say $h$, is not a fanout branch line. Then a test vector is always found in
$T$, that sets $x_h = 0$ where $f(h) = x_h$ and all other $x_i's = 1$, for $1 \leq i \leq n$, $i \neq h$
with $a_0 = 0$ or 1. Under the application of this test vector the faulty output
of the affected AND gate will be 1, which is otherwise 0 in the fault free
condition. This will cause a change of the logic value at the output. Hence $f_b$
is detected. But if all the lines involved in the bridging are fanout branches
then it cannot be guaranteed that $T$ will detect the bridging fault. Reasons
behind this are similar to that in Class C case.
Interate bridging faults:

Here also T may fail to detect such faults if all the lines involved in the bridging are fanout branches. Reasons are similar as in the case of intragate bridging faults.

Bridging fault involving the primary input lines:

The test set T may fail to detect such faults because their detection by the test set T depends on how many times and in what way the literals connected to the input lines involved in the bridging appear in the BMC expansion of the function realized.

Lastly we consider a bridging fault \( f_b \) that involves some lines that are inputs to some AND gates and some lines that are directly connected from their input stems to some collector row EXOR gates. In this case also the presence of the fault may not be ensured by applying test vectors included in T. The explanation of this failure is similar as in the previous cases.

3.3.3.3. Detection of single stuck-at faults:

It is already known [B-2] that the \((n+4)\) tests given earlier detect all single stuck-at faults in the BMC network excepting a few ones at those primary inputs which appear in an even number of product terms in the BMC expansion. However, we will show later that these faults will be detected by the same \((n+4)\) tests after some proper augmentation of the network. Also we will show that in this augmented network the bridging faults in \(L_0\) and \(L_1\)-level that are undetectable by the test set T at network output before augmentation will be detected by this test set T.

We now propose the following testable design to detect the above mentioned undetectable bridging faults.
3.3.5. A testable design:

We now give a technique to add an extra AND gate to make the universal test set $T$ sufficient to detect the different types of bridging faults and stuck-at faults considered in the fault model. The output of the added AND gate is assumed to be observed during testing. The augmented network is shown in Fig. 3.5. This added gate is an $n$-input AND gate, realizing the function $(x_1 \cdot x_2 \cdots x_n)$.

We now show that all the bridging faults that are undetected under the test set $T$ in the unaugmented network will be detected at the observable output point $O_2$ by the application of tests from the same test set $T$. It is interestingly seen that the bridging faults in the $L_0$-level described earlier are nothing other than some single and multiple bridging faults. Any such fault is detected at $O_2$ by a test vector that fixes one of the bridged lines, say $i$, at 0 by making $x_i = 0$, where $f(i) = x_i$ and all other $(n-1)$ variables at 1. In absence of the fault, the output at $O_2$ is 0 under such input vector, while it becomes 1 when the fault happens to occur. This input vector is clearly included in $T$. Moreover another type of fault, namely multiple group bridging fault in this level is also detected at $O_2$ in the following way. Let the multiple group bridging fault be $f = \left\{ f_{b_1}, f_{b_2}, \ldots, f_{b_m} \right\}$. To detect the fault at $O_2$, we select arbitrarily one of the component faults, say $f_{b_1}$, and apply an input vector $'t'$ that sets only one of the lines, say $h$, involved in the bridging $f_{b_1}$ at 0 by making $x_h = 0$, where $f(h) = x_h$ and all other $x_i$'s in the binary $n$-vector at 1. In absence of $f_{b_1}$, the output at $O_2$ is 0 while it becomes 1 when the fault happens to occur. So, $t$ detects $f_{b_1}$. It is seen that $t \in T$. The Class C type of faults described earlier in this section can also be detected at the observable output $O_2$ in a similar way. In each of the above cases, the detection procedure takes...
help of the fact that the effect of a bridging fault involving a fanout branch line always propagates to the corresponding stem line.

We have seen earlier that the test set $T$ fails to detect stuck-at faults at those primary inputs which appear in an even number of product terms. However, we see that the test inputs in $T$ are sufficient to detect such faults at the observable output $O_2$ of the testing AND gate because a single path is sensitized from each primary input to the output $O_2$. Thus, in fact all single stuck-at faults at the primary inputs are detected at the output $O_2$. Also due to the same reason all stuck-at-0 and stuck-at-1 faults of the extra AND gate are detected by this test set $T$.

We now state the results so far obtained in theorem 3.2.

Theorem 3.2: An AND-EXOR array realizing the complement free KMC expansion of a switching function $F_q$ of $n$-variables can be so augmented by adding an extra AND gate that the universal test set $T$ of cardinality $(n+4)$ is sufficient to detect the different intralevel OR bridging faults and all single stuck-at faults.

It may be noted that any bridging fault involving some lines in $L_0$-level and some of the input lines of the testing AND gate, or simply involving some of the input lines of this gate is always detected by the same test set $T$ at the augmented output $O_2$. The detection procedure is identical to that in case of $L_0$-level bridging described above.

3.3.4. Consideration of AND-bridging faults:

In case of AND-bridging also, similar arguments prevail regarding the failure of the test set $T$ to detect some of the intralevel bridging faults in the unaugmented network. These bridging faults are of the same classes as in the case of OR-bridging.
We have shown earlier that in case of OR-bridging faults only one extra AND gate is necessary to make the universal test set $T$ sufficient for detecting the different bridging faults and all single stuck-at faults. So naturally question arises whether addition of only one extra OR gate makes the test set $T$ sufficient in case of AND bridging faults. However the answer is negative. The following discussion shows that we will have to generate another function independent test set $T_\alpha$ of cardinality $n$, which together with the test set $T$ will be sufficient for detecting the different AND bridging faults considered in the fault model and all single stuck-at faults if the network is made testable by adding only one extra OR-gate. $T_\alpha$ is given by:

\[
T_\alpha = \begin{bmatrix}
  a_0 & x_1 & x_2 & x_3 & \ldots & x_n \\
  d & 1 & 0 & 0 & \ldots & 0 \\
  d & 0 & 1 & 0 & \ldots & 0 \\
  d & 0 & 0 & 1 & \ldots & 0 \\
  \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\
  d & 0 & 0 & 0 & \ldots & 1 
\end{bmatrix}
\]

We propose the following testable design in which an extra OR gate is added to the AND-EXOR array as shown in Fig. 3.6 and the output $0'_2$ of the added gate is assumed to be observed during testing. This added gate is an $n$-input OR gate realizing the function $(x_1 + x_2 + \ldots + x_n)$.

The way of detection of all the bridging and stuck-at faults of the fault model by the test sets $T$ and $T_\alpha$ at the observable output points $0_1$ and $0'_2$ is similar to that in the case of OR-bridging. Also all single stuck-at faults of the added OR gate are detected by the test inputs in $T$ and $T_\alpha$, at the observable output $0'_2$. That the test set $T$ fails even in this augmented network is clear from the following discussion.
Consider a bridging fault \( f_b \) involving some lines \( h, k, \ldots, l \) in the \( L_0 \)-level and also let us assume that this fault \( f_b \) was initially undetectable by \( T \) at network output before augmentation. Suppose the corresponding line functions are \( x_h, x_k, \ldots, x_l \) respectively. In order to detect \( f_b \) at the augmented output \( O'_2 \), at least one of these variables is to be fixed at 0. If we choose some input vector \( t \) from the set \( T \) to do so, then this input vector sets all other \((n-1)\) variables at 1. Due to the bridging the line functions of all the bridged lines become 0. But if there exists in \( L_0 \)-level at least one line, say \( i \) with \( f(i) = x_i \), not involved in the bridging such that \( f(i) \) differs from all the line functions of the involved lines, then all lines emanating from the parent stem line of line \( i \) together with the line \( i \) will not be affected by the bridging fault. So, under this input assignment \( f(i) \) will always be 1 as well as an input line to the OR gate, which is directly connected to the parent stem line of line \( i \) will always have a logic value 1 irrespective of whether the fault is present or not. Hence the output at \( O'_2 \) will always have a logic value of 1 regardless of the presence or absence of \( f_b \). Thus \( t \) fails to detect \( f_b \). On the other hand if we select some input vector from the set \( T_\alpha \) to fix only one of the variables \( x_h, x_k, \ldots, x_l \) at 1 and all other \((n-1)\) variables at 0 then in absence of \( f_b \), output at \( O'_2 \) will be 1 and it will be 0 when \( f_b \) is present. Thus \( f_b \) is detected. In fact, in this way it can be easily shown that the test set \( T \) together with the test set \( T_\alpha \) is sufficient to detect all bridging faults of the fault model.

The following theorem reflects the above obtained results.

**Theorem 3.3:** An AND-EXOR array realizing the complement free ERM expansion of a switching function \( F_0 \) of \( n \)-variables can be so augmented by adding an extra OR gate that the universal test set \( T_u \) of cardinality \((2n+4)\) is sufficient to
detect the different intralevel AND bridging faults and all single stuck-at faults. 

\[ T_u = T \cup T_\alpha \]

Here also any bridging involving some of the inputs of the testing OR gate and some other lines in the \( L_0 \)-level or simply involving some of the inputs of the testing OR gate is always detected at the testing gate output by the same test set \( T_u \).

**Corollary 3.1**: Any AND-bridging fault in the \( L_0 \)-level, that does not change the fault-free function at network primary output \( 0_1 \) is always detected at the observable output \( 0_2' \) of the testing OR gate by a test 't', where \( t \in T \), provided all of the lines involved in the bridging fault are not fanout branch lines of the same input stem line.

**Proof**: Consider a bridging fault \( f_b \) in \( L_0 \)-level, which does not change the fault-free function at network primary output and so it is basically an undetectable fault. But the effect of the bridging fault always propagates to the inputs of the testing OR gate. Let \( h \) be a line that is involved in the bridging fault \( f_b \) and let the line function of line \( h \) be \( x_h \). Then an input vector 't' that sets \( x_h = 1 \) and all other \( x_i 's = 0 \), for \( 1 \leq i \leq n \), \( i \neq h \) is a test, because under the application of 't', the output at the observation point \( 0_2' \) is 1 in absence of \( f_b \), while it becomes 0 in presence of \( f_b \). It is clear that \( t \in T_\alpha \). Q.E.D.

As a consequence of corollary 3.1 question may arise about the necessity of detecting undetectable bridging faults because in presence of such faults the network operates properly. But the presence of such undetectable bridging faults may invalidate the valid tests for detecting some detectable stuck-at faults at
network primary output \(0_1\) when simultaneously bridging and stuck-at faults occur. We give an example of such a situation. Consider the network shown in Fig. 3.7. The fault free function at network output \(0_1\) is:

\[ F_0 = x_1 \cdot x_2 \oplus x_1 \cdot x_2 \cdot x_3 \oplus x_1 \cdot x_2 \cdot x_4 \]

We consider a bridging fault \(f_b = * (h/k)\) as shown by the dotted line in the figure. It is seen that \(f_b\) does not change the fault free function \(F_0\). Now, we assume that in presence of \(f_b\), the line 1 has been stuck-at-1. Due to the simultaneous occurrence of the bridging and the stuck-at fault, the faulty function at network output \(0_1\) becomes:

\[ F_f = x_1 \cdot x_2 \oplus x_1 \cdot x_2 \cdot x_3 \oplus x_1 \cdot x_4 \]

We now try to detect this stuck-at fault by the test designed for it. It is:

\[ x_1 = 1, x_2 = 0, x_3 = 1, x_4 = 1 \text{ and } a_0 = 0 \text{ or } 1 \]

Clearly this test belongs to the set \(T\). It is seen that this test fails to detect the stuck-at fault at the output \(0_1\) because due to the presence of the bridging and stuck-at fault the faulty and the fault free logic values under this test at lines \(n, n\) and \(p\) are identical. In other words, presence of this undetectable bridging fault has masked the otherwise detectable stuck-at fault at the output \(0_1\). However this problem can be totally circumvented by the test set \(T_f\) which detects this type of bridging faults at the observable output \(0'_2\).

3.4. Conditions for undetectability of bridging faults among primary input lines:

We now give the necessary and sufficient conditions so that a bridging fault involving some primary input lines in a complement free ERM network becomes undetectable by any test at the network primary output. This is illustrated in the following theorems.
Theorem 3.4a: Let $h$ and $m$ be two primary input lines connected to the literals $x_h$ and $x_m$ respectively in a complement free EMC network $N$ realizing a Boolean function $F$. Then a bridging fault $f_b = *(h/m)$ is undetectable by any test at the network primary output if and only if $x_h$ appears only in all the terms containing the literal $x_m$ in the BMC expansion.

Proof: [Only if]: The complement free BMC expansion of $F$ can always be factored with respect to the literals $x_h$ and $x_m$ in the following way:

$$F = A \oplus x_h \cdot B \oplus x_m \cdot C \oplus x_h \cdot x_m \cdot D$$

where the Boolean functions $A$, $B$, $C$ and $D$ are independent of $x_h$ and $x_m$. We now consider a bridging fault $f_b = *(h/m)$, where $f(h) = x_h$ and $f(m) = x_m$ and the lines $h$ and $m$ are primary input lines.

Let $F_o \xrightarrow{N} F_f$, where the faulty function $F_f$ at network primary output is:

$$F_f = A \oplus x_h \cdot x_m \cdot B \oplus x_h \cdot x_m \cdot C \oplus x_h \cdot x_m \cdot D$$

For $f_b$ to be undetectable at the network output by any test,

$$F_o = F_f$$

i.e. $A \oplus x_h \cdot B \oplus x_m \cdot C \oplus x_h \cdot x_m \cdot D = A \oplus x_h \cdot x_m \cdot B \oplus x_h \cdot x_m \cdot C \oplus x_h \cdot x_m \cdot D$

or, $x_h \cdot B \oplus x_m \cdot C = x_h \cdot x_m \cdot B \oplus x_h \cdot x_m \cdot C$

or, $B \cdot (x_h \oplus x_h \cdot x_m) = C \cdot (x_m \oplus x_h \cdot x_m)$

or, $x_h \cdot x_m \cdot B = x_h \cdot x_m \cdot C$

Clearly (1) is true only when $B = C = 0$.

In other words, the necessary condition for the bridging fault $f_b$ to be undetectable at network primary output is that there cannot exist any term in the EMC expansion of $F_o$, which contains one of the literals of $x_h$ and $x_m$ and not both.
Let $PQ = A \oplus x_h \cdot x_m \cdot D$, where the Boolean functions $A$ and $D$ are independent of $x_h$ and $x_m$.

Let the bridging fault be $f_b = *(h/m)$ where the line functions of the primary input lines $h$ and $m$ are $x_h$ and $x_m$ respectively. Let

$$F_o \xrightarrow{f_b} N \rightarrow F_f,$$

where the faulty function $F_f$ at network primary output is:

$$F_f = A \oplus x_h \cdot x_m \cdot D$$

Thus $F_o = F_f$ and hence $f_b$ is undetectable by any test at network primary output.

This proves the sufficiency part of the theorem.

Theorem 3.4b: Let $h$ and $m$ be two primary input lines connected to the literals $x_h$ and $x_m$ respectively in a complement free BMC network $N$ realizing a Boolean function $F_o$. The BMC expansion can always be factored as:

$$F_o = A \oplus x_h \cdot B \oplus x_m \cdot C \oplus x_h \cdot x_m \cdot D,$$

where the Boolean functions $A$, $B$, $C$ and $D$ are independent of $x_h$ and $x_m$. Then a bridging fault $f_b = +(h/m)$ is undetectable at the network primary output by any test if and only if

$$B = C = D$$

Proof: [Only if]: We have the fault free function at network primary output as:

$$F_o = A \oplus x_h \cdot B \oplus x_m \cdot C \oplus x_h \cdot x_m \cdot D$$

We now consider the bridging fault $f_b$ as mentioned in the theorem. Let

$$F_o \xrightarrow{f_b} N \rightarrow F_f.$$
where the faulty function $F_f$ at network primary output is :

$$F_f = A \oplus (x_h + x_m) B \oplus (x_h + x_m) C \oplus (x_h + x_m) D$$

For $f_b$ to be undetectable at the network primary output,

$$F_o = F_f$$

i.e. $A \oplus x_h \oplus x_m \oplus x_h \oplus x_m \oplus D = A \oplus (x_h + x_m) B \oplus (x_h + x_m) C \oplus (x_h + x_m) D$

or, $(x_m \oplus x_h \oplus x_m) B \oplus (x_h \oplus x_m) C = (x_h \oplus x_m) D$

or, $x_h \overline{x}_m B \oplus x_h \overline{x}_m C = x_h \overline{x}_m D \oplus x_h \overline{x}_m D$

or, $x_h \overline{x}_m (C \oplus D) = x_h \overline{x}_m (B \oplus D)$ ... (1)

Since the functions $B$, $C$ and $D$ are all independent of $x_h$ and $x_m$, condition (1) is true if and only if

$$(C \oplus D) = (B \oplus D) = 0,$$

which implies, $B = C = D$, which is the necessary condition for $f_b$ to be undetectable at network primary output.

[If] : Proof of the 'If' part is obvious. Q.E.D.

Theorems 4a and 4b depict conditions of undetectability of bridging faults among primary input lines. Note that whenever the complement free EMC expansion of a Boolean function satisfies such properties those bridging faults become undetectable irrespective of network topology. Even these bridging faults can be detected at the outputs $O_2$ and $O_2'$ of the testing gates.

3.5 Detection of feedback bridging faults:

Although we have not included in our fault model the occurrence of any feedback bridging fault, still the testable designs proposed in this chapter are capable of detecting a large number of such faults. For example, let us consider a feedback bridging fault $f_b = +(h/k)$, where $f(h) = x_h$ and $f(k) = F_k$, a product
term containing the literal $x_h$. Now we consider an input vector that sets $x_h = 1$, and some control literal $x_c$ in $P_k = 0$, and all other $x_i$'s = 1, for $i \neq h, i \neq c$, with $a_o = 0$ or 1. This input vector is included in the set $T$. Under the application of this input vector the logic value at line $k$ becomes 1 due to the presence of the fault, but that of the line $h$ remains unaltered. This means that the effect of the fault cannot propagate backward. In other words, if the line $h$ happens to be some fanout branch line, then the effect cannot propagate to the corresponding stem line and thereby cannot propagate to all other branch lines of the stem line. Instead, this effect propagates to the network primary output under the application of this input vector and hence can be detected. In fact, although $f_b$ is a feedback bridging fault, still this input vector does not allow the fault to induce any feedback effect when it is applied to detect the fault. In a similar way, we can detect a large number of feedback bridging faults by the function independent tests we have considered.

3.6. Conclusion:

In the present chapter, it has been shown that in EMC networks bridging faults can be detected by function independent tests as is the case with stuck-at faults. It has also been shown that the necessary augmentation for detecting both OR and AND type bridging faults in a complement free EMC network requires the addition of only one extra gate in each case. For any EMC expansion other than complement free, we propose the following augmentation. In case of OR-bridging faults, one OR gate and one AND gate both of which are $n$-input gates for an $n$-variable function realized by the network in question are required. The output functions of the respective gates are $(x_1 + x_2 + \ldots + x_n)$ and $(x_1 x_2 \ldots x_n)$. In addition to the above mentioned two gates, another AND gate with $n_1$-inputs is required where $n_1$ is the number of distinct complemented...
literals that appear in the EMC expansion. The input lines of this AND gate are lines drawn from the outputs of the corresponding inverters used to obtain the \( n_1 \)-complemented literals. However the required tests are the members of the test set \((T \cup T_\alpha \cup T_\beta)\) where \(T\) and \(T_\alpha\) have been mentioned earlier and \(T_\beta = \{I_n \mid \text{wt}(I_n) \leq j\}\), i.e. set of all \(n\)-vectors of weight \(j\) or less, \(j\) being the order of the function realized. By 'order' we mean that \(j\) is the maximum of the number of literals contained in any product term in the EMC expansion and weight of the binary \(n\)-vector \(I_n\), \(\text{wt}(I_n)\) is the number of 1's in the binary vector. \(T_\beta\) is applied with \(a_0 = d\), where \(d\) can be taken as 0 or 1. In case of AND bridging faults, a proper augmentation can also be done similarly.

It is quite easily seen that the condition of undetectability of bridging faults involving primary input lines in networks realizing EMC expansion of a Boolean function based on any polarity vector other than complement free can similarly be derived as in the case of complement free EMC expansion.

From the point of view of fault detection, so far almost all existing works are based on stuck-at fault model and incorporation of bridging faults has been so far ignored although in MOS-LSI circuits the probability of bridging faults in different layers of metallization and diffusion is substantially high. That is why our present work includes bridging faults. But we have not considered interlevel bridging faults because in that case the behavior of the circuit would become highly complex and some additional tests might be necessary. Moreover we can avoid the possibility of interlevel bridging faults to a large extent by proper fabrication of the chip so that the proximity effect among lines corresponding to different levels is minimized with a consequent reduction in the probability of occurrence of interlevel bridging faults.
Fig. 3.1a. Original circuit

Fig. 3.1b. Equivalent faulty circuit for AND bridging fault

Fig. 3.1c. A feedback bridging fault
Network realizing the function \( F = x_1 \oplus x_2 \oplus x_3 x_4 \oplus x_5 x_6 x_7 \).

Fig. 3.2. Network realizing the same function \( F_0 \) as in Fig. 3.2.

Network realizing the function \( F_0 = x_1 \oplus x_2 \oplus x_3 x_4 \oplus x_5 x_6 x_7 \).

Fig. 3.3. Network realizing the same function \( F_0 \) as in Fig. 3.2.
Fig. 3.4. A general model of a complement-free RMC network

Fig. 3.5. A testable design in case of OR-type bridging
Fig. 3.6. A testable design in case of AND-type bridging

The added OR gate

Fig. 3.7. Network realizing the function $F_0 = x_1 x_2 \oplus x_3 \oplus x_1 x_2 x_4$