# Table of Contents

List of Publications ................................................................. iv-vi

Table of Contents ....................................................................... vii-x

## CHAPTER 1

### INTRODUCTION........................................................................................................... 1-43

1.1. An Overview of Nanoscale CMOSFETs.......................................................... 1-15

1.1.1. Novel Device Structures .................................................................................. 8-13

1.1.1.1. SOI MOSFETs ....................................................................................... 8-9

1.1.1.2. Multi-Gate MOSFETs .............................................................................. 10

1.1.1.3. Source/Drain Engineering ........................................................................ 10-13

1.1.2. New Channel Materials .................................................................................. 14-15

1.2. Why Ge .................................................................................................................. 16-18

1.3. Review of Work on Ge MOSFETs...................................................................... 19-26

1.3.1. Ge MOSFET Substrate Preparation .............................................................. 19-22

1.3.2. Gate Stacks in Ge MOSFETs ....................................................................... 22-23

1.3.3. Surface Passivation Schemes for Ge MOSFETs ......................................... 24

1.3.4. Source/Drain Junctions and Contacts in Ge MOSFETs .............................. 24-25

1.3.5. Modeling and Simulation .............................................................................. 25-26

1.4. Untouched Areas ............................................................................................... 26

1.5. Scope of the Present Work .................................................................................. 27

1.4 Organization of the Thesis .................................................................................. 27-28

References .............................................................................................................. 29-43
# CHAPTER 2

CONTROL OF SHORT CHANNEL EFFECTS IN GERMANIUM CHANNEL MOSFETS BY EMPLOYING HALO IMPLANTS .......................... 44-81

2.1. Introduction .................................................................................................................. 44-47

2.2. Device Structure Under Study ..................................................................................... 48-49

2.3. Modeling and Simulation ............................................................................................ 49-58
   2.3.1. Model Development ............................................................................................... 49-55
   2.3.2. Simulation Setup ..................................................................................................... 55-58

2.4. Results and Discussions ............................................................................................... 59-73

2.5. Summary ....................................................................................................................... 74

References .......................................................................................................................... 75-81

# CHAPTER 3

ACCURATE DRAIN CURRENT MODEL FOR NANOSCALE GeOI MOSFETS BASED ON 2D CHANNEL POTENTIAL USING NON-CHARGE SHEET FORMULATION .................................................... 82-107

3.1. Introduction .................................................................................................................... 82-84

3.2. Device Structure Under Study ..................................................................................... 85

3.3. Modeling and Simulation ............................................................................................ 86-92
   3.3.1. Calculation of 2-D Channel Potential .................................................................... 86-88
   3.3.2. Non-Charge Sheet Drain Current Model ............................................................... 89-92
   3.3.3. Numerical Simulation of GeOI MOSFETs ........................................................... 92

3.4. Model Validation .......................................................................................................... 93

3.5. Results and Discussion ................................................................................................. 94-102

3.6. Summary ....................................................................................................................... 102

References .......................................................................................................................... 103-107
CHAPTER 4

2-D COMPACT DRAIN CURRENT MODEL FOR FULLY DEPLETED NANOSCALE GeOI MOSFETS .................................................. 108-130

4.1. Introduction .................................................................................................................. 108- 109

4.2. Model Formulation .......................................................................................................... 110-115

  4.2.1. Calculation of Surface Potential and Inversion Charge ........................................... 110-113

  4.2.2. Drain Current Model ................................................................................................. 113- 115

4.3. Simulation of GeOI MOSFETs ....................................................................................... 116

4.4. Results and Discussion ................................................................................................. 117-125

4.5. Summary ....................................................................................................................... 125

References ......................................................................................................................... 126-130

CHAPTER 5

EFFECTS OF GATE, SOURCE AND DRAIN ENGINEERING ON THE PERFORMANCE OF NANOSCALE GeOI MOSFETS FOR MIXED SIGNAL SYSTEM-ON-CHIP (SOC) APPLICATIONS ........................................ 131-161

5.1. Introduction .................................................................................................................. 131-133

5.2. PART A

Effects of Gate Engineering on the Performance of GeOI MOSFETs for Mixed Signal SoC Applications................................................................. 134-146

  5.2.1. Device Structure and Simulation Setup ....................................................................... 134-136

  5.2.2. Model Calibration ...................................................................................................... 137-138

  5.2.3. Results and Discussion .......................................................................................... 139- 146

ix
5.3. PART B

Impact of Metal Source/Drain Contacts on Nanoscale UTB-GeOI
MOSFETs for Mixed-Signal SoC Applications........................................... 147-154
5.3.1. Device Description .........................................................................147-148
5.3.2. Results and Discussion .................................................................149-154
5.4. Summary ..........................................................................................155

References ..............................................................................................156-161

CHAPTER 6

CONCLUSION AND FUTURE WORK ......................................................162-165
6.1. Conclusion ........................................................................................162-164
6.2. Future Work ......................................................................................165
CHAPTER 1

INTRODUCTION

1.1. An Overview of Nanoscale CMOSFETs

In 1928 the concept of the metal-oxide-semiconductor field-effect-transistor (MOSFET) was introduced in a patent filed by Julius Edgar Lilienfeld [1]. The realization of a functional MOSFET took more than thirty years and in 1958 the first practical silicon MOSFET was successfully demonstrated by Kahng and Atalla at the Solid State Device Research Conference in Pittsburgh [2]. The revolution in MOSFET technology took place in 1963 with the discovery of the complimentary MOS (CMOS) circuit, consisting of both n-channel and p-channel MOS devices fabricated on a single silicon substrate [3]. These circuits allow large number of transistors with interconnections to integrate on a single silicon chip with low cost and can offer extremely low static power consumption, high switching power density and very high noise immunity with significantly high packing density. CMOS circuit, being an ideal voltage controlled switch, is used to perform all basic logic operations as well as amplifiers in analog applications.

In 1965, just six years after the invention of the integrated circuit by Jack St. Clair Kilby [4], Dr. Gordon Moore predicted a trend of MOSFET device dimension scaling, is now better known as Moore’s Law, simply states that the number of transistors on an integrated circuit chip would double every year and a half [5]. Continuous scaling of MOSFET devices was successfully propelled by the rapid advancement of device engineering and fabrication technology for gaining better performance and higher packing density leading to greater computational complexity and reduced cost per individual transistor for every successive generation.
1.1. An Overview of Nanoscale CMOSFETs

Chapter 1

Fig. 1.1 Schematic diagram of a planar bulk MOSFET

Fig. 1.2 (a) A large MOS device and (b) scaled down MOS device with the similar electric-field patterns.
However, as the device size approaches tens of nanometers conventional device dimension scaling of the Si CMOS devices becomes more and more challenging and fundamental as well as practical constraints is limiting [6]-[7] the maximum performance achievable by these scaled transistors. Fig. 1.1 shows the schematic diagram of conventional planar bulk MOS transistor. Traditionally, constant field scaling, originally proposed by Dr. R. H. Dennard in 1974 [8], is followed to maintain the overall electric field unchanged in the device so that the scaled device is not worse than the original device with respect to performance and reliability. The basic idea behind the constant field scaling is described in Fig. 1.2. A large MOS device, shown in Fig 1.2 (a), is scaled down in size by reducing all of its horizontal and vertical dimensions by a common factor k ( >1 ) to produce a smaller MOS device, shown in Fig 1.2 (b), with the similar electric-field patterns as the larger device. In addition to the physical size reduction of the device the impurity doping concentrations must be increased and the power supply voltage (V_DD) must be decreased in the smaller device to ensure the preservation of the electric field patterns within the device. A more detailed list of the constant field scaling rules for various device parameters and performance factors is shown below in Table 1.1. The three most crucial results of constant field scaling are: the circuit density improves by a factor k^2; the speed of the device improves by a factor k; and the power dissipation per circuit is reduced by a factor k^2 [9]. Thus constant field scaling offers a preliminary insight of the concepts and techniques behind scaling of MOSFETs. But with the increase in substrate doping concentration the mobility of the carriers in the inversion channel is decreased because of the higher impurity scattering. On the other hand the power-supply voltage is seldom scaled in proportion to channel length due to degradation of MOSFET drivability. So, the prerequisite in reduction of the substrate doping concentration and supply voltage with the same factor of physical dimensions of the device is too much restrictive.
### Table 1.1 Detailed List of the Constant Field Scaling Rules for Various Device Parameters and Performance Factors

<table>
<thead>
<tr>
<th>MOSFET device and circuit parameters</th>
<th>multiplication factor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device parameters</strong></td>
<td></td>
</tr>
<tr>
<td>Device dimensions</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Power-supply voltage</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>$k$</td>
</tr>
<tr>
<td>Electric field</td>
<td>1</td>
</tr>
<tr>
<td>Carrier velocity</td>
<td>1</td>
</tr>
<tr>
<td>Capacitance</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Inversion charge density</td>
<td>1</td>
</tr>
<tr>
<td>Channel resistance</td>
<td>1</td>
</tr>
<tr>
<td><strong>Circuit performance parameters</strong></td>
<td></td>
</tr>
<tr>
<td>On current</td>
<td>$k$</td>
</tr>
<tr>
<td>Circuit delay time</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Speed of the device</td>
<td>$k$</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>$1/k^2$</td>
</tr>
<tr>
<td>Power-delay product per circuit</td>
<td>$1/k^3$</td>
</tr>
<tr>
<td>Circuit density</td>
<td>$k^2$</td>
</tr>
<tr>
<td>Power density</td>
<td>1</td>
</tr>
</tbody>
</table>
The technology node with their corresponding power supply voltage, gate oxide thickness and vertical electric field for several generation of CMOS VLSI technology is enlisted in Table 1.2. One can easily observe from Table 1.2 that the electric field inside the MOSFET increases from one technology generation to the next. The higher field in the channel degrades the device performance and the reliability as well. The larger lateral electric field compared to vertical electric field within the aggressively scaled devices leads to several problems, commonly known as short channel effects (SCEs) [10]. The SCEs cause the variation in threshold voltage on channel length. The reduction of threshold voltage at shorter channel length is well known as threshold voltage ($V_{TH}$) roll-off which leads to disperse of device characteristics with the scatter of gate length produced during the fabrication process. Smaller $V_{TH}$ at higher drain voltage ($V_{DS}$) due to a modulation of the source-channel potential barrier by the drain voltage termed as drain induced barrier lowering (DIBL) is degraded in scaled channel lengths. Smaller value of threshold voltage in short channel devices increases the off-state leakage current.

In order to maintain the relatively strong gate control of the channel potential in bulk devices, various technological improvements such as ultra-thin gate dielectrics, ultra-shallow source/drain junctions, halo implants and advance channel dopant profile engineering techniques have become essential. Each of these technologies is now approaching fundamental limitations which may, in turn, hinder further scaling of device dimensions. Therefore, technological progresses by means other than scaling such as alternative gate concepts (e.g. double gate devices, FinFETs, etc.), innovative device architectures and new materials with improved carrier mobility are needed to continue upgrading device performance.

The 1st sub-100 nm ITRS technology node, 90 nm node, was launched in 2004. At this 90 nm node SiGe was employed to introduce uniaxial/biaxial strain in the channel to
attain the high carrier mobility and hence the current drive improvements [11]-[14]. The oxide thickness was aggressively reduced to less than 1 nm for the 90 nm and 65 technology node to set the vertical electric field in the channel much larger than the lateral electric field in the channel so that the short channel effects like DIBL can be reduced significantly. Thin gate oxide also enhances the driving capability of MOSFETs. The improved short channel effects are obtained with thinned gate oxide thickness at the cost of enhanced quantum mechanical tunneling which increases the direct gate leakage current. High-k gate dielectrics are being introduced into the gate stack to replace the so called best insulator, SiO$_2$, to combat the problem of increasing direct gate tunneling current with decreasing oxide thickness. A high-k gate dielectric with dielectric constant higher than silicon dioxide offers a superior gate capacitance compared to the same
physical thickness of silicon dioxide. In other words, equal gate capacitance can be obtained with n-times higher physical thickness of a high-k dielectric having dielectric constant n-times higher than silicon dioxide. It is reported that lower than 3 nm SiO$_2$ thickness the gate leakage current increases by greater than 3 times for every 1 Å of gate oxide thickness reduction [15]. So, the larger physical thickness suppresses direct tunneling of carriers through the gate dielectric thereby reducing the gate leakage current by several orders of magnitude [16]. However, integration of high-k is challenging and faced problems including threshold voltage pinning due to charge neutrality level, mobility degradation due to soft optical (SO) phonons, and poor reliability [17]-[19]. Metal gates eliminate the poly depletion effect and improve the mobility degradation by screening the SO phonons introduced by high-k dielectrics. The metal gate and high-k dielectrics were successfully integrated at 45nm node in 2007 [20]. This fundamental change in transistor design was then called “The Biggest Change in Transistor Technology in 40 Years” by Gordon Moore. This was followed by 32 nm technology node with higher process induced stress, realized using contacts and shallow trench isolation (STI) structure adjacent to transistors [21]. At present, the 22 nm technology node is running production with the physical gate length approaching 10 nm. Volume production of Intel Core i5 and Intel Core i7 processors based on 22 nm technology is selling worldwide. Beyond 22 nm, more changes in materials and transistor architectures are expected. In near future changes are expected in the front of architectures which include multi-gate devices – FinFET, surround gate, and so on. The Intel® Core™ M processors using 22 nm 3D tri-gate transistors are already manufactured for production in 2014. The novel device architectures with source/drain and gate engineering are desirable for providing better gate control and reducing the problem of DIBL. The other likely option is to fabricate MOSFETs using high mobility channel materials such as Ge and III-V semiconductors.
1.1. An Overview of Nanoscale CMOSFETs

1.1.1. Novel Device Structures

1.1.1.1. SOI MOSFETs

The Silicon on Insulator (SOI) CMOS technology is relatively new technology [22-26] where MOS devices are built on a thin layer of crystalline silicon. This thin layer of silicon is isolated from the parent Si substrate by a thick buried oxide, SiO$_2$, layer leaving the devices electrically isolated from the underlying substrate. SOI MOSFETs can be categorized into partially depleted (PD), fully depleted (FD) and dynamic depleted (DD) MOSFETs based on the depletion layer thickness as compared to Si body thickness.

In case of PD SOI MOSFETs silicon film thickness is larger than the maximum depletion depth under the gate as shown in Fig. 1.3 (a). In this case there is no interaction between the two depletion regions formed by the front gate and back gate bias conditions, and there exists a region of neutral silicon in between the front and back depletion regions. The top-gate bias is used to control the inversion layer, whereas the back-gate is usually grounded to form a typical SOI MOSFET. The neutral substrate, called “body”, may be connected to a body bias [body contacted (BC)] or kept floating [floating body (FB)]. When this body is connected to a particular bias, the characteristics of the device become exactly same as that of the bulk device and PD SOI MOSFETs essentially behave like a bulk MOS device. When this body is left electrically floating, these devices shall essentially operate like a bulk MOSFET, together with two important parasitic effects [27]. The first one is kink effect or floating body effect, and second one is the presence of parasitic open base NPN bipolar transistor between source and drain which essentially increases the leakage current through silicon controlled rectifier effect (SCR), named as latch-up, in PD SOI MOS device. With clever circuit design the PD SOI offers lower parasitic capacitance at the source/drain nodes in an inverter circuit, and exhibit lower self-capacitances and higher
Fig. 1.3 Schematic diagrams of (a) a partially depleted SOI MOSFET and (b) a fully depleted SOI MOSFET.

switching speeds. However, PDSOI runs into similar troubles as with the bulk MOSFET’s with respect to scaling and hence may not be a scalable technology for future generations.

On the other hand if the silicon substrate is thinned down such that the semiconductor film under the gate is completely depleted in the OFF state of the device, then the SOI MOSFET is referred to as a FDSOI MOSFET. By eliminating the floating substrate region, the parasitic effects are suppressed in the FDSOI MOSFET. FDSOI MOSFETs have received significant attention because of their superior performance over the PDSOI and bulk- silicon MOSFETs. Because of very thin silicon substrate, FDSOI devices offer reduced short channel effects, smaller leakage current and elimination of latch up. Further, by increasing the buried oxide thickness, essentially ideal sub-threshold slopes of 60mV/decade may be achieved. But, with a thick buried oxide the source-channel barrier height is reduced with increased value of drain to source voltage. Use of thin buried oxide can mitigate this problem by terminating the drain field lines on the back substrate at the cost of degraded sub-threshold slope.
1.1.1.2. Multi-Gate MOSFETs

The stronger electrostatic control of gate over the inversion channel can be achieved by increasing the number of gates from single-gate FDSOI to double gate (DG) SOI, FinFET, surrounding gate and gate all around (GAA) MOSFET [28-30]. Multiple gate MOSFETs (MG-FETs) may be thought of as an extension to the ultra-thin body FETs or the fully depleted SOI FETs but with more than one gate around the thin silicon body. In DGMOSFETs the channel is controlled by both front- and back gates. Because of the increased gate control, larger Si-film thickness can be used as compared to a FDSOI having the same gate length to achieve similar OFF state performance. On the other hand, because of the increased electrostatic control, further scaling of the channel length is possible. More gate control and so the improved short channel effects (SCEs) can be achieved using FinFETs and GAA-MOSFETs. The improvements of SCEs in MG-FETs let the channel to be lightly doped as compared to single-gate FETs. The reduced channel doping results in lower average electric field in the channel and so the improvement in carrier mobility in the channel is achieved which in turn increases the drive current of the device. The combinations of thin body and light body doping concentration yield steeper sub-threshold swing, and lower junction and body capacitances thereby offering lower gate delay in circuit applications. One of the most feasible multi-gate configurations in terms of being manufacturable is the FinFET. Fig. 1.4 shows the schematic of a FinFET structure where the gate controls the channel along the silicon sidewalls of the fin.

1.1.1.3. Source/ Drain Engineering

The author has already discussed scaling rules in section 1.1. However, the supply voltage, $V_{DD}$, scaling has been delayed as shown in Fig. 1.5 because MOSFET terminal
characteristics, particularly, the sub-threshold current exhibits wide variation with change in temperature [31]. The ideal subthreshold swing (SS) is limited to \((kT/q)\ln(10)\) or 60 mV/decade at room temperature 300 K. For a given off-state current \(I_{OFF}\) and threshold voltage \(V_{TH}\) as \(V_{DD}\) is reduced the on-state current \(I_{ON}\) reduces due to trimmed down gate overdrive \(V_{GT} = V_{GS} - V_{TH}\). Similarly, maintaining the same \(I_{ON}\) at reduced \(V_{DD}\) leads to the reduction of \(V_{TH}\) and thereby increasing \(I_{OFF}\), which consequently offers higher standby power dissipation. Either way, \(V_{DD}\) scaling is necessary in order to reduce power density on an IC maintaining both \(I_{ON}\) and \(I_{OFF}\) to specified values.
Fig. 1.5 ITRS specifications of supply voltage ($V_{DD}$) with corresponding year for high performance (HP) devices.

Thus, to the device designer, the one of the major challenges of CMOS scaling is to keep $I_{ON}$ as high as possible keeping a constant $I_{OFF}$ while scaling $V_{DD}$. The resistance associated with the source/drain (S/D) extensions and also in the channel is one of the pressing challenges to preserve high $I_{ON}$. This means that the desired $I_{ON}$ can be achieved by reducing or eliminating resistance associated with the source/drain and channel regions without sacrificing MOSFET switching integrity, regardless of the device structure in question (e.g., planar bulk, SOI, multi-gate MOSFETs, etc.). Reduced channel length $L_G$ may reduce the channel resistance due to the shorter path length between the source and drain regions. Further reduction of channel resistance is possible through strain...
engineering or alternative substrate materials. However, the source/drain extension junction depth $X_{j,SDE}$ must scale with $L_G$ in order to maintain switching integrity. One solution to alleviate the problem of resistance associated with the S/D is to replace the ohmic contacts on highly doped junctions by metallic extensions. This approach readily takes advantage of the reduced sheet resistance of metal compared to heavily doped junctions and also benefits from atomically sharpened metal/semiconductor junctions. Series resistance can be reduced further using Schottky contacts on highly doped substrate. Metallic source and drain allows for the reduction of short channel effects without the added complexity of using other techniques such as shallow S/D extensions, halo implants etc. The use of metallic source and drain which leads to Schottky barrier FETs is immune to parasitic bipolar actions like latch-up. Furthermore the low-thermal budget, abrupt metal/semiconductor junctions, integration on novel bulk semiconductors and the overall ease of fabrication make these devices a viable solution for the deca-nanometer range. The idea of metallic source/drain (MSD) CMOS, is nothing new. The first MSD MOSFET using PtSi source/drain regions in lieu of doped source/drain was published in 1968 to demonstrate silicon channel pMOSFET behavior [32]. This device utilizes advantages of both MSD MOSFETs and Schottky barrier (SB) MOSFETs. The first actual surge in SB-FET research however came in the 80s with the introduction of the first SB-NMOS device [33]. Because of the advantages of implementing SB-FETs in advanced and simple process technology [34] compared to that for conventional MOSFETs new surge of attention in these devices was awoken and SB junctions have since been incorporated in everything from the standard symmetric SB-MOSFETs [35] to FinFETs [36]-[37] and nanowires [38].
1.1.2. New Channel Materials

Novel materials are explored with a view to using them in different regions of the device structure to achieve high switching speed under acceptable power consumptions. In recent years materials scientists as well as device engineers introduce more and more new materials in order to keep up with performance scaling [39]-[43]. The drain current in saturation ($I_{D_{\text{Sat}}}$) normalized to channel width ($W$) can be written as $I_{D_{\text{Sat}}}W = C_{ox,inv}V_{GT} v$, where $C_{ox,inv}$ is the effective gate capacitance in the strong inversion region of operation, $V_{GT}$ is the gate overdrive voltage and $v$ is the velocity of carriers in the channel, either electrons or holes. The improvement of the drive current requires enhancement of carrier velocity, either in the mobility limit (where carrier velocity $v = \mu(E)E$ or in the ballistic limit (where the velocity $v = v_{\text{inj}}$). For extremely scaled MOSFETs where the channel length is less than the mean free path of the carrier in the channel, the carrier moves with the velocity at which it is injected at the source end, the injection velocity. The injection velocity of the carriers being inversely proportional with carrier effective masses in the transverse direction, the drive current can be increased by using channel materials having lower carrier effective masses in the transverse direction. Table 1.3 summarizes the important material and electrical properties of high carrier mobility bulk Gr. IV and III-V compound semiconductors along with Si. A clear trade-off between dominant carrier mobility and band gap is seen in Table 1.3. Narrow band gap materials offer enhanced carrier mobility but suffer from high junction leakage and band to band tunneling. The main advantage of a semiconductor with a small transport mass under ballistic condition is its high injection velocity. However, these materials also have a very low density of states, which tends to greatly reduce the inversion charge and hence reduce the drive current.
### Table 1.3 Material Properties of Bulk Semiconductors

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Ge</th>
<th>Si</th>
<th>GaAs</th>
<th>InAs</th>
<th>InSb</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap, ( E_g ) (eV)</td>
<td>0.66</td>
<td>1.12</td>
<td>1.42</td>
<td>0.354</td>
<td>0.17</td>
<td>1.34</td>
</tr>
<tr>
<td>Electron affinity, ( \chi ) (eV)</td>
<td>4.05</td>
<td>4.0</td>
<td>4.07</td>
<td>4.9</td>
<td>4.59</td>
<td>4.38</td>
</tr>
<tr>
<td>Intrinsic carrier concentration (cm(^{-3}))</td>
<td>2.4×10(^{13})</td>
<td>1.5×10(^{10})</td>
<td>2.1×10(^{6})</td>
<td>1.1×10(^{15})</td>
<td>2.1×10(^{16})</td>
<td>1.3×10(^{7})</td>
</tr>
<tr>
<td>Effective density of states in conduction band, ( N_C ) (cm(^{-3}))</td>
<td>1.02×10(^{19})</td>
<td>2.8×10(^{19})</td>
<td>4.35×10(^{17})</td>
<td>8.7×10(^{16})</td>
<td>4.2×10(^{16})</td>
<td>8.6×10(^{7})</td>
</tr>
<tr>
<td>Effective density of states in valence band, ( N_V ) (cm(^{-3}))</td>
<td>5.6×10(^{18})</td>
<td>1.04×10(^{19})</td>
<td>7.57×10(^{18})</td>
<td>6.6×10(^{18})</td>
<td>7.3×10(^{18})</td>
<td>5.7×10(^{17})</td>
</tr>
<tr>
<td>Density of states effective mass for electrons (( m_e^{*} ) dos/m(_0))</td>
<td>0.55</td>
<td>1.06</td>
<td>0.067</td>
<td>0.026</td>
<td>0.0135</td>
<td>0.0795</td>
</tr>
<tr>
<td>Density of states effective mass for holes (( m_h^{*} ) dos/m(_0))</td>
<td>0.37</td>
<td>0.56</td>
<td>0.47</td>
<td>0.574</td>
<td>0.432</td>
<td>0.6</td>
</tr>
<tr>
<td>Hole mobility, ( \mu_h ) (cm(^2)V(^{-1})s(^{-1}))</td>
<td>1900</td>
<td>450</td>
<td>400</td>
<td>480</td>
<td>1250</td>
<td>150</td>
</tr>
<tr>
<td>Electron mobility, ( \mu_e ) (cm(^2)V(^{-1})s(^{-1}))</td>
<td>3900</td>
<td>1450</td>
<td>8500</td>
<td>40000</td>
<td>77000</td>
<td>4600</td>
</tr>
<tr>
<td>Dielectric constant, ( k )</td>
<td>16.0</td>
<td>11.9</td>
<td>12.9</td>
<td>15.15</td>
<td>17.7</td>
<td>12.4</td>
</tr>
<tr>
<td>Melting point, ( T_m ) (°C)</td>
<td>937</td>
<td>1412</td>
<td>1240</td>
<td>942</td>
<td>527</td>
<td>1060</td>
</tr>
</tbody>
</table>
1.2. Why Ge?

Ge is the most promising material for pMOSFETs with the highest hole mobility (1900 cm²/V.s) among all the semiconductors. Hole mobility of Ge is almost 4.3 times higher than that of Si. Ge also offers a lower effective mass for both electrons and holes thereby resulting in a high injection velocity for both carriers. Thus drive current can be enhanced both in the mobility limit and ballistic limit by using Ge as the channel material. The other advantages of Ge over other materials are— compatibility to already developed silicon process technology making the low fabrication cost, low energy bandgap which enables further scaling of power supply voltage and low temperature process due to lower melting point (~940°C) as compared to silicon (~1400°C) permitting reduced thermal budget. The lower-than-Si band gap of Ge allows lower contact resistance with metal contacts due to the smaller barrier height. The low thermal budget processing is especially attractive for high-k/metal gate technology because low thermal budget can maintain the integrity of the gate stack and three dimensional (3D) integrated circuit technologies. For pMOSFET applications, Ge provides highest bulk hole mobility. At the same time, its bulk electron mobility is approximately two times higher than in silicon which is high enough to obtain high performance nMOSFETs. On the basis of the data in Fig. 1.5, the most promising material for the future CMOS device is Ge since it offers lowest electron and hole mobility ratio allowing matched p- and n-MOSFET performance which would be a unique feature.

Nevertheless several critical issues of Ge technology are far from being settled. Some decisive aspects of using Ge in MOSFETs are: lack of a thermally and chemically stable native oxide, poor interface properties, limited electron mobility gain with respect to strained-Si, high reactivity of Ge towards surrounding materials, difficult n-type doping, lattice mismatch with Si, a small bandgap which is responsible for enhanced leakage and
Fig. 1.6 The mobility landscape of semiconductors. The bulk mobility is plotted against the bandgap for silicon, germanium and a variety of group III–V materials. Filled symbols indicate electrons, and open symbols indicate holes. Germanium offers the highest hole mobility of any known semiconductor material [44].

high permittivity resulting in early onset of short channel effects (SCEs) [45]. However, the interface property has been improved considerably [46]-[47] with the adoption of elegant passivation schemes such as an ultra-thin epitaxial layer of Si and thermally grown GeO$_2$ along with suitable high-k dielectric materials like HfO$_2$, ZrO$_2$ etc. The use of ultrathin Si interfacial layer [48]-[49] is the most effective passivation technology with significant progress. Another opposing force with Ge is the significantly low energy bandgap which results in high OFF-state leakage current ($I_{OFF}$) due to band-to band tunneling (BTBT). There are two major strategies for resolving the energy bandgap ($E_g$) challenges with Ge. The first is to use low power-supply voltage ($V_{sup}$) with $V_{sup} < E_g$. The second approach is to fabricate these devices in a quantum-confined system (for example, an ultrathin body or nanowire) where the quantum confinement generates strong quantization of the energy levels and effectively offering a larger bandgap hence reducing OFF-state leakage current.
It is found that germanium (Ge) is a potential semiconductor for the next generation electronic and optoelectronic devices. In conjunction with other group IV materials - silicon (Si) and silicon-germanium alloy (Si$_x$Ge$_{1-x}$), Ge has produced high-speed transistors [44], [50]-[51] as well as photonic devices such as photo-detectors [52]-[53] and also modulators [54]. The band gap and strain engineering play a vital role in optimizing the performance of Ge-based devices similar to Si CMOS technology. For example, over two times enhancement in hole mobility can be obtained by applying compressive stress to Ge [55]-[56]. Similarly, tensile strain is required to enhance the electron mobility in Ge [57]. The incorporation of tin (Sn) into substitutional states germanium (Ge) lattice materializes the semiconducting Ge$_{1-x}$Sn$_x$ alloy which is another possible route for engineering the electronic properties of Ge. Ge$_{1-x}$Sn$_x$ alloy exhibits two promising properties: - a direct band gap for Sn concentration starts around 9% and the potentiality to further increase the hole and electron mobilities by inducing strain due to the lattice mismatch with Ge [58]-[59]. The prospect of attaining high electron and hole mobilities in the Ge$_{1-x}$Sn$_x$ alloy rationalizes the research interest in developing Ge$_{1-x}$Sn$_x$ for high speed transistor applications. Accordingly, Ge$_{1-x}$Sn$_x$ alloys provide a common material platform for enabling convergence of high-speed logic and optoelectronic devices for future integrated circuits. The technological importance of Ge$_{1-x}$Sn$_x$ devices is further amplified by the fact that they can be integrated monolithically on a low-cost Si platform. From a device design perspective, GeSn alloys expand the design space beyond Si, Ge and SiGe for greater flexibility in band gap and strain engineering. The bandgap of GeSn materials is even smaller than that of Ge. Therefore one can expect that those difficulties will also be present, possibly with a larger impact, when applying the technique on GeSn MOS structures.
1.3. Review of Work on Ge MOSFETs

Fabrication of Ge channel MOSFETs consists of three main steps – processing of Ge substrate, formation of gate stacks, and also source/drain contacts. There have been extensive work reported in the literature on Ge channel MOSFETs, which include process techniques of Ge, characterization of Ge film and Ge channel MOSFETs, modeling and simulation of Ge MOS devices. Works carried out in different fronts are described in the following sub-sections.

1.3.1. Ge MOSFET Substrate Preparation

Given the advanced state of silicon manufacturing technology, it is very likely to use silicon as the platform in mainstream manufacturing. In order to realize Ge CMOS fully compatible to Si VLSI technology, Ge active layer has to be grown on Si substrate. Due to the 4.2% lattice mismatch between Ge and Si with a larger lattice constant of Ge, thickness of Ge greater than the critical thickness results in a relaxed Ge layer, which exhibits lower mobility. So, a thick pseudomorphic Ge layer cannot be grown on top of Si substrate directly due to large lattice mismatch between Ge and Si [60]. Hence an extremely thin film of Ge with its thickness lower than the critical thickness can be grown pseudomorphically on Si resulting in a Si-Ge heterostructure. T. Irisawa et al., have grown Si$_{0.3}$Ge$_{0.7}$/Ge/Si$_{0.3}$Ge$_{0.7}$ heterostructures with a drastic increase of room temperature Hall hole mobility up to 2100 cm$^2$/Vs in the strained Ge channel and improved device characteristics of the strained Ge channel MOSFET [61]. One of the novel growth techniques of Ge is multiple hydrogen anneal hetero-epitaxy (MHAH) which utilizes a combination of low and high temperature growth combined with hydrogen annealing [62]. First, the low temperature process at slow growth rate is performed to obtain smooth Ge layer growth with small surface roughness. Then a thicker Ge layer is grown on the
1.3.1. Ge MOSFET Substrate Preparation

underlying seed Ge layer at high temperatures. Multiple hydrogen annealing and growth confine misfit dislocations near the Ge–Si interface not threading to the surface as expected in this 4.2% lattice-mismatched system. Ammar Nayfeh and his group fabricated high-performance germanium p-MOSFETs directly on Si using MHAH growth technique with effective hole mobility as high as 250 cm²/Vs [62]. The quality of epitaxial Ge layer on Si can further be improved by applying selective MHAH growth. Hyun-Yong Yu et al., reported ~ 80% enhanced hole mobility of Ge p-MOSFETs with high-\(k\) dielectric and metal gate by the selective MHAH technique as compared to the Si hole universal mobility [63]. A variety of growth techniques, such as molecular beam epitaxy [64]-[66], chemical vapour deposition [48], [67] and ultra-high-vacuum chemical vapour deposition [68]-[69] have been employed for growing germanium on silicon substrates. Because of higher dielectric constant of Ge than Si, Ge MOSFET exhibits pronounced short channel effects (SCEs). To obtain better electrostatic control for aggressively scaled MOSFETs ultrathin body GeOI structures or multigate structures are required.

![Crystalline Ge](Image)

**Fig. 1.7 Multiple hydrogen anneal heteroepitaxy (MHAH) of Ge on Si [62]**
Few promising techniques in preparing GeOI substrate are discussed in the following.

(i) Wafer bonding and etch-back technique are used to fabricate GeOI substrates when a thick layer of the substrate is required. A detailed description of wafer bonding and etch-back approaches for strained Si, SiGe, and Ge on-insulator is found in [70] with low threading dislocation densities and precise control over layer thickness. Room temperature bonding and etch-back scheme are presented in [71] eliminating the requirement for intermediate chemical mechanical polishing or subsequent long time annealing steps of typical wafer bonding techniques.

(ii) Smart-Cut process, originally developed to manufacture SOI, has achieved a high degree of maturity with mass production. The potential of Smart-Cut expands the range of applications from conventional hetero-epitaxy to single crystal thin film transfer to any type of substrate. Formation of GeOI substrate from Ge bulk wafers by the Smart-Cut™ technology with thickness from 200 mm down to 40 nm has been demonstrated in [72] in which GeOI MOSFET showed electron and hole mobilities of 300 and 350 cm²/V.s, respectively, and interface-trapped charge density of $5 \times 10^{12}$ cm⁻² eV⁻¹ at the Ge/BOX interface. A 200 mm GeOI formation from Ge bulk wafers has also been demonstrated using the Smart-Cut™ technology [73].

(iii) Ge condensation technique in SiGe layer is used for the formation of GeOI substrate [74]-[75]. Enhanced mobility of both electrons and holes are achieved in integrated Ge-rich s-SGOI (GOI) PMOSFETs with s-Si/SGOI NMOSFETs or UTB-SOI NMOSFETs against the universal mobility for Si p- and n-MOSFETs [74]. This technique starts from SiGe on insulator (SGOI) substrate and utilizes selective oxidation of Si in a SiGe layer where Si is selectively oxidized by thermal oxidation thereby increasing Ge concentration in the SiGe layer. Finally almost 100% Ge layer is formed on substrate
oxide. By utilizing this technique, almost 10x higher hole mobility has been achieved, which is comparable with SOI n-MOSFET electron mobility [74]. Planar Ge pFETs and Si nFETs were fabricated using a low temperature process (<600°C) with high-K and metal gate by the local Ge enrichment technique on SOI wafers. Functional Ge- and Si channel transistors (with gate length down to 160 nm). This hybrid CMOS integration exhibits excellent mobility of 275 and 142 cm²/Vs for electrons (Si) and holes (Ge), respectively [76].

(iv) Liquid phase epitaxy or rapid melt growth can be employed to grow an amorphous Ge layer on an insulator with seed pattern. The Ge film is then etched in the form of narrow patterns followed by rapid thermal annealing [77]-[78]. Liu et al. [77] developed a method to form GeOI based on liquid-phase epitaxy growth on Si substrates and a defect necking technique in which defects are confined within very short distance.

(v) Selective epitaxial growth of thin Ge layer in shallow trench isolation (STI) regions is of great interest in advanced devices due to the good lateral electrical isolation of shallow trenches and the possibility of integrating Ge on Si wafers. G. Wang et al. [79] reported facet-free growth of Ge in shallow trench isolated Si windows with an acceptable threading dislocation density (TDD) of 4.2×10⁸ cm⁻².

1.3.2. Gate Stacks in Ge MOSFETs

The first semiconductor device was made using germanium [80]. Despite that, Si has been the mostly prevalent in LSI/VLSI technologies because Si has a chemically and electrically stable oxide SiO₂ while Ge oxides are water soluble and desorbs at low temperatures [81]. The earlier studies of Ge MOS devices on the basis of deposition of SiO₂ on germanium by chemical vapour deposition [82] showed marked signatures of interface trap states with significantly degraded carrier mobility. Ge attracted attention
recently when high-k/metal gate technologies were under research and development [83]. High-k/metal gate is one of the key technology enabler for sub-22 nm technology node [84]. It suppresses short channel effects and improves device performance by decreasing equivalent-oxide-thickness (EOT), without increasing the gate leakage current density. Si process typically requires high thermal budget especially for source/drain dopant activation. This high thermal budget degrades the chemical and electrical properties of high-k/metal gate. Therefore, Ge is more suitable material for high-k/metal gate technology because Ge allows low thermal budget processing due to its lower melting point. However, introduction of high-k was very challenging with the associated defect control – which was responsible for reduction of carrier mobility and degradation of device reliability. Good known high-k gate dielectrics for use on Ge channel devices are GeO$_2$, GeON, HfO$_2$, ZrO$_2$ and ALD-Al$_2$O$_3$ [85-89]. S. C. Martin et al. [85] reported a peak room temperature channel mobility of 770 cm$^2$/V.s in a p-channel Ge MOSFET using GeO$_2$ as the gate dielectric. Interface state densities of the order of $8 \times 10^{12}$ cm$^{-2}$eV$^{-1}$ is reported by P. Batude et al. [86] in a Ge/GeON/HfO$_2$/TiN stack. The high resolution cross-sectional TEM image shows the high quality GeO$_x$N$_y$/epi-Ge interface and the Ge single crystal atomic lattice [62]. The ALD-Al$_2$O$_3$/Ge interface states of $8 \times 10^{11}$ cm$^{-2}$eV$^{-1}$, the peak mobility of 225 cm$^2$ V$^{-1}$s$^{-1}$ and on-/off-current ratio exceeding $10^3$ for the p-MOSFET with W/L = 100 μm/4 μm is reported in ref. [87]. Germanium MOS capacitors with a thin layer of ZrO$_2$ with EOT of 2.2 nm were fabricated which exhibit the subthreshold slope as low as 100 mV/decade [88]. HfO$_2$ acts as a promising high-k material on top of Si to create good interface properties. HfO$_2$ with EOT of 0.97 nm is used as high-k gate dielectric using a novel remote plasma-assisted chemical vapor deposition technique [89].
1.3.3. **Surface Passivation Schemes for Ge MOSFETs**

In order to improve interface properties of high-k/Ge MOS gate stack, surface passivation has been widely studied. Since native oxide of Ge is chemically/electrically unstable, alternative surface passivation on Ge without increasing EOT has been extensively explored. Various kinds of surface passivation methods were proposed, such as interlayer of GeON, GeN [90], Si [91] and ozone oxidation. Although Ge oxide is unstable, it can be stabilized by incorporating nitrogen as GeON or GeN. Nitrogen incorporation also contributes to the increase of the dielectric permittivity at the interface gate dielectric. The drawback of nitrogen incorporation is that nitrogen generally causes oxide defects such as dangling bonds and fixed charges which degrade carrier mobility similar to SiON and SiN in Si [92]. Ozone oxidized GeO$_2$ [93] followed by high-k dielectric has also been investigated and exhibited $D_{it}$ on the order of $10^{11}$ cm$^{-2}$eV$^{-1}$. 0.7–0.8 nm HfO$_2$/Al$_2$O$_3$/Ge gate stack has been fabricated with Dit as low as $10^{11}$ cm$^{-2}$ eV$^{-1}$ [94]. An epitaxial Si layer provides a very clean interface between Si and Ge [95]. This Si passivation layer is oxidized and SiO$_2$ is formed with a stable interface between SiO$_2$ and Si. The possible concerns about Si passivation are (a) inefficient EOT scaling by finite thickness of a Si layer and (b) acceptable valence band offset between silicon and germanium, works only for hole confinement.

1.3.4. **Source/Drain Junctions and Contacts in Ge MOSFETs**

Both n-type and p-type dopants in Ge have been investigated [96]. It has been understood that p-type dopant diffusion is slow in Ge. Hence shallow junction formation is relatively easier with p-type dopants rather than n-type dopants. On the other hand, p-type dopants have lower solid solubility and lower activation rate in typical rapid thermal anneal process. In addition, n-type dopant diffusion is fast in Ge and it is quite challenging to achieve shallow junctions for n-MOSFET. This n-type dopant characteristic is
problematic not only for making S/D in n-MOSFETs but also for channel implant in p-MOSFETs. Especially, steep profile of halo pocket doping is required to suppress the short channel effect. However, since n-type dopants diffuse fast, halo doping broadens and unintentionally increases channel doping concentration, which may cause severe mobility degradation in Ge p-MOS devices [51]. To achieve shallow/highly activated junction, more elaborate source/drain activation technique may be needed. In addition the poor n-type dopant activation and diffusion lead to reduction of active surface n-type doping, resulting in higher contact resistance. The resistance associated with the source/drain (S/D) extensions is one of the pressing challenges to preserve high on-current. One solution to alleviate the problem of high resistance associated with the S/D is to replace the ohmic contacts on highly doped junctions by metallic extensions. This approach readily takes advantage of the reduced sheet resistance of metal compared to heavily doped junctions and also benefits from atomically sharpened metal/semiconductor junctions.

1.3.5. Modeling and Simulation

Screening of recent literature unveils that Ge-channel MOS devices are of great interest to researchers in academia and industry at advanced technology nodes. The efficiency and accuracy of model pertaining to these devices may be gauged in terms of its speed and margin of accuracy to predict the device characteristics. The choice of proper models determines the efficiency of simulation results. Only a few reports on modeling and simulation of Ge MOS devices are available in the literature [97]-[102]. Vita Pi-Ho Hu et al., [97] investigated the impacts of box thickness, channel thickness and back-gate bias on the electrostatic integrity for the UTB GeOI MOSFET by means of an analytical solution of Poisson’s equation verified with TCAD simulation. Bhattacherjee and Biswas
[98] studied the electrical behavior of symmetric double gate Ge MOSFET based on the solution of Poisson–Boltzmann equations considering the effect of interface-trapped charge density and Pao-Sah’s current formulation. A consistent parameter set applicable to Ge pMOSFET simulation is extracted to incorporate in commercial TCAD simulation tools [99]. Simulations of germanium-on-insulator fully-depleted pMOSFET have been carried out from process to device using Silvaco software [100] and compared with experimental results to study trap densities at both top and bottom interfaces and to extend TCAD mobility model from silicon to germanium [101]. Process and device simulations have been performed to investigate the substrate bias sensitivity of Ge pMOSFETs with halo implantation [102].

1.4. Untouched Areas

In all designs – either a device or a circuit or a system the prototypes are verified through the use of appropriate models/ simulators before being reproduced in real design to detect errors early in the design process and to avoid the costly and time consuming prototyping. The choices of proper models can accurately predict the performance of a CMOS design and describe the behavior of the transistors in the circuit. The device models used to mimic the behavior of devices essentially determine the accuracy and speed of the circuit simulation. The challenge faced by device model developers is the formulation and efficient numerical implementation of physically-based models that are predictive for practical device structures.

However, analytical modeling and simulation studies on Ge channel MOSFETs are still at their infancy. Studies in this area are important and timely, and constitute the line of investigation in the present research topic.
1.5. **Scope of the Present Work**

The aim of this dissertation is to develop accurate analytical models for the high performance nanoscale Ge channel MOSFETs for various device architectures in order to study the short channel effects in terms of different device parameters such as threshold voltage ($V_{TH}$), subthreshold slope ($SS$), and drain-induced barrier lowering ($DIBL$) and also to evaluate the device parameters related to analog and RF applications such as transconductance, output conductance, voltage gain, cut-off frequency, and maximum frequency of oscillations. Furthermore, the thesis includes the numerical simulation of ultra-thin body Ge channel p-MOSFETs in order to determine various analog and logic circuit parameters for system-on-chip applications.

1.6. **Organization of the Thesis**

This dissertation is organized in total 6 Chapters and is outlined as follows:

**Chapter 1** reviews and briefly discusses various aspects of high performance Ge-channel MOS devices with a view to replacing conventional Si MOSFETs.

**Chapter 2** deals with the control of short channel effects in germanium MOSFETs by employing halo implants in both source channel and drain channel junctions in the presence of interface-trapped charge and fixed-oxide charge densities. The halo implant involves incorporation of impurities that are the same polarity to substrate while having a high level of concentration with respect to substrate so that the depletion width in the channel may be reduced. Different device parameters like threshold voltage $V_{TH}$, drain induced barrier lowering $DIBL$ and subthreshold slope $SS$ of Ge MOS devices are calculated based on the solution of 2D Poisson’s equation subject to suitable boundary conditions [103-104].
Chapter 3 presents the drain current model for nanoscale GeOI MOSFETs based on 2D channel potential using the non-charge sheet formulation taking into account the effects of the fixed and interface-trapped charge densities. This model is employed to evaluate various device parameters related to analog and RF applications such as transconductance, output conductance, voltage gain, unity gain cut-off frequency, and maximum frequency of oscillations for both GeOI and equally-sized SOI devices. Furthermore, the device parameter associated with digital circuit applications such as gate delay is presented for both GeOI and SOI devices [105-106].

Chapter 4 describes a compact model for drain current of nanoscale fully depleted GeOI devices based on 2D surface potential approach. The model is valid in all regions of device operation. The present model takes into account the effect of interface-trapped charge and fixed charge densities, and also includes velocity saturation, channel length modulation, carrier mobility degradation, and drain induced barrier lowering [107-108].

Chapter 5 reports the effect of different source, drain and gate engineering on the electrical behavior of GeOI MOSFETs for mixed signal system-on-chip (SoC) applications.

In the first part of Chapter 5, the impact of different work function profiles of the gate material on the short channel effects and also on the analog and logic performances of ultra-thin body GeOI MOSFETs is studied at channel length of 30 nm [109-110].

In the next part of Chapter 5 impacts of metal source/drain (S/D) contacts on GeOI MOSFETs with high-k gate dielectric and metal gate are investigated [111].

Finally an overall contribution of this dissertation is summarised in Chapter 6.
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