CHAPTER 6
IMPLEMENTATION OF 6T SRAM MEMORY CIRCUIT
WITH HIGH-K DIELECTRICS BASED DMSGJLT

6.1. INTRODUCTION

In this unit the dual metal surround gate junctionless transistor is been implemented with different high-k dielectrics. The leakage characteristics analysed in the previous unit is been analysed in detail by obtaining the energy band diagram in the subthreshold region. The tunnelling path is taken for SiO$_2$ and HfO$_2$ gate dielectrics. It is found that the tunnelling path in the drain region is high for HfO$_2$ than SiO$_2$ in the subthreshold state. The energy gap between Fermi level and conduction band is found to be high for HfO$_2$. Due to this the band to band leakage current will also be less with high-k dielectrics. The capacitance of the device also increases with increase in k value of the gate dielectric. Due to the increase in the capacitance the charge holding capability of DMSGJLT is high with HfO$_2$ gate dielectrics. Thus the possibilities of charge leakage reduces and hence DMSGJLT gives improved memory performance with HfO$_2$ gate dielectrics for 6T SRAM.

6.2. DEVICE STRUCTURE

The dual metal structure with work function of 4.97 eV for the first gate and 4.27 eV for the second gate is shown in Figure 6.1. The length of the first and
second gate is \( L_1 = L_2 = 20 \) nm. The doping concentration of the centre silicon rod is taken to be \( 2 \times 10^{19} \) cm\(^{-3} \) throughout the device.

The conventional SiO\(_2\) gate dielectric has large band gap of about 9 eV hence it used as gate dielectric for years. But now due to extensive scaling of device the oxide thickness becomes 2 nm. The device is formed by replacing SiO\(_2\) with other high-\( k \) dielectrics.

6.3. RESULTS AND DISCUSSION

Figure 6.2 shows the band diagram of DMSGJLT with both SiO\(_2\) and HfO\(_2\) gate dielectric in off State. The similar band structure analysis has been made in (Suresh et al., 2012 & Haijun lou et.al., 2013). It is found that the conduction band of HfO\(_2\) based DMSGJLT is elevated to higher energy level than SiO\(_2\) based device. This is due to the fact that, for HfO\(_2\) gate dielectric, as the dielectric constant increases, it renders more resistance to the device active region in the off state. It is also found that the tunneling path for HfO\(_2\) is found to be higher than SiO\(_2\). Hence the HfO\(_2\) based device gives more isolation for tunneling of electron in the drain region.
Figure 6.2 Energy band in channel region in off state for SiO$_2$ and HfO$_2$ gate dielectrics

The Figure 6.3 shows the distance between Fermi level and conduction band of channel region of both HfO$_2$ and SiO$_2$ based DMSGJLT.

Figure 6.3 Energy Band at Channel region showing distance between Fermi level and conduction band
It is known that Fermi level is an intermediate level, which has electrons. It is also found that as the dielectric constant of the gate dielectric increases the distance between Fermi level and conduction band increases. This reduces the direct band to band tunneling of electron for conduction in off state. This leads to the suppression of the tunneling leakage current, when high-k dielectrics is used.

The band diagram of various high-k dielectric such as SiO$_2$, Si$_3$N$_4$, Al$_2$O$_3$, Y$_2$O$_3$, HfO$_2$ and TiO$_2$ is taken separately.

![Figure 6.4 Energy gap between Fermi Level and Conductance band in channel region](image)

The energy gap between Fermi level and conduction band for various dielectrics is given in the Figure 6.4. It is found from the Figure 6.4 that as the dielectric constant increases, the resistive nature of dielectrics increases and the conduction band elevates to higher energy level. It is seen that HfO$_2$ shows 0.3424 eV increase in energy gap between Fermi level and Conduction band than SiO$_2$ in off state.
Figure 6.5 shows the capacitance variation with respect to gate source voltage of DMSGJLT for different high-k dielectrics.

![Graph showing capacitance variation](image)

**Figure 6.5 Gate capacitance variation with respect to gate source voltage**

Here the gate source voltage varies from -3 V to +3 V. It is found that as the dielectric constant of the gate dielectric increases the gate capacitance also increases. This is due to the dielectric constant of the gate dielectric increases the relative permittivity of the dielectric material increases. This improves the capacitance value as the dimension remains constant. Due to this the charge holding capability of the dielectrics increases as the total charge is proportional to the capacitance. It is also found from the charging, discharging plot from Figure 6.6 that as the dielectric constant increase, the discharge is slow. Hence the high-k dielectric such as HfO$_2$ is provide a better dielectric property for the device and improves its sub threshold performance and reduces its leakage current. Thus in the off state the tunneling of the electron from gate to the channel will avoided much when high-k dielectrics is used.
As the capacitance and the total charge increases the device will be well suited for memory application. Semiconductor Memories are classified according to the type of data storage and the type of data access mechanism into the following two main groups:

![Figure 6.6 Input voltage and output voltage with respect to time period](image)

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- Non-volatile Memory (NVM) also known as Read-Only Memory (ROM) which retains information when the power supply voltage is off. With respect to the data storage mechanism NVM are divided into the following groups:
  
  - Mask programmed ROM. The required contents of the memory is programmed during fabrication,
  
  - Programmable ROM (PROM). The required contents is written in a permanent way by burning out internal interconnections (fuses). It is a one-off procedure.
– Erasable PROM (EPROM). Data is stored as a charge on an isolated gate capacitor (“floating gate”). Data is removed by exposing the PROM to the ultraviolet light.

– Electrically Erasable PROM (EEPROM) also known as Flash Memory. It is also based on the concept of the floating gate. The contents can be reprogrammed by applying a suitable voltages to the EEPROM pins. The Flash Memories are very important data storage devices for mobile applications.

Read/Write (R/W) memory, also known as Random Access Memory (RAM). From the point of view of the data storage mechanism RAM are divided into two main groups:

– Static RAM (SRAM), where data is retained as long as there is power supply on.

– Dynamic RAM, where data is stored on capacitors and requires a periodic refreshment.

SRAM is one of the important memories because of its enhanced performance than other memories and its reliabilities. The SRAM is faster than DRAM and it consumes only less static power compared to DRAM.

There are four different types of SRAM they are

- 4 Transistor SRAM ie 4T SRAM
- 6 Transistor SRAM ie 6T SRAM
- 8 Transistor SRAM ie 8T SRAM
- 9 Transistor SRAM ie 9T SRAM

The 6T static Random Access Memory is an optimized form of SRAM because of its improved performance and simple operation. It circuit has been implementation in the following section.
6.4. 6T SRAM MEMORY CIRCUIT IMPLEMENTATION

Figure 6.7 shows the Circuit of 6T SRAM. The 6T SRAM circuit consist of 6 transistors with 4 NMOS and 2 PMOS transistors. 2 NMOS and 2 PMOS forms two inverter circuits. It has a bit line and word line.

![6T SRAM Circuit](image)

The major operation of 6T SRAM is given below.

**READ Operation**

Consider a data read operation, assuming that logic '0' is stored in the cell. The transistors M₅ and M₃ are turned off, while the transistors M₁ and M₄ operate in linear mode. Thus internal node voltages are \( V₁ = 0 \) and \( V₂ = VDD \) before the cell access transistors are turned on. After the pass transistors M₂ and M₆ are turned on by the row selection circuitry, the voltage CB of will not show any significant variation since no current flows through M₆. On the other hand M₁ and M₂ will conduct a nonzero current and the voltage level of...
CB will begin to drop slightly. The node voltage $V_1$ will increase from its initial value of '0'V. The node voltage $V_1$ may exceed the threshold voltage of $M_5$ during this process, forcing an unintended change of the stored state. Therefore voltage must not exceed the threshold voltage of $M_5$, so the transistor $M_5$ remains turned off during read phase.

**WRITE Operation**

Consider the write '0' operation assuming that logic '1' is stored in the SRAM cell initially. The transistors $M_1$ and $M_4$ are turned off, while $M_5$ and $M_3$ are operating in the linear mode. Thus the internal node voltage $V_1 = V_{DD}$ and $V_2 = 0$ before the access transistors are turned on. The column voltage $V_b$ is forced to '0' by the write circuitry. Once $M_2$ and $M_6$ are turned ON, we expect the nodal voltage $V_2$ to remain below the threshold voltage of $M_1$. The voltage at node 2 would not be sufficient to turn on $M_1$. To change the stored information, i.e., to force $V_1 = 0$ and $V_2 = V_{DD}$, the node voltage $V_1$ must be reduced below the threshold voltage of $M_5$, so that $M_5$ turns OFF.

![Figure 6.8 Hold Butterfly diagram of 6T SRAM with SiO₂ based DMSGJLT](image)

Figure 6.8 Hold Butterfly diagram of 6T SRAM with SiO₂ based DMSGJLT
The above circuit is implemented using DMSGJLT with SiO$_2$ and other high-k dielectrics. The performance of the memory circuit implemented is measured by calculating its read, write and hold noise margin. Figure 6.8 shows the hold butterfly diagram of SiO$_2$ based DMSGJLT. The individual butterfly diagram for the memory circuit with all the dielectrics are obtained and its noise margins are tabulated below.

Table 6.1 Performance Analysis of 6T SRAM Circuit Using DMSGJLT with Different High-k Dielectrics

<table>
<thead>
<tr>
<th>Materials</th>
<th>Read</th>
<th>Write</th>
<th>Hold</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SNM1</td>
<td>SNM2</td>
<td>SNM1</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>0.02444</td>
<td>0.04412</td>
<td>0.45197</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>0.0264</td>
<td>0.04812</td>
<td>0.5017</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>0.0294</td>
<td>0.05122</td>
<td>0.5312</td>
</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>0.0324</td>
<td>0.05612</td>
<td>0.5612</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>0.03456</td>
<td>0.06214</td>
<td>0.6214</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>0.06656</td>
<td>0.06414</td>
<td>0.6414</td>
</tr>
</tbody>
</table>

Table 6.1 shows the read, write and hold margin analysis of SRAM memory circuit implemented using DMSGJLT with different high-k dielectric material. Here SNM$_1$ is the signal to noise margin of first butterfly and SNM$_2$ is the signal to noise margin of the second butterfly. From the table it is clear that the write and hold noise margin is high for this device and read noise margin is comparatively less. It is also found that as the dielectric constant
increases the read, write and hold noise margin increases. It is found that from 
SiO₂ to HfO₂ the read noise margin shows an improvement of 41.4 %, whereas write noise margin shows 37.49 % improvement and hold noise 
margin shows 30.16 % improvement. From this it is clear that, high-k 
dielectric is best suited for memory application.

6.5. CONCLUSION

In this paper the Dual Metal Surround Gate Junctionless Transistor with 
high-k dielectrics has been proposed for improved leakage performance. The 
band to band leakage current is analysed by analysing the band structure of the 
region of intersection of gate oxide and channel. The tunnelling path increases 
as the dielectric constant increases. Thus tunnelling of electron will be much 
reduced with high-k dielectrics. The capacitance also found to show an 
improvement of 0.1 µF with HfO₂ than SiO₂. Due to the improvement in 
capacitance, the 6 Transistor SRAM also shows good performance with HfO₂ 
than SiO₂. The read, write and hold noise margin shows improvement with 
HfO₂ based device than SiO₂ based device.