CHAPTER 2
LITERATURE REVIEW

2.1. INTRODUCTION

The transistor is the building block of all electronic system. The invention of MOSFET provided an evolutionary change in the silicon industry. The device has to be continuously scaled in order to satisfy MOORE’S LAW according to which the number of transistors in a chip should be doubled every two years. The scaling of the conventional MOSFET leads to increase in sub-threshold leakage current which affects the device performance. This leads to the next type of device called silicon on insulator, i.e. a buried oxide layer is introduced in between the substrate and the channel which reduces the leakage current. Many works have been published in silicon on insulator structure (SOI) by (Ran-Hong Yan et al., 1992). The second gate is also introduced beyond the substrate region which is called back gate which provides some field in the lower region (T. Tanaka et al., 1991). The scaling of the SOI double gate MOSFET has been done for many years which results in shrinking of effective channel length which leads to less control of gate voltage to the device operation. Short channel effects that arise due to continuous scaling are avoided by means of an alternative structure named symmetrical Double Gate MOSFET. There are many works being carried out using DG MOSFET for the analog performance enhancement by (Qiang Chen et al., 2003).
The gate engineering technique partitions the gate as dual/triple metal gate as suggested and its fabrication techniques are specified in some articles by (Rupendra Kumar Sharma et al., 2009). Gate engineering gives considerable increase in the drain current characteristics. Some works have been reported by (N. Mohankumar et al., 2013) in channel engineering which includes doping of the channel region with different materials to improve the performance of the device. High k dielectric instead of SiO$_2$ gives an improvement in quantum performance as suggested by Nicolas Loubet et al., 2008, here metal gate is employed and fabricated successfully. As the device becomes smaller and smaller the source and drain region gets closer to each other such that even DGFET techniques fails to control the channel and SCE’s. Thus to have a better control over the gate voltage of the device tri-gate and surround gate structures are proposed.

2.2. TRI-GATE AND SURROUND GATE STRUCTURE

Steady miniaturization below 45 nm increases SCE’s, sub threshold leakage and gate dielectric effects hence tri-gate and surround gate devices are opted (S. K. Vishvakarma et al., 2010). Works have been published in cylindrical gate MOSFET (Pujarini Ghosh et al., 2012) and pi gate (J. T. Park et al., 2001) which gives an improved DIBL. Though this structure provides a superior performance over Short Channel Effects (SCE) this structure employs different gradient concentration across source and drain junctions. As the device is scaled down thoroughly to 20 nm regime formation of ultra-thin junction requires costly annealing technique making fabrication process difficult. Thus we go for transistor with electrostatically depleted channel. Moreover, the concentration gradient from source to drain is zero, which means device is uniformly doped from source to drain.

2.2.1. Junction-less Transistor

Junction-less transistors are also called vertical slit device or gated resistors. This device electrostatically depletes the channel to switch the
device by varying the work function difference between gate material and channel region. The conduction mechanism focuses on the bulk conduction of majority carrier and the transistor employing junctions like DG MOSFET, TGMOSFET, SGMOSFET when extremely scaled down faces many fabrication challenges. The concentration gradient in nm scale is required ranging from $1 \times 10^{19} \text{cm}^{-3}$ n-type doping for source, drain and $1 \times 10^{18} \text{cm}^{-3}$ p-type doping for channel region is needed to form the junction. For this costly millisecond annealing technique is needed for thermal budgeting (Jean-Pierre Colinge et al., 2009). This complicates the silicon industry to manufacture extremely thin silicon devices. The junction less transistor employs no junction (Chi-Woo Lee et al., 2009) the silicon layer has the same type of doping and doping concentration. This device is also discussed in other articles as vertical slit field effect transistor (Weis, M. et al., 2008), nanowire pinch off FET (Magnus et al., 2008) and junction less multi-gate transistor (J. T. Park et al., 2001) having the same operation. The junction less transistor will be the best alternative for future transistor fabrication (Cui, Y., Zhong et al., 2003). The major applications of junction-less transistor are in nonvolatile memory (Choi, S.-J et al., 2011), DRAM (Lee, C.-W. et al., 2010) and SRAM (Kranti et al., 2010). Many literature work mentions the advantages of junction-less transistor over inversion mode device (Lee et al., 2009, Vitale et al., 2010). The channel engineering in junction-less transistor has been done in (Yongbo Chen et al., 2013) which employs a slightly high doping near the drain side and thus gives improvement in $g_m$, $f_t$, gain etc which proves to be good for RF application. But the concentration gradient complicates the fabrication process. The dual material gate junction-less transistor is being presented in (Ratul K Baruah et al., 2014) which employs high-k spacer. The conventional junction-less transistor is reported to give less drain current and transconductance for a particular gate voltage when compared to IM device. The dual material gate junction-less transistor is reported to give higher drain
current and trans-conductance compared to other JLT. A triple material gate IM device is being proposed by (Angsuman Sarkar et al., 2012). This technique can also be implemented in junction-less transistor. The analysis of the different structures of junction-less transistor published so far is as follows.

2.3. DIFFERENT JUNCTION-LESS STRUCTURE

2.3.1. Junction-less SOI Transistor

Figure 2.1. Junction-less SOI Transistor (Elena Gnani et al., 2012)

Figure 2.1 shows the structure of SOI junction-less transistor (Elena Gnani et al., 2012). Above the bulk silicon substrate the buried oxide layer (BOX) layer is formed and on top of it silicon layer is formed. The drain and source contact is formed in the end of this layer. The silicon layer is doped with same type and concentration of the doping throughout. Above the silicon layer the gate dielectric is placed and followed by gate electrode. The gate electrode should have opposite work function when compared to the silicon this makes the device in the off state. The work function of the gate material should be high in the order of 5.2 ev. Doping of the device layer should be as high as $1.9 \times 10^{19}$ cm$^{-3}$. The direct gate tunneling can be avoided by using high-k dielectric stack. In this structure in the lower side the bulk silicon is available which provides some field to the device layer but due to the buried oxide layer the field is less which is considered in the next structure.
2.3.2. Bulk Planar Junction-less Transistor

The bulk planar Junctionless Transistor is shown in Figure 2.2. In this structure the device layer is placed in the bulk silicon layer instead of BOX layer (Suresh Gundapaneni et al., 2012). In the previous device band to band tunneling occur between channel and the drain region. This was due to high doping concentration, which makes the bands to overlap with each other and hence the valence band of channel overlaps with the conduction band of the drain. This makes a considerable increase in the off state current flow between source and drain (J. Chen et al., 1991).

![Bulk planar junction-less transistor](image)

Figure 2.2. Bulk planar junction-less transistor

A slight variation in the junction-less transistor is proposed in which dielectric separation is replaced by a p-type separation thus forming a PN junction in the vertical axis. This results in channel isolation at both sides, isolation due to work function difference in the top and PN junction in the bottom reduces the sub threshold leakage current to a considerable amount junction-less n-channel transistors, respectively.

The BPJLT produce good $I_{on}/I_{off}$ ratio than SOI JLT. It ensures superior enhanced electrostatic behavior such as high $I_{on}/I_{off}$, low DIBL and sub threshold slope than SOIJLT. Thus it can be used for further scaling. Thus leakage current in this structure is much more reduced and its performance is
improved. The junction-less transistor so far investigated is SOI device thus scaling beyond a limit is technologically challenging and expensive. Moreover the work function requirement is very high ie 5.5 ev for highly scaled n-channel device. The control of the gate in this structure is less as only one gate is available. Thus the symmetrical Double Gate Junctionless Transistor (DGJLT) is proposed.

2.3.3. Symmetrical Double Gate Junction-less Transistor

The symmetrical double gate junction-less transistor shown in Figure 2.3. has got a very simplified structure with a silicon layer of thickness \( t_{si} \) which is doped uniformly with the same type of dopant either n type or p type throughout the layer from source to drain. This has two gates in the top and bottom with gate dielectric in symmetric structure. Many works has been published in this type of structure (J. P. Duarte et al., 2011). The basic structural dimension is given by (Chi-Woo Lee et al., 2009) which compare the conventional inversion mode device and the junction-less device

![Figure 2.3. Cross sectional view of DGJLT.](image)

DGJLT structure with the above dimensions produces better short channel properties than the conventional inversion mode devices. In junction less transistor the \( L_{gate}=L_{eff} \) as there is no junction. JLTs produces identical transfer characteristics compared to that of the conventional MOSFET. The leakage current from drain to source is almost below the detection limit and
also the $I_{on}/I_{off}$ ratio is better for DGJLTs. Behavior of transistor in sub threshold realm seems important to obtain better $I_{on}/I_{off}$ ratio and switching behavior.

Table 2.1. Parameters of the conventional MOSFET and JLTFET

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional</th>
<th>Junction-less</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel doping</td>
<td>$2 \times 10^{15}$ cm$^{-3}$ (p-type)</td>
<td>$8 \times 10^{19}$ cm$^{-3}$ (N-type)</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>2 nm</td>
<td>2 nm</td>
</tr>
<tr>
<td>Gate work function</td>
<td>4.6 ev</td>
<td>5.5 ev</td>
</tr>
<tr>
<td>$t_{si}$</td>
<td>5 nm</td>
<td>5 nm</td>
</tr>
<tr>
<td>$W$</td>
<td>5 nm (Fin Width)</td>
<td>5 nm (Fin Width)</td>
</tr>
<tr>
<td>$L$</td>
<td>5-30 nm</td>
<td>10-30 nm</td>
</tr>
</tbody>
</table>

The junction-less transistor produces almost ideal sub threshold slope for short channel junction-less transistor ($L=5$ nm) of about 80 mv/decade which shows the potential of junction-less transistor for short channel application. If the channel doping concentration is increased the cross sectional need will decrease and drive current increases. The scaling of the device will elevate the short channel effects, thus enhancement in gate is required which gives good gate control over the channel. Hence triple gate structure is proposed.

2.3.4. **Triple Gate Junction-less transistor**

The Schematic 3D view and longitudinal view of junctionless triple metal gate transistor is shown in Figure 2.4 (a) and (b). This is a tri gate structure in which three sides of the device layer is covered by the gate dielectric and gate electrode and one side by the BOX layer. This is also an SOI structure as the device layer is mounted in the dielectric layer. It is an attractive device in terms of short channel effects as the DIBL and sub threshold slope is much reduced in this device. Different works publishes the
different voltage and current characteristics of the device (Renan Doria Trevisoli et al., 2012).

Figure 2.4. (a) Schematic 3-D view (b) longitudinal section of a triple-gate n-type JLT.

2.3.5. Quadruple Gate Junction-less Transistor

This is a quadruple gate structure shown in Figure 2.5 of junction-less transistor in which four sides of the device layer is covered by gate (Linfeng He et al., 2014). This structure provides a good control of the gate over the channel. As the number of the gate increases the short channel effects
decrease. (Linfeng He et al., 2014) studies the corner effect and the potential distribution problems of a quadruple gate junction-less MOSFET here the gate control is better compared to the DGJLT FET.

![Figure 2.5. Quadruple gate junction-less Transistor](image)

In conventional quadruple gate MOSFET the leakage current exists at the corner due to surface conduction where in JLTs the corner effects aren’t considered due to bulk conduction mechanism unlike, surface conduction. This type of gate behave similar to DGFET but the corner effects are ignored here.

### 2.3.6. Cylindrical Gate Junction-less Transistor

The cylindrical gate junctionless transistor is shown in the Figure 2.6. This structure is cylindrical gate all around junction-less transistor. The modeling of this device is associated by employing cylindrical coordinates. In the inversion mode device the cylindrical structure plays a major role. To improve the performance of the device and to be used for RF application gate engineering is employed in this structure and we could see an improvement compared to the normal device in transconductance, gain etc.
The surround gate MOSFET (Sung-Jin Choi et al., 2011; Shinji Migita et al., 2014) is one of the solutions for controlling the scaling limitations and increasing the device performance. In the surround gate structure, the source, drain and gate are arranged vertically and the sidewalls of the pillar are used as the channel region (Pujarini Ghosh et al., 2012). The surround gate structure produces good gate control, but on scaling of the device the drain current decreases and hence an alternative has to be made to improve the performance of the device. Gate engineering is a technique which improves the ON state current and decreases the short channel effects of the device. This technique proves to be good in the conventional inversion mode device (Pujarini Ghosh et al., 2012). This same technique has been incorporated in the cylindrical junctionless transistor and its performance is analyzed.

### 2.3.7. Double metal surround gate Junctionless Transistor

Dual Metal Surround Gate Junctionless Transistor (DMSGJLT) design effectively suppresses short channel effects and leads to a simultaneous increase in transconductance and drain current (Pujarini Ghosh et al.,). The 3D and correctional view of DMSGJLT is shown in the Figure 2.7(a) and (b).
This is a cylindrical structure with two different metal gates where metal M$_1$ is of workfunction 5.2 eV and the metal M$_2$ is made of workfunction 4.33 eV. The length of the first metal L$_1$ is 20 nm and the length of second metal L$_2$ is 20 nm. The center rod is a cylindrical silicon rod with a doping of about 1x10$^{19}$ cm$^{-3}$, uniform throughout the device layer. This is the device active region where the device operation takes place. The cross sectional view of the device is shown in Figure 2.7(b).

Work function of the metal gate for two regions is chosen such that the work function of the first metal should be higher than the work function of the second metal (Angsuman Sarkar et al., 2012). Electrostatic potential and workfunction are inversely related so decrease in workfunction increases the electrostatic potential and due to this a step increase is obtained in DMSGJLT. The step increase in the surface potential for dual metal structure given in
(Angsuman Sarkar et al., 2012; Pujarini Ghosh et al., 2012). This will increase the carrier transport efficiency and drain current. The leakage will be a major factor that has to be taken into account in a short channel device. The choice of proper high-k gate dielectrics will be the best solution for off state leakage current. This will be discussed in the following section.

2.4 Alternate Gate Oxide Material

The advancement in digital technology is seen vastly by the dimensions in the transistors which are reduced to twice the number for every 18 months (Moore 1965; Huff et al., 2003). The 2010 ITRS (International Technology Roadmap for Semiconductor) update clearly explains that we are progressing towards high-k dielectric materials which will make SiO$_2$ vanish in the MOSFET. In the device modeling, dielectric has emerged as one of the most difficult challenges for future device as per the ITRS (2003 Edition). An attempt to find the alternative dielectric material for MOSFET is made here. The conventional gate dielectric SiO$_2$ cannot survive the challenge of an EOT (Effective Oxide Thickness) = 1 nm. Also, as projected by the ITRS, no manufacturable solution has yet been found to fabricate the SiO$_2$ thickness. So it is highly preferable that materials with lesser physical thicknesses and high dielectric constants will be used for MOSFET devices (Hasanur et al., 2008). The equivalent oxide thickness (EOT) is a figure of merit to judge a gate oxide and is defined as in (2.1), where $d_{\text{high-k}}$ is the thickness of high-k dielectrics, $k_{\text{SiO}_2}$ and $k_{\text{high-k}}$ is the dielectric constant of SiO$_2$ and high-k dielectrics.

\[
EOT = \left( \frac{k_{\text{SiO}_2}}{k_{\text{high-k}}} \right) d_{\text{high-k}} \quad (\text{Hubbard et al., 1996}) \quad (2.1)
\]

According to Equation (2.1), if a dielectric material with a higher dielectric constant material can replace SiO$_2$ ($k = 3.9$), retaining the same capacitance $C_{\text{ox}}$, the dielectric layer thickness can be increased proportionally.
With scaling of the gate length downward, the gate dielectric must also be reduced by increasing the speed and density. However, this has reached to a fundamental limitation because with the SiO$_2$ dielectric layer for MOSFETs, gate dielectric thickness in the range of tunnelling has been reached. Consequently, with much larger thickness, scaling is allowed in the gate dielectrics with higher dielectric constants, this has become an active research area. The main cause for the replacement of higher dielectric constants for SiO$_2$ is the undesirable increase in gate leakage current with decreasing thickness (Y. I. Alivov et al., 2008). Electrical properties for some dielectric materials is summarized in Table 2.1 (J. Ajayan et al., 2015).

High-k gate dielectric materials such as hafnium dioxide (HfO$_2$), zirconium dioxide (ZrO$_2$), and titanium dioxide (TiO$_2$) have a dielectric constant or k above 3.9. For successful demonstration of high performance logic transistors on high-mobility non-silicon substrates with high I$_{ON}$/I$_{OFF}$ ratios, High-k gate dielectric is required. A high-k dielectric has a low drain leakage current, high $V_T$, high transit frequency, low channel resistance and high gate capacitance.

Keeping the capacitance same, the EOT shows the effective oxide thickness of the high-k dielectric material layer to SiO$_2$. The tunnelling current can be drastically reduced since a thicker layer is used. However, many requirements have to be met before a new high-k material can be integrated into the present ULSI (Ultra large scale integration) process flow, (Hori 1997; ITRS 2010). The electrical properties of SiO$_2$ and the outstanding material is one of the most crucial elements that allow successful scaling (Hori et al., 1997; Huff et al., 2003). First, it can be grown thermally on Si with uniformity and excellent control of thickness. It forms a very stable interface with a low defect density on the Si substrate. Up to 1000°C, SiO$_2$ is thermally very stable which is essential for the MOSFET fabrication. The band gap of SiO$_2$
approximately +9 eV which is large, with sufficiently large conduction and valence band offsets. The dielectric breakdown field of SiO₂ is ~ 13 MV/cm. In addition, SiO₂ facilitates photolithography because of its water insoluble properties. In the self-aligned CMOS technology, the use of a polysilicon (Poly-Si) gate electrode was also a determining factor in the scaling. However, as technology evolves, the properties such as high OFF current and reliability concerns, SiO₂ will soon reach its physical limitation (ITRS2010). The scaling down of the MOSFET device continuously with the minimum feature size of 90 nm and below would require EOT (equivalent oxide thickness) of less than 15 Å which corresponds to around 3 or 4 mono layers of SiO₂. In this thinner EOT range, SiO₂ is very difficult for low power applications as it mostly suffers from high OFF current (MarioLanza et al., 2011). So the next alternative high-k dielectric material for future CMOS technology is proposed.

2.4.1 Aluminium Oxide (Al₂O₃)

Due to its special physical and chemical properties, Aluminium oxide (Al₂O₃) has the potential to be used for future generation devices. Al₂O₃ has a large band gap of about 8.8 eV, a dielectric value of ~8, elevated Aluminium crystallization temperature (Xeng Yang et al., 2010), thermal stability as well as high-barrier offset. Because of its high crystallisation temperature, Al₂O₃ is also an alternative for conventional gate dielectric material. So it is compatible with conventional process of integrating complementary MOS devices, it involves high temperatures above 1000°C. At temperatures as high as 900°C, thermal degradation is not observed for ultrahigh vacuum (UHV) annealing. Al₂O₃ shows gate leakage much lower than that of the normal SiO₂ of effective oxide capacitance which furthermore gives great interface quality (Bouazra et al., 2008). The disadvantage of Al₂O₃ is that it has bad water leakage consistency contrasted with Zirconium-di-oxide (Berthelot et al., 2006).
2.4.1 Titanium-Di-Oxide (TiO$_2$)

TiO$_2$ is considered as the alternate gate dielectric for SiO$_2$. Despite the fact that the electronic band gap of this material is generally small (3.5 eV), its dielectric constant can vary from 40 to 110. Depending on the development procedure, TiO$_2$ presents two critical stages, Anatase and Retile. The last stage is the thermally 12 stable period that displays the higher dielectric constant, more or less 80. Anatase is a thermally flimsy stage with low dielectric constant transforming in Retile phase at temperatures In 600°c's (Albertin et al., 2007). TiO$_2$ has bad thermo dynamical stability with silicon and large band gap though TiO$_2$ has a very high dielectric constant. So it is not preferred in devices (Hubbard et al., 1997).

2.4.2 Hafnium-Di-Oxide (HfO$_2$)

HfO$_2$ can be viewed as the most promising dielectric oxide material to replace SiO$_2$ gate dielectric, because it is thermodynamically more stable on Si compared to other high-k materials. HfO$_2$ devices have exhibited many orders of decreased magnitude in gate leakage with an EOT of around 1.0 nm for cutting edge transistors. Due to the higher value of dielectric constant (k) and less debasement of HfO$_2$ dielectric material, which demonstrate a better properties.

The OFF current and the DIBL are found to decrease exponentially with increase in gate dielectrics which implies that the device has superior short channel effect suppression capability with high-k dielectrics. The lateral electric field also increases with increase in gate dielectric value (Shruti .K et al., 2011). Here in DMSGJLT we have replaced the gate dielectric SiO$_2$ with high k dielectric such as Si$_3$N$_4$, Al$_2$O$_3$, Y$_2$O$_3$, HfO$_2$ and TiO$_2$ and the parameters such as OFF current, I$_{ON}$/I$_{OFF}$ ratio and DIBL is taken. It is found that OFF current shows a considerable decrease for high k dielectric such as HfO$_2$ than SiO$_2$. Thus the high k dielectric such as HfO$_2$ shows a good leakage performance.
2.5 Conclusion

Different structures of junction-less transistors are analyzed. The complexity of fabrication is much reduced as the device employs no concentration gradient and type of doping throughout the device. Among the above structures, cylindrical structure with dual metal gate engineering is the most promising structure for Device scaling in terms of short channel effects, DIBL, sub threshold slope. It gives an improved current and voltage characteristics than the other devices. Thus this structure can be used for further scaling in the nano scale range. The leakage current decreases much with HfO$_2$ than SiO$_2$. HfO$_2$ is found from the analysis that it is the appropriate alternative for SiO$_2$ as it has appropriate band gap of about 6 eV whereas TiO$_2$ has a band gap of 3.5 eV which will improve the leakage parameters. The HfO$_2$ gate dielectric material is studied in detail by synthesizing and characterizing it in the following unit.