CHAPTER 5

A NEW SPACE VECTOR TECHNIQUE FOR THE DIRECT
THREE-LEVEL MATRIX CONVERTER

5.1 INTRODUCTION

The voltage stresses on the power devices can be reduced by using multi-level inverters (MLIs) (Celanovic and Boroyevich 2000, Lopez et al 2008 and Aneesh et al 2009). MLIs permit the use of lower rating power supplies and power devices for achieving higher output power rating. Using the same idea in the matrix converters, a new family of converters called multilevel matrix converters evolved with different concepts: i) Replacing each bidirectional switch in the CMC with n cells, each cell consisting of a capacitor connected to the centre of the H Bridge (Erickson and Al-Naseem 2001 and Erickson et al 2006). This topology generates multi-level output but at the cost of a more complicated circuit configuration and modulation strategy. ii) Modifying the topology of the IMC with additional switches, which makes available two different voltages levels at the output, i.e., the phase and the line voltages (Meng Yeong Lee et al 2010). This topology is effective for two-level and three-level voltage conversion with less complicated circuit configuration and modulation strategy as compared to (i).

Modified IMC based three-level converter uses the diode clamped multi-level space vector technique (Meng Yeong Lee et al 2010) on the inverter side and the conventional space vector technique on the rectifier side. In this chapter, a new class of direct three-level matrix converter (DTMC) along with its modulation techniques is developed and its performance is analyzed.
5.2 PROBLEM FORMULATION

The objective of this chapter is to develop a new DTMC topology namely, the direct three-level matrix converter, which requires three bidirectional switches of lower ratings (phase voltage rated) and the CMC topology. The structure is a $4 \times 3$ matrix converter that facilitates the increase in the output voltage levels by making the source neutral available to the load terminals. In addition to the multilevel operation, the converter also has the ability to control bi-directional power flow. The proposed DTMC is evaluated by simulation and hardware experimentation. The modulation strategy of the DTMC uses the multi-level space vector modulation technique along with the proposed neutral current balancing strategy. The same is implemented using the Xilinx based system generator facility, which is available as a toolbox in MATLAB R2010a, along with an FPGA.

5.3 PROPOSED TOPOLOGY

A DTMC in its very generic form, shown in Figure 5.1, consists of three arms that are connected to the source and one arm connected to the star point (neutral) of the input filter capacitances. Figure 5.1 depicts the general configuration of the proposed DTMC structure which consists of a CMC and a neutral point connector.

5.3.1 Indirect Matrix Converter Representation for the DTMC

The proposed DTMC topology consists of an array of $4 \times 3$ bidirectional switches, which includes the $3 \times 3$ switches of the CMC and three additional switches for making the neutral point of the input filter capacitance to be available at the load terminals. Equations (5.1) and (5.2) give the output voltages and the input currents of the DTMC.
Figure 5.1 Topology of the direct three-level matrix converter

\[ \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} & S_{Na} \\ S_{Ab} & S_{Bb} & S_{Cb} & S_{Nb} \\ S_{Ac} & S_{Bc} & S_{Cc} & S_{Nc} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \\ 0 \end{bmatrix} \]  
(5.1)

\[ \begin{bmatrix} I_A \\ I_B \\ I_C \\ I_N \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \\ S_{Na} & S_{Nb} & S_{Nc} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \]  
(5.2)

Since the DTMC is supplied by a voltage source, the input phases must never be shorted, and due to the inductive nature of the load, the output phases must never be left open. These constraints are realized by Equation (5.3).

\[ S_{Aj} + S_{Bj} + S_{Cj} + S_{Nj} = 1 \quad j \in \{a, b, c\} \]  
(5.3)
The DTMC can be decoupled into an indirect three-level matrix converter (ITMC) consisting of a fictitious two-level converter (FTC – input converter) and a fictitious inverter (FI - output converter), as shown in Figure 5.2.

![Figure 5.2 Topology of the indirect three-level matrix converter](image)

**Figure 5.2 Topology of the indirect three-level matrix converter**

The FTC consists of three phase arms and one neutral arm. Switching ON any of the two phase arms leads to the line voltage being available at the FDCB and switching ON any one phase arm with the neutral arm leads to the phase voltage being available at the FDCB. This results in twelve active voltage vectors on the rectifier side. This decoupled representation simplifies the control of the input current and the output voltage in DTMC, as described in the next section.
5.4 SPACE VECTOR MODULATION TECHNIQUE FOR THE DTMC

The switching function for the DTMC is represented as the product of the rectifier switching function and the inverter switching function and is given by Equation (5.4).

\[
\begin{bmatrix}
S_{Aa} & S_{Ba} & S_{Ca} & S_{Na} \\
S_{Ab} & S_{Bb} & S_{Cb} & S_{Nb} \\
S_{Ac} & S_{Bc} & S_{Cc} & S_{Nc}
\end{bmatrix}
= \begin{bmatrix}
S_{IA} & S_{Ia} \\
S_{IB} & S_{Ib} \\
S_{IC} & S_{Ic}
\end{bmatrix}
\times \begin{bmatrix}
S_{CA} & S_{CB} & S_{CC} & S_{CN}
\end{bmatrix}
\] (5.4)

The switching states for synthesizing the required currents and voltages are described in the following subsections.

5.4.1 The Fictitious Two-Level Converter Stage

Assuming that the output of the FTC is a constant current source $I_{DC}$, the space vector for all valid switching states are determined by Equations (5.5) to (5.7).

\[
\begin{align*}
I_\alpha &= I_A + I_B \cos \frac{2\pi}{3} + I_C \cos \frac{4\pi}{3} \\
I_\beta &= I_B \sin \frac{2\pi}{3} + I_C \sin \frac{4\pi}{3} \\
I_0 &= I_A + I_B + I_C
\end{align*}
\] (5.5) (5.6) (5.7)

As described in Section 5.3.1, switching ON the neutral arm causes the current to flow in the source neutral resulting in the space vector having a component along the $I_0$ axis. Table 5.1 gives the space vector components for different valid switching states and Figure 5.3(a) shows the space vectors distribution.
Table 5.1 Space vectors for the fictitious two-level converter

<table>
<thead>
<tr>
<th>Type</th>
<th>Vector</th>
<th>[SCA SCB SCC SCN]</th>
<th>I_A</th>
<th>I_B</th>
<th>I_C</th>
<th>I_N=I_0</th>
<th>I_in</th>
<th>∠i_in</th>
<th>V_DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active long vectors</td>
<td>I_{L1}[AB]</td>
<td>[1000 0000]</td>
<td>+I_{DC}</td>
<td>-I_{DC}</td>
<td>0</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>330°</td>
<td>V_{AB}</td>
</tr>
<tr>
<td></td>
<td>I_{L2}[AC]</td>
<td>[1000 0001]</td>
<td>+I_{DC}</td>
<td>0</td>
<td>-I_{DC}</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>30°</td>
<td>V_{AC}</td>
</tr>
<tr>
<td></td>
<td>I_{L3}[BC]</td>
<td>[0010 0000]</td>
<td>0</td>
<td>+I_{DC}</td>
<td>-I_{DC}</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>90°</td>
<td>V_{BC}</td>
</tr>
<tr>
<td></td>
<td>I_{L4}[BA]</td>
<td>[0010 0001]</td>
<td>-I_{DC}</td>
<td>+I_{DC}</td>
<td>0</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>150°</td>
<td>V_{BA}</td>
</tr>
<tr>
<td></td>
<td>I_{L5}[CA]</td>
<td>[0010 0100]</td>
<td>-I_{DC}</td>
<td>0</td>
<td>+I_{DC}</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>210°</td>
<td>V_{CA}</td>
</tr>
<tr>
<td></td>
<td>I_{L6}[CB]</td>
<td>[0010 0101]</td>
<td>0</td>
<td>-I_{DC}</td>
<td>+I_{DC}</td>
<td>0</td>
<td>√3I_{DC}</td>
<td>270°</td>
<td>V_{CB}</td>
</tr>
<tr>
<td>Active short vectors</td>
<td>I_{P1}[AN]</td>
<td>[1000 0001]</td>
<td>+I_{DC}</td>
<td>0</td>
<td>0</td>
<td>-I_{DC}</td>
<td>I_{DC}</td>
<td>0°</td>
<td>V_{AN}</td>
</tr>
<tr>
<td></td>
<td>I_{P2}[NC]</td>
<td>[0001 0010]</td>
<td>0</td>
<td>0</td>
<td>-I_{DC}</td>
<td>+I_{DC}</td>
<td>I_{DC}</td>
<td>60°</td>
<td>V_{NC}</td>
</tr>
<tr>
<td></td>
<td>I_{P3}[BN]</td>
<td>[0100 0001]</td>
<td>0</td>
<td>+I_{DC}</td>
<td>0</td>
<td>-I_{DC}</td>
<td>I_{DC}</td>
<td>120°</td>
<td>V_{BN}</td>
</tr>
<tr>
<td></td>
<td>I_{P4}[NA]</td>
<td>[0001 0100]</td>
<td>-I_{DC}</td>
<td>0</td>
<td>0</td>
<td>+I_{DC}</td>
<td>I_{DC}</td>
<td>180°</td>
<td>V_{NA}</td>
</tr>
<tr>
<td></td>
<td>I_{P5}[CN]</td>
<td>[0010 0001]</td>
<td>0</td>
<td>0</td>
<td>+I_{DC}</td>
<td>-I_{DC}</td>
<td>I_{DC}</td>
<td>240°</td>
<td>V_{CN}</td>
</tr>
<tr>
<td></td>
<td>I_{P6}[NB]</td>
<td>[0001 0100]</td>
<td>0</td>
<td>-I_{DC}</td>
<td>0</td>
<td>+I_{DC}</td>
<td>I_{DC}</td>
<td>300°</td>
<td>V_{NB}</td>
</tr>
<tr>
<td>Zero vectors</td>
<td>I_Z</td>
<td>[1 0 0 0; 1 0 0 0; 0 0 1 0; 0 0 1 0]</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

where, \( I_{in} = \sqrt{I_{i\alpha}^2 + I_{i\beta}^2} \) and \( \angle i_{in} = \tan^{-1} \frac{I_{i\beta}}{I_{i\alpha}} \).

Vectors represented by \( I_{Li} \) (active long vectors) are conventional rectifier space vectors, which do not contribute to the neutral current. Vectors represented by \( I_{Pi} \) (active short vectors) contribute to the neutral current. To ensure that the input current is sinusoidal, the reference space vector must lie on the \( \alpha\beta \) plane requiring the neutral current to be zero on application of the vector \( I_{Pi} \). This is carried out by applying equally the adjacent \( I_{Pi} \) vectors,
which lie on the upper and the lower halves of the $\alpha\beta$ plane. This ensures that the average neutral current is zero over a switching period. The example in Table 5.2 explains the same.

**Table 5.2 Neutral current balancing and virtual vector synthesis**

<table>
<thead>
<tr>
<th>Switching time</th>
<th>Applied vectors</th>
<th>$I_A$</th>
<th>$I_B$</th>
<th>$I_C$</th>
<th>$I_N$</th>
<th>$V_{DC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_s/2$</td>
<td>$I_{P6}$</td>
<td>0</td>
<td>-$I_{DC}$</td>
<td>0</td>
<td>+$I_{DC}$</td>
<td>$V_{NB}$</td>
</tr>
<tr>
<td>$T_s/2$</td>
<td>$I_{P1}$</td>
<td>+$I_{DC}$</td>
<td>0</td>
<td>0</td>
<td>-$I_{DC}$</td>
<td>$V_{AN}$</td>
</tr>
<tr>
<td>$T_s$</td>
<td>$I_{VP1}=\frac{1}{2}I_{P6}+\frac{1}{2}I_{P1}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>$-\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>0</td>
<td>$\frac{1}{2}V_{AB}$</td>
</tr>
</tbody>
</table>

This solution to the neutral current balancing problem (Celanovic and Boroyevich 2000) introduces virtual vectors $I_{VPi}$, which lie completely on the $\alpha\beta$ plane, as given in Table 5.3 and shown in Figure 5.3(b).

![Figure 5.3(a) Space vectors of the FTC](image-url)
Figure 5.3(b) Space vectors and virtual vectors of the FTC

Table 5.3  Virtual current space vectors

<table>
<thead>
<tr>
<th>Virtual vectors</th>
<th>Sharing vectors</th>
<th>$I_A$</th>
<th>$I_B$</th>
<th>$I_C$</th>
<th>$I_N$ = $I_0$</th>
<th>$\angle I_{in}$</th>
<th>$V_{DC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VP1}$[AN]</td>
<td>$I_{P6}$,$I_{P1}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>330°</td>
</tr>
<tr>
<td>$I_{VP2}$[NC]</td>
<td>$I_{P1}$,$I_{P2}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>30°</td>
</tr>
<tr>
<td>$I_{VP3}$[BN]</td>
<td>$I_{P2}$,$I_{P3}$</td>
<td>0</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>90°</td>
</tr>
<tr>
<td>$I_{VP4}$[NA]</td>
<td>$I_{P3}$,$I_{P4}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>150°</td>
</tr>
<tr>
<td>$I_{VP5}$[CN]</td>
<td>$I_{P4}$,$I_{P5}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>210°</td>
</tr>
<tr>
<td>$I_{VP6}$[NB]</td>
<td>$I_{P5}$,$I_{P6}$</td>
<td>0</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>$\frac{1}{2}I_{DC}$</td>
<td>0</td>
<td>$\frac{\sqrt{3}}{2}I_{DC}$</td>
<td>270°</td>
</tr>
</tbody>
</table>
Figure 5.4(a) shows the sector zero of the space vector diagram of the FTC. Each sector consists of two active long vectors, two active virtual short vectors and four zero vectors. To synthesize the required reference input current and the FDCB voltage, the three nearest current vectors (Busquets-Monge et al 2004) are selected, as shown in Figure 5.4(b), depending on the modulation index $m_c$ of the FTC.

Figure 5.4(a) Sector region identification of the FTC

Figure 5.4(b) Region vector identification of the FTC

In order to identify the region in which the reference vector lies, equations of the three lines are derived and shown in Figure 5.5. Table 5.4 gives the rules for identifying the region in which the reference vector lies in the FTC for different values of modulation indices $m_c$. 
Duty cycles of the selected vectors for different regions are computed using Equation (5.8), where \((x_i, y_i)\) are the coordinates of the selected vector \(I_i\) and \(d_i\) is its duty cycle. \(X\) and \(Y\) are the coordinates of the reference vector \(I_{REF}\) and are given by Equation (5.9).
\[
\begin{bmatrix}
  x_1 & x_2 & x_3 \\
  y_1 & y_2 & y_3 \\
  1 & 1 & 1
\end{bmatrix}
\begin{bmatrix}
  d_1 \\
  d_2 \\
  d_3
\end{bmatrix}
= \begin{bmatrix}
  X \\
  Y
\end{bmatrix} \quad (5.8)
\]

\[X = m_c \cos \theta_c \quad \& \quad Y = m_c \sin \theta_c \quad (5.9)\]

While computing the duty cycle, the sector in Figure 5.6(a) is rotated as shown in Figure 5.6 (b). The coordinates are chosen according to the region in which the reference vector lies, as shown in Figure 5.6 (b). Table 5.5 gives the duty cycles derived for different regions

**Figure 5.6 (a) Sector 1 and (b) sector 1 rotated**

**Table 5.5 Duty cycles for different regions in a given sector**

<table>
<thead>
<tr>
<th>Region</th>
<th>( \mathbf{d}_1 - \mathbf{I}_1 )</th>
<th>( \mathbf{d}_2 - \mathbf{I}_2 )</th>
<th>( \mathbf{d}_3 - \mathbf{I}_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 )</td>
<td>( \frac{2}{\sqrt{3}} m_c \sin(\theta_c) )</td>
<td>( 2 m_c \cos(\theta_c) - 1 )</td>
<td>( 2 - \frac{4}{\sqrt{3}} m_c \sin(60^\circ + \theta_c) )</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>( 2 m_c \sin(30^\circ + \theta_c) - 1 )</td>
<td>( \frac{2}{\sqrt{3}} m_c \sin(60^\circ - \theta_c) )</td>
<td>( 2 - \frac{4}{\sqrt{3}} m_c \sin(60^\circ + \theta_c) )</td>
</tr>
<tr>
<td>( R_3 )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin(60^\circ + \theta_c) - 1 )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin(60^\circ - \theta_c) )</td>
<td>( 2 - 4 m_c \cos(\theta_c) )</td>
</tr>
<tr>
<td>( R_4 )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin(60^\circ + \theta_c) - 1 )</td>
<td>( 2 - 4 m_c \sin(30^\circ - \theta_c) )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin \theta_c )</td>
</tr>
<tr>
<td>( R_5 )</td>
<td>( 1 - \frac{4}{\sqrt{3}} m_c \sin(60^\circ + \theta_c) )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin(60^\circ - \theta_c) )</td>
<td>( \frac{4}{\sqrt{3}} m_c \sin \theta_c )</td>
</tr>
</tbody>
</table>
where, $\theta_c$ is the angle of $I_{REF}$ within the sector and $m_c$ is the inverter zero compensated converter modulation index discussed later and is given in Equation (5.14).

### 5.4.2 The Fictitious Inverter Stage

The conventional SVPWM is implemented in the inverter stage. This consists of six active voltage vectors and two zero voltage vectors, as shown in Figure 5.7. To generate the required reference vector $V_{OUT}$, adjacent active vectors $V_\gamma$, $V_\delta$ and a zero vector $V_0$ are selected whose duty cycles $d_\gamma$, $d_\delta$ and $d_0$ are given by Equation (5.10)

$$d_\gamma = \sin \left(60^\circ - \theta_v\right) \quad d_\delta = \sin(\theta_v) \quad \text{and} \quad d_0 = 1 - (d_\gamma + d_\delta) \quad (5.10)$$

where, $\theta_v$ is the angle of $V_{OUT}$ within a sector. The output voltage of the inverter can be adjusted by any one of the two schemes: (i) changing the FDCB voltage to the inverter, (ii) changing the modulation index $m_v$ of the inverter. The second scheme is not used for reasons explained in the next paragraph and hence $m_v=1$. The FDCB voltage can be varied by changing the modulation index $m_c$ of FTC as given in Equation (5.11)

![Figure 5.7](attachment:image.png) (a) Space vectors of the FI and (b) sector and duty cycle allocation
where, \( m_{\text{DTMC}} \) is the required modulation index of the DTMC. At higher modulation indices, the FTC reference vector, \( I_m \), lies in any one of the regions \( R_1, R_2, R_3 \) or \( R_4 \). These regions do not use any zero vectors for the modulation, as described in section 5.4.1. Simultaneous use of the zero vectors at the inverter stage would cause the output voltage to become zero. This is not consistent with the idea of multilevel switching techniques as it increases the THD at the output. To decrease the THD of the DTMC, zero vectors are not used at the inverter stage, which does not allow for the change in modulation index \( m_c \). With the elimination of the zero vectors, the duty cycles for active vectors are recomputed as given in Equation (5.12). This increases the output voltage vector as given by Equation (5.13). Thus the reference vector is brought outside the inscribed circle of the space vector hexagon leading to an over modulation condition.

\[
d_{\gamma}' = \frac{d_{\gamma}}{d_{\gamma} + d_\delta} \quad \text{and} \quad d_{\delta}' = \frac{d_\delta}{d_{\gamma} + d_\delta} \quad (5.12)
\]

\[
V_{\text{OUT}}' = d_{\gamma}' V_{\gamma} + d_\delta' V_\delta = \frac{V_{\text{OUT}}}{d_{\gamma} + d_\delta} \quad (5.13)
\]

The increase in the output voltage vector is compensated by adjusting the FDCB voltage by modifying the modulation index of the FTC dynamically, as given by Equation (5.14).

\[
m_c = \frac{\sqrt{3}}{2} m_{\text{DTMC}} (d_{\gamma} + d_\delta) \quad (5.14)
\]

Figure 5.8 shows the allocation of the switching vectors in a sampling period for a particular inverter sector and for different regions of the converter sector. The period of the virtual vector is divided into two, during which the adjacent upper and lower active short vectors of the corresponding
virtual vector is applied. The real-time switching pattern for the DTMC is computed for each vector combination of the FTC and the FI using Equation (5.4). Figure 5.8(a) shows the switching pattern for the DTMC for regions $R_1$ and $R_2$ when only one active virtual vector is used. Figure 5.8(b) shows the switching pattern for the DTMC for regions $R_3$, $R_4$ and $R_5$ when two active virtual vectors are used.

**Figure 5.8 (a) Switching pattern of the DTMC for the regions $R_1$ and $R_2$**

**Figure 5.8(b) Switching pattern of the DTMC for the regions $R_3$, $R_4$ and $R_5$**

### 5.5 DTMC OPERATION UNDER ABNORMAL INPUT CONDITIONS

From Equation (5.14) it can be shown that within a sector, $m_c$ reaches the peak once when $(d_v^e + d_v^o) = 1$ and reaches the minimum value twice when $(d_v^e = 0)$ or $(d_v^o = 0)$, and this repeats for all the six sectors. Hence the
dynamic variation of the \( m_c \) introduces a sixth harmonic component \( 6f_i \) at the FDCB, as shown in Figure 5.9 (a), where \( f_i \) is the fundamental frequency of the input voltage.

![Figure 5.9 (a) Calculated FDCV with a balanced input voltage](image)

It was shown in chapter 4 that an input unbalance introduces a second harmonic component \( 2f_i \) at the FDCB of the CMC. Hence, the FDCB voltage of DTMC, as shown in Figure 5.9(b), contains two components \( 6f_i \) & \( 2f_i \) during the input unbalance.

![Figure 5.9 (b) Calculated FDCB voltage with an unbalanced input voltage](image)

The instantaneous variation can be determined by Equation (5.15), where \( V_R, V_S \) and \( V_T \) are the FDCB voltage on applying the switching vectors \( I_1, I_2 \) and \( I_3 \) respectively.

\[
V_{DC} = d_1 \times |V_R| + d_2 \times |V_S| + d_3 \times |V_T|
\]  
(5.15)
To mitigate the effects of the unbalance at the output, as explained in chapter 4, the input voltage of the FI must be limited to the minimum of the FDCB voltage $V_{\text{DC}}$ over an input cycle expressed as $V_{\text{DC\_Min}}$. This is achieved by dynamically modifying $m_c$, as given in Equation (5.16). This mitigates the effect of unbalance and harmonics in the output currents while the input current harmonics are left uncompensated.

$$m_c = \frac{\sqrt{3}}{2} m_{\text{DTMC}} (d_\gamma + d_\delta) \times \frac{V_{\text{DC\_Min}}}{V_{\text{DCF}}}$$  \hspace{1cm} (5.16)

### 5.6 MODELING OF LOSSES IN THE CMC AND THE DTMC

There are three types of losses in power semiconductor devices namely the ON, the OFF and the switching losses. The power loss in the device when it is “OFF” is negligible compared to its power loss when it is either “ON” or when it is undergoing transition. The power loss in the device during its ‘ON’ state is called the conduction loss while the power losses in the device during its transition (‘ON’ to ‘OFF’ or vice-versa) states is called the switching loss. Conduction loss is the product of the voltage drop across the device and the current through the device, when it is in the ‘ON’ state. Switching loss is proportional to the product of blocking voltage and conduction current at the instant of switching; and if this is significant, it is termed as hard switching loss (Bierhoff and Fuchs 2004). If the switching occurs when either the current through the device or the voltage across the device is nearly zero, the commutation is referred to as ‘soft switching’ and the switching loss in the device is negligible. For an IGBT, there are two types of losses during hard switching: $T_{\text{on\_losses}}$ and $T_{\text{off\_losses}}$, associated with the device turn-ON and turn-OFF process respectively. For a diode, the switching loss is caused by reverse recovery mechanism that occurs only during the diode turn-OFF. Hence, the turn-ON loss for a diode is not considered.
5.6.1 Conduction Loss Modeling for the CMC and the DTMC

From Equation (5.3), it can be seen that in each phase only one switch conducts at any given time. Hence, there is always only one IGBT that conducts and only one diode that conducts at an output phase of the CMC and the DTMC. Equations (5.17) and (5.18) give the conduction loss and the conduction energy of one output phase in each switching cycle

$$C_{\text{Losses}}(v, i_L) = v_{\text{dIGBT}}(i_L) \times i_L + v_{\text{ddiode}}(i_L) \times i_L \quad (5.17)$$

$$E_{C}(v, i_L) = \int_0^{T_s} C_{\text{Losses}}(v, i_L) \, dt \quad (5.18)$$

where, $v_{\text{dIGBT}}(i_L)$ is the ON state voltage drop in the IGBT and $v_{\text{ddiode}}(i_L)$ is the ON state voltage drop in the diode and given by Equations (5.19) and (5.20)

$$v_{\text{dIGBT}}(i_L) = x + y \times i_L^z \quad (5.19)$$

$$v_{\text{ddiode}}(i_L) = m + n \times i_L^k \quad (5.20)$$

where, x, y, z, m, n and k are constants that are obtained from the curve fitting equation of $V_{ce}$-$I_c$ characteristics given in the datasheet of the device used. Then the average conduction loss over an interval T, for the CMC and the DTMC, is given by Equation (5.21).

$$C_{L_{\text{Avg}}} = \frac{1}{T} \int_0^T C_{\text{Losses}}(t) \, dt \quad (5.21)$$

5.6.2 Switching Loss Modeling for the CMC and the DTMC

During switching transients, the switching energy is described by Equation (5.22) (Wang and Venkataramanan 2006, Apap et al 2003)

$$E_{\text{sw}}(v_{\text{Block}}, i_L) = E_{\text{swR}} \times (v_{\text{Block}} \times i_L) / (V_{R} \times i_{R}) \quad (5.22)$$
where, $V_R$, $i_R$ and $E_{swR}$ are respectively the voltage, current and switching energy of the device at the rated $V_R$ and $i_R$. From Figure 1.4, and the four step commutation procedure, discussed in chapter 1, it can be seen that when commutation happens between the bidirectional switch $S_1$ to switch $S_2$ under the condition of $V_{in} > 0$ and $I_{out} > 0$, commutation losses do not occur for switches $S_1^-$, $S_2^+$ and $S_2^-$. This is because the switches $S_1^-$ and $S_2^-$ do not block any voltage and the switch $S_2^+$ does not conduct current. This creates only a turn OFF loss for the switch $S_1^+$. Similarly, $S_2$ to $S_1$ transition creates a turn ON loss for the switch $S_1^+$ and a turn OFF loss for the diode $D_2^-$. Table 5.6 summarizes the switching energy losses for commutation between $S_1$ and $S_2$ evaluated for all conditions of input voltages and output currents.

**Table 5.6  Switching energy losses for switch $S_1$ to switch $S_2$ transition**

<table>
<thead>
<tr>
<th>Switch transition</th>
<th>$S_1 \rightarrow S_2$</th>
<th>$S_2 \rightarrow S_1$</th>
<th>$S_1 \rightarrow S_2$</th>
<th>$S_2 \rightarrow S_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in} +$</td>
<td>$E_{off}$</td>
<td>$E_{on} + E_{rr,D}$</td>
<td>$E_{on} + E_{rr,D}$</td>
<td>$E_{off}$</td>
</tr>
<tr>
<td>$V_{in} -$</td>
<td>$E_{on} + E_{rr,D}$</td>
<td>$E_{off}$</td>
<td>$E_{off}$</td>
<td>$E_{on} + E_{rr,D}$</td>
</tr>
</tbody>
</table>

From Table 5.6, it can be generalized that two commutation events, i.e., (i) first phase to second phase transition and (ii) second phase to first phase transition within a switching cycle produces three switching losses namely (i) an IGBT ON loss, (ii) an IGBT OFF loss and (iii) a Diode OFF loss. Hence $E_{swR} = E_{on} + E_{off} + E_{rr,D}$ where, $E_{on}$ and $E_{off}$ are the switching energy for the IGBT ON and IGBT OFF switchings at the rated $V_R$ and $i_R$. $E_{rr,D}$ is the DIODE OFF switching energy at the rated $V_R$ and $i_R$. In general, for a particular transition from the input phase $x$ to the input phase $y$, and vice-versa the switching loss is given by Equation (5.23).
\[ E_{SW}(v_{xy}, i_L) = (E_{ON} + E_{off} + E_{rr.D}) \times (|v_{xy}| \times i_L) / (V_R \times i_R) \]

(5.23)

From the \( T_{\text{delay}} \)-I \(_c\) characteristics of the datasheet, \( T_{on}, T_{off} \) and \( T_r \) are identified. Equation (5.24) gives the switching power loss.

\[ S_{\text{Losses}}(v_{xy}, i_L) = \left( \frac{E_{on}}{T_{on}} + \frac{E_{off}}{T_{off}} + \frac{E_{rr.D}}{T_r} \right) \times (|v_{xy}| \times i_L) / (V_R \times i_R) \]

(5.24)

5.6.2.1 Switching energy calculation for the CMC

Switching losses depend on the modulation technique. In this work, a double-sided space vector switching technique is selected for the CMC as well as the DTMC. It can be seen that the optimized switching technique (Nielsen et al 1996) leads to eight commutation events over all the three output phases in a switching cycle \( T_s \). Four of these commutation events occur in an output phase and two commutation events each occur in the other two output phases.

![Figure 5.10 Commutation events of the CMC in a switching period for voltage sector 1 and current sector 1](image)

From Figure 5.10, it can be seen that the total switching energy of the CMC over a sampling time \( T_s \) is given by Equation (5.25)
\[ E_{sw} = K \cdot (|v_{AC}| \cdot i_a + |v_{BC}| \cdot i_b + (|v_{AB}| + |v_{AC}|) \cdot i_c) \] (5.25)

where, \( K = \frac{(E_{on} + E_{off} + E_{rr,D})}{(V_R \times i_R)} \). For other voltage and current sectors, Equation (5.25) can be generalized as Equation (5.26)

\[ E_{sw} = K \cdot (x i_a + y i_b + z i_c) \] (5.26)

where, \( x, y \) and \( z \) take any of the values \(|v_{AB}|, |v_{BC}|, |v_{AC}|, (|v_{AB}| + |v_{BC}|) \) or \((|v_{AB}| + |v_{AC}|)\) depending on the sectors of the current and the voltage.

### 5.6.2.2 Switching energy calculation for the DTMC

In the DTMC, two types of commutation events occur namely: i) the line commutation where the blocking voltage is the line voltage and ii) the phase commutation where the blocking voltage is the phase voltage. Extending the optimized indirect space vector switchings for the DTMC, as explained in Appendix II, the number of commutation events for a particular voltage sector \( X \) and different regions of current sector \( Y \) is calculated and given in Table 5.7. Equations (5.27) to (5.31) give the total switching energy of the DTMC over a sampling time \( T \) for the voltage sector 1 and different regions of the current sector 1.

<table>
<thead>
<tr>
<th>Commutation events</th>
<th>Converter sector - ( Y ) &amp; Inverter sector -( X )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Regions of converter sector</td>
</tr>
<tr>
<td>Line voltage commutation</td>
<td></td>
</tr>
<tr>
<td>Phase voltage commutation</td>
<td></td>
</tr>
</tbody>
</table>
Region 1

\[ E_{sw.R1} = K \cdot (|v_{AN}| \cdot i_a + (|v_{BC}| + |v_{CN}| + |v_{BN}|) \cdot i_b + (|v_{AB}| + |v_{AC}| + 2|v_{AN}| + |v_{BN}| + |v_{CN}|) \cdot i_c) \]  
\[ (5.27) \]

Region 2

\[ E_{sw.R2} = K \cdot (|v_{AN}| \cdot i_a + (|v_{BC}| + 2|v_{CN}|) \cdot i_b + (|v_{AB}| + |v_{AC}| + 2|v_{AN}| + 2|v_{CN}|) \cdot i_c) \]  
\[ (5.28) \]

Region 3

\[ E_{sw.R3} = K \cdot (3|v_{AN}| \cdot i_a + (|v_{BC}| + |v_{CN}| + |v_{BN}|) \cdot i_b + (|v_{AB}| + 3|v_{AN}| + |v_{BN}| + |v_{CN}|) \cdot i_c) \]  
\[ (5.29) \]

Region 4

\[ E_{sw.R4} = K \cdot (3|v_{AN}| \cdot i_a + (|v_{CN}| + |v_{BN}|) \cdot i_b + (|v_{AC}| + 3|v_{AN}| + |v_{BN}| + 2|v_{CN}|) \cdot i_c) \]  
\[ (5.30) \]

Region 5

\[ E_{sw.R5} = K \cdot (2|v_{AN}| \cdot i_a + (|v_{BN}| + 2|v_{CN}|) \cdot i_b + (|v_{BN}| + 2|v_{AN}| + 2|v_{CN}|) \cdot i_c) \]  
\[ (5.31) \]

The switching and conduction losses for the DTMC were derived and compared with those for the CMC. A complete loss model was developed using the Simulink blockset in MATLAB. Through simulations, switching energy losses for different regions for different sectors of the current and the voltage are calculated using the above procedure and results obtained are discussed and presented in the next section.
5.7 SIMULATION

To evaluate the performance of the proposed topology with the modified space vector technique, simulation with R–L load was performed. Table 5.8 gives the simulation parameters.

Table 5.8 Simulation parameters for the DTMC topology

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-L Load</td>
<td>R = 20Ω, L = 21mH</td>
</tr>
<tr>
<td>Input phase voltage</td>
<td>100 V</td>
</tr>
<tr>
<td>Input voltage frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Input filter</td>
<td>L = 2 mH, C = 35 µF, R$_d$ = 15 Ω</td>
</tr>
<tr>
<td>Output Voltage frequency</td>
<td>25 Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>6 kHz</td>
</tr>
<tr>
<td>Modulation Index</td>
<td>0.72, 0.5, 0.25</td>
</tr>
</tbody>
</table>

For modulation indices between $\frac{\sqrt{3}}{4}$ and $\frac{\sqrt{3}}{2}$, the output voltage switches between the active long vectors and the active short vectors but for lower modulation indices, the output voltage switches between the active short vectors and the zero vectors. Figure 5.11 shows the output phase voltages, output line voltages, input currents and output currents for the voltage transfer ratio that is changed from 0.72 to 0.5 at 0.4 s and 0.5 to 0.25 at 0.5 s. The harmonic content of the input and the output currents increase with decrease in the voltage transfer ratio. In the CMC, the peak of the output voltage is $\sqrt{3}$ times the input voltage for all values of modulation indices. However, in the DTMC, the peak of the output voltage is $\sqrt{3}$ times the input voltage for the modulation indices greater than $\frac{\sqrt{3}}{4}$ while the peak of the
output voltage is $\frac{\sqrt{3}}{2}$ times the input voltage for modulation indices lesser than $\frac{\sqrt{3}}{4}$. This leads to lower switching stress on the power devices in the case of the DTMC.

Figure 5.11 (Continued)
Figure 5.11 Performance of the DTMC with a balanced supply for different modulation indices (0.72, 0.5, 0.25) (a) output phase voltage, (b) output line voltage, (c) input phase current and (d) output phase current

A 20% unbalance in the phase B was introduced. In addition, second and third harmonics with magnitudes of 4% and 7% of the fundamental respectively were added to all the three phases as shown in Figure 5.12(a). By dynamically modifying the modulation index, as explained in the previous section, the effect of the unbalance and harmonics has been mitigated in the output voltages and currents, as shown in Figures. 5.12(b) and 5.12(d). The unbalanced input currents are shown in Figure 5.12(c).
Figure 5.12 Performance of the DTMC with an unbalanced supply
(a) output phase voltage, (b) output line voltage, (c) input
phase current and (d) output phase current and
(e) modulation index
Figures 5.13 to 5.15 present a quantitative comparison between the CMC and the DTMC. Simulation was carried out for the CMC and the DTMC for a Modulation Index (MI) of 0.866 and the THD of the output voltage are shown in Figures 5.13(a) and 5.13(b). At the maximum modulation index of 0.866, the THD for the DTMC reduces by 10% when compared to the CMC. The THD content of the output voltage for the CMC and the DTMC, for all modulation indices, is presented in Figure 5.13(c). It can be seen that the DTMC has a better (lower) THD than the CMC for all modulation indices. In the DTMC, for modulation indices varying from 0.866 to 0.45, the current vector lies in any of the regions of R₁, R₂, R₃, or R₄ and the THD is almost constant as zero vectors are not selected. When the current vector is in the region R₅ (MI < 0.4), the THD of the DTMC rises linearly with modulation index, as in the case of the CMC, because of the use of the zero vectors.

Figure 5.13 (Continued)
Figure 5.13 Output voltage THD for MI of 0.866 (a) CMC, (b) DTMC, (c) output voltage THD for the CMC and the DTMC with 6 kHz switching frequency for different MI

At very low modulation index, the THD for the DTMC reduces by approximately 58% as compared to the CMC due to the use of phase vectors. From Figure 5.14(a), it can be observed that the conduction losses are always greater than the switching losses in the CMC, for different values of MIs. Figure 5.14(b) shows that as the input power factor decreases, the output power of the converter also decreases.
Figure 5.14 (a) Losses vs. MI and (b) output vs. MI (different IPF)

The conduction losses for the DTMC and the CMC are the same under all operating conditions. However, the switching losses for the DTMC are higher than the switching losses of the CMC for all MIs, since the switching events are more in the DTMC than in the CMC. With a double side banded SVM, the DTMC exhibits higher switching losses for all values of MIs. Nevertheless, for the single sided SWM, the DTMC exhibits higher switching losses for lower values of MIs and lower switching losses for higher values of MIs. This is because the switching events of the regions $R_3$, $R_4$ and $R_5$ are very high compared to the switching events of the regions $R_1$ and $R_2$, as shown in Figure 5.15.
Figure 5.15 Conduction and switching losses for the DTMC and the CMC for different values of MI

5.6 HARDWARE IMPLEMENTATION

To validate the proposed switching algorithm, a 3 kVA direct multilevel matrix converter prototype was developed. The setup consists of a control circuit, CONCEPT gate driver module (6SD106EI), multilevel matrix converter module with bidirectional switches (SEMIKRON - SK60GM123). The control circuit consists of an FPGA (SPARTEN 3A DSP-XC3S1800A) for generating switching pulses for the DTMC.

The switching information and the current direction information were processed using the FPGA for generating the DTMC switching pulses along with the implementation of the four-step commutation. The system generator toolbox in the MATLAB was used to generate the FPGA code in VHDL for generating the firing pulses. The experiment was conducted with a balanced input phase voltage of 100V, switching frequency of 6 kHz, \( R_L = 20 \Omega \), \( L_L = 21 \text{mH} \) and \( MI = 0.72 \). The DTMC was used for converting the 50 Hz input voltage to 25 Hz output voltage. Figure 5.16 shows the laboratory prototype of
the DTMC. Selected waveforms from experimental results shown in Figure 5.17 verify the implementation and the effectiveness of the proposed DTMC ISVM method. Individual units of the hardware are shown in detail in Appendix I. Figures 5.17 (a) and 5.17 (b) show the output line voltage and the output phase voltage of the DTMC respectively. Figure 5.17 (c) shows the 25Hz output current of the DTMC and Figure 5.17 (d) shows the 50Hz filtered input current of the DTMC.

Figure 5.16 DTMC hardware prototype

(a)

Figure 5.17 (Continued)
Figure 5.17 Hardware output for balanced input condition (a) output phase voltage, (b) output line voltage, (c) output phase current and (d) input phase current
5.7 SUMMARY

In this chapter, the space vector PWM technique for the direct three-level matrix converter has been proposed for synthesizing balanced sinusoidal three-level output voltages from balanced and unbalanced non-sinusoidal input voltages. In addition, conduction losses and switching losses were modelled for the DTMC and a comparative study of the same for the CMC and the DTMC has been carried out.

MATLAB simulation and hardware results verify the effectiveness of the proposed technique. The THD of the output voltage is lower for the DTMC as compared to the CMC. However, the switching losses for the DTMC are higher than those of the CMC.