ABSTRACT

This thesis proposes the modeling and analysis of Static synchronous Compensator (DSTATCOM) systems utilizing Cascaded-Multilevel Converters (CMCs). Among Flexible AC Transmission System (FACTS) controllers, the DSTATCOM has shown feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Referring to the literature reviews, the CMC with separated DC capacitors is clearly the most feasible topology for use as a power converter in the DSTATCOM applications.

The controls for the CMC-based DSTATCOM were, however are very complicated. In order to operate in a high-voltage application, a large number of DC capacitors are utilized in a CMC-based DSTATCOM. All DC capacitor voltages must be balanced in order to avoid over-voltages on any particular link. These uneven DC voltages introduce voltage stress on the semiconductor switches, and also lower the quality of the synthesized output waveforms of the converter.

Previous researches into DC capacitor voltage-balancing techniques were very straightforward, in that individual voltage compensators
were added into the main control loop. However, the compensator design for these individual loops is very challenging because of the complexity of the voltage-loop transfer functions. Basically, the trial and error methods are used for the compensator design which is very complicated for the system with greater number of voltage levels. As a result, this approach potentially reduces the reliability of the controller.

The goal of this thesis is to provide, high-performance, reliable, flexible, cost-effective power stages and controllers for the CMC-based DSTATCOM. Major contributions done in this thesis are given as follows: 1) Optimized design for the CMC-based DSTATCOM power stages and passive components, 2) Accurate models of the CMC for reactive power compensations in both abc and dqo coordinates, 3) DC-link balancing strategies, 4) Improvements in the CMC topology and 5) Analysis of various CMC topology.

To simplify the control system design, well-defined models of the CMC in both abc and dq0 coordinates are proposed. In order to balance the DC capacitor voltages, effective Space Vector Pulse Width Modulation (SVPWM) technique is used, which is suitable for any number of H-bridge converters.
With the combination of the decoupling power control and the cascaded SVPWM, a CMC with any number of voltage levels can be simply modeled as a three-level and five-level cascaded converter, which is the simplest topology to deal with. This significantly simplifies and optimizes the control design process. To verify the accuracy of the proposed models and the performance of the control system for the CMC-based DSTATCOM, three-level and five-level cascaded-based DSTATCOM is implemented in MATLAB/Simulink.