CHAPTER 4  
NEW SVM INVERTER BASED UPFC SYSTEM TO  
REDUCE HARMONICS  

4.1 INTRODUCTION  

The objective of this chapter is to study the reduction in the harmonics of injected voltage of UPFC system. Two bus system with Unified Power Flow Controller is modeled and simulated using the blocks of simulink. Sending end acts as one bus and receiving end acts as another bus. UPFC with PWM inverter and SVM inverter is modeled, simulated and the harmonic analysis is observed. A new SVM based UPFC system is proposed to reduce the harmonics in the injected voltage.

In a transmission system, the independent control of real power and reactive power is essential to maintain the desired voltage level in a transmission system. In this chapter two bus system is considered and it is modeled by using the blocks of simulink. The UPFC is connected in this system to achieve the independent control of real and reactive power. The real power is independently controlled by varying the angle of voltage injection of the UPFC. The reactive power is controlled by varying the magnitude of shunt voltage injected by the UPFC.

Harmonic distortion originates in the nonlinear characteristics of devices and loads on the power system. The harmonic distortion is measured in single quantity as Total Harmonic Distortion (THD). Voltages and currents
having frequency components that are not integer multiples of the frequency at which the supply system is designed to operate are called interharmonics. It can be found in networks of all voltage levels. The main sources of interharmonics waveform distortion are power electronic circuits such as static frequency converters, cycloconverters, induction furnaces and arcing devices. Power line carrier signals are also coming in this category. These harmonics result in failure or misoperation of consumer equipments.

The output of inverter contains odd harmonics. PWM is considered such that lower order harmonics are eliminated. Higher order harmonics are harmless since their magnitude is negligible. The output does not contain even harmonics since the output has odd symmetry. THD is the ratio of harmonic voltage to the fundamental voltage.

In this chapter the harmonic analysis is made for two cases. One is PWM inverter based UPFC system and the other one is SVM inverter based UPFC system. The total harmonic distortion is compared with the two methods.

4.2 CIRCUIT MODEL OF TWO BUS SYSTEM WITH UPFC FOR INDEPENDENTLY VARYING REAL AND REACTIVE POWER

The voltage drop in the transmission system is 20% of rated voltage. Therefore a voltage of 20% of rated voltage has to be injected in the middle of line. UPFC is an ideal device for this purpose. Therefore UPFC is selected. The voltage rating of UPFC is 2.2 KV.

Circuit model of two bus system with UPFC is shown in Figure 4.1 Shunt converter at the sending end is represented as a voltage source ($V_{\text{shunt}}$). The series converter is represented by another source ($V_{\text{serex}}$). Power
measurement block is connected in parallel with the load to measure real and reactive powers. The purpose of increasing the angle is to increase the real power supplied to the load.

Figure 4.1 Circuit Model of 2 Bus System with UPFC

The transmission lines are represented by a lumped reactive impedances. Shunt capacitance is neglected. The load voltage and current waveforms at $\alpha=0^\circ$ are shown in Figure 4.2. The corresponding real and reactive powers are shown in Figure 4.3. Load voltage and current waveforms at $\alpha=36^\circ$ are shown in Figure 4.4. The real and reactive powers with $\alpha=36^\circ$ are shown in Figure 4.5. Load voltage and current waveforms at $\alpha=72^\circ$ are shown in Figure 4.6. The real and reactive powers with $\alpha=72^\circ$ are shown in Figure 4.7.
Figure 4.2 Load Voltage and Current Waveform at $\alpha=0^\circ$

Figure 4.3 Real and Reactive Power at $\alpha=0$

Figure 4.4 Load Voltage and Current Waveform at $\alpha=36^\circ$
Figure 4.5 Real and Reactive Power at $\alpha=36^\circ$

Figure 4.6 Load Voltage and Current Waveform at $\alpha=72^\circ$
In PWM based UPFC system the gating signals of the inverter are generated by comparing a sinusoidal reference signal with a triangular carrier wave. The frequency of reference signal determines the inverter output frequency. The peak amplitude of controls the modulation index, hence controls the RMS output voltage. Based on the carrier frequency the number of pulses per half cycle will be decided.

Figure 4.8 shows the model of UPFC system with Pulse Width Modulated inverter. Figure 4.9 and 4.10 show the input voltage and input current of UPFC system with PWM inverter respectively. Figure 4.11 shows the DC link output voltage. Figure 4.12 and 4.13 show the output voltage and output current of UPFC system with PWM inverter respectively. The frequency spectrum of the UPFC system with PWM inverter is shown in Figure 3.14. It is observed that the total harmonic distortion is 23.22%.
Figure 4.8 Model of UPFC System with PWM Inverter
Figure 4.9 Input Voltage of UPFC System with PWM Inverter

Figure 4.10 Input Current of UPFC with PWM Inverter

Figure 4.11 DC Link Output Voltage of UPFC with PWM Inverter
Figure 4.12 Output Voltage of UPFC with PWM Inverter

Figure 4.13 Output Current of UPFC with PWM Inverter
4.4 SVM BASED UPFC SYSTEM MODEL

Space Vector Modulation (SVM) is quite different from the PWM methods. With PWMs, the inverter can be thought of as three separate push-pull driver stages, which create each phase waveform independently.

SVM, however, treats the inverter as a single unit, specifically, the inverter can be driven to eight unique states. The concept of space vector is derived from the rotating field of ac machine which is used for modulating the inverter output voltage. SVM is a digital modulating technique, where the objective is to generate PWM load line voltages that are in average equal to a given load line voltage. This is done in each sampling period by properly selecting the switch states of the inverter and the calculation of the appropriate time period for each state.

Figure 4.14 Frequency Spectrum of Output Voltage with PWM Inverter
To implement the space vector PWM, the voltage equations in the a-b-c reference frame can be transformed into the stationary d-q reference frame that consists of the horizontal (direct) and vertical (quadrature) axes.

Figure 4.15 Model of UPFC System with SVM Inverter
Then it involves vectorially decomposing a desired voltage space vector \( \mathbf{V} \) into voltage vector components that can be generated using a typical three-phase inverter.

There are eight possible combinations of ON and OFF patterns for the three upper power switches. The ON and OFF states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power switches are determined. Figure 4.15 shows the UPFC with SVM inverter.

4.4.1 Modulation Scheme

There are four steps to perform the space vector modulation:

- First, the reference signals for phase A, B and C are mapped into the Orthogonal d-q coordinates, and are represented by a reference vector \( \mathbf{V}_{ref} \).

- Second, switching vectors are selected, including non-zero and zero vectors to synthesize the reference vector \( \mathbf{V}_{ref} \) for one switching cycle.

- Third, the time durations for all selected switching vector are calculated by a simple trigonometric algorithm. The objective is to make the averaged switching vector in one switching cycle equal to the reference vector \( \mathbf{V}_{ref} \).

- Fourth, the switching vectors are sequenced and dispatched to the switching network.
4.5 MODULATION ALGORITHM

Step 1 :: Read three phase reference voltages. \((V_a, V_b, V_c)\)

Step 2 :: Obtain three-phase to two-phase transformation \((a,b,c \rightarrow d,q)\)

Step 3 :: Calculate absolute value of \(V_d, V_q\) and arctangent \((V_d/V_q)\)

Step 4 :: Identify the sector in which the reference voltage vector lies.

Step 5 :: Select the switching vectors corresponding to the identified sector.

Step 6 :: The switching times are calculated depending on the output voltage vector magnitude.

Step 7 :: Sequence the switching vectors as given by the sequencing scheme (symmetrical).

Step 8 :: Control signals are dispatched for each phase leg of the switching network.

Step 9 :: Output is obtained at the load terminals of the VSI.

Normal inverter is replaced by SVM inverter. Figure 4.16 and 4.17 show the input voltage and input current of UPFC with SVM model respectively. Figure 4.18 shows the DC link output voltage. DC link voltage is 350 volt. Figure 4.19 shows the SVM model. In SVM M shaped voltage is compared with the triangular voltage to reduce the harmonics. The voltages in abc frame are converted to dq frame. The switches are turned on based on the current sector. The output voltages of SVM model are shown in Figure 4.20 and 4.21 respectively. The output currents of SVM model are shown in Figure 4.22 and 4.23 respectively. The frequency spectrum of the UPFC with SVM is shown in Figure 4.24. It is observed that the Total Harmonic Distortion is
7.02%. Hence the SVM inverter based UPFC system has lower Total Harmonic Distortion (THD) than PWM inverter based UPFC system.

**Figure 4.16 Input Voltage of UPFC System with SVM Inverter**

**Figure 4.17 Input Current of UPFC System with SVM Inverter**

**Figure 4.18 DC Link Output Voltage of UPFC System with SVM Inverter**
Figure 4.19 SVM Model

Figure 4.20 Output Voltage of UPFC System with SVM Inverter

Figure 4.21 Output Voltage of UPFC System with SVM Inverter
Figure 4.22 Output Current of UPFC System with SVM Inverter

Figure 4.23 Output Current of UPFC System with SVM Inverter

Figure 4.24 Frequency Spectrum of Output Voltage with SVM Inverter
4.6 RESULTS AND DISCUSSION

4.6.1 Results of two bus system with UPFC model

The real power increases with the increase in the angle of injection. The corresponding graph is shown in figure 4.25. Real power is directly proportional to sine of the angle. Therefore the real power increases with the increase in the angle of injection. The bus voltage increases with the increase in the injected voltage. The reactive power increases with the increase in the shunt voltage. The corresponding graph is shown in Figure 4.26. This is because the reactive power is directly proportional to the square of the voltage. PQ measurement block is connected at the receiving end. Therefore the power measured is the reactive power at the receiving end. The UPFC provides the possibility of operating shunt and series converter separately. In such case the shunt converter operates as STATCOM and the series converter as SSSC.

Figure 4.25 Real Power Versus Angle of Injection
Results of PWM and SVM Inverter based UPFC Model

From the Table 3.1 it is observed that SVM inverter based UPFC is injecting less harmonics than PWM inverter based UPFC system. Hence it is clear that SVM inverter based UPFC system is superior than PWM inverter based UPFC system.

Table 4.1 THD Comparison of PWM and SVM Inverter based UPFC System

<table>
<thead>
<tr>
<th>Harmonic Distortion</th>
<th>PWM Inverter based UPFC system</th>
<th>SVM Inverter based UPFC System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Harmonic Distortion (THD) in %</td>
<td>23.22</td>
<td>7.02</td>
</tr>
</tbody>
</table>
4.7 SUMMARY

The model of UPFC using shunt and series sources is presented and it is connected with the two bus system in this chapter. Variation of real and reactive powers is also presented. It is observed that the real power increases with the increase in the angle of injection. The reactive power increases with the increase in the shunt voltage. The bus voltage increases with the increase in the injected voltage. PWM and SVM based UPFC system is proposed and the results of this system are presented.