CHAPTER IX
SUMMARY AND FUTURE WORK

The thesis covers some important aspects of general-purpose reversible computer design. Design of a reliable system in reversible domain is a centre of attraction to the computer designers, because reversibility is associated with the maximum efficiency of a system. A reliable system design in traditional domain is an interesting open problem and reversibility imposes an additional constraint to the same. A number of frequently used design rules are restricted in reversible domain and all auxiliary computations are to be undone for efficient sharing of resources. For example presence of fanout is inherently restricted in a reversible design. As a result of these inherent constraints, optimal reversible implementation of any known optimal depth circuit becomes very difficult.

Some interesting design-tricks like inverse bijection and replication are introduced in this thesis that ensures reversible implementation of optimal depth circuits. This inverse bijection is helpful for reversible erasure of auxiliary computations leading to an optimal garbage realization. Synthesis of any reversible sequential circuit depends upon a redirection device. The available devices are based on electron wave-guide Y-branch technology and it is difficult to realize these devices in deep-sub-micron domain. In this thesis a CMOS mapping of a redirection device is introduced, that is easily realizable with the help of available technology. This is a big leap towards the development of a general-purpose reversible computer with the help of available technology. Most of the design-tools and design-styles in state-of-the-art VLSI design become readily applicable to reversible domain provided that the restriction on fanout is strictly followed.

In this thesis the following problems are studied:

(i) A comprehensive analysis of functional representation in Mixed Polarity Reed Muller (MPRM) domain is done and some interesting results on duality and self-duality are explored. A linear-time logic array to transform one MPRM form to another is established in the present work that forms the backbone of efficient circuit realization in Reed-Muller domain. It is established in this thesis that an adoptive decision making using greedy approach based upon this logic array results in near-optimal synthesis of any switching function in reversible domain.
(ii) Optimal garbage synthesis of unate symmetric functions and elementary symmetric functions is also explored. A theory on hierarchical synthesis of symmetric and bi-symmetric function is developed to give near optimal synthesis in reasonable amount of time.

(iii) A theory on optimal garbage synthesis of ripple carry adder is developed, using a set of bijective operators introduced in this thesis. Logarithmic-depth synthesis of carry-look-ahead-adder and carry-save multiplier is also explored.

(iv) Optimal level synthesis of a logarithmic barrel shifter using shuffle-exchange network and butterfly network are explored. An optimal garbage synthesis of the same is also done, using a comprehensive theory on in-place shifting developed in this thesis.

(v) Sequential functions in reversible domain are identified, classified and explored. In this thesis it is also established that, realization of arbitrary synchronous sequential machine in reversible domain is possible with the help of a maximal length feed-back-shift-register and other combinational circuits.

(vi) Testability issues of the circuits developed in this thesis are studied. For each of these problems, several design tools are developed and relevant applications have been demonstrated.

9.1 FUTURE WORK

Corollary 4.1 tells that, 'if a switching function $f(X_1, X_2)$ exhibits partial symmetry over two disjoint set of variables $X_1$ and $X_2$ then $f$ can be hierarchically decomposed into a function of $\lceil \log_2 |X_1| \rceil + \lceil \log_2 |X_2| \rceil + 2$ variables'. This is an interesting result that tells that decomposition of arbitrary switching function using its symmetry (and partial-symmetry) elements is an important issue in efficient circuit synthesis.

Classification of a switching function in terms of its symmetry and partial symmetry is an interesting research problem and it requires some exhaustive search, to do the same. The number of equivalent classes is relatively small and each member of the same equivalent class share the same design methodology resulting in a finite number of design methodologies to synthesize arbitrary switching function.

Bijective nature of a Multistage Interconnection Network (MIN) makes it an essential tool in reversible architecture. Optimal reversible synthesis of the functionalities shown in Table 6.2 is of research interest.
Algorithm and Data Structure in reversible domain are important issues as demonstrated in Appendix B. Further work in this area is essential for the development of appropriate software in reversible domain.