CHAPTER 1
INTRODUCTION

1.1 Analog over Digital design-A Perspective

Modern digital IC design technology has replaced the conventional analog ICs for its lack of accuracy in prototyping the design, stability of devices, field programming ability/reconfiguring ability, and design automation. This is despite the fact that analog ICs process information closer to natural processes, have higher resolution, consume less power and have higher integration density [1, 2]. The ever-increasing demand for higher computational capacity and lower power consumption has been driving the research to explore innovative alternatives to address these issues. Substantial research towards high integration densities in digital design technology has been conducted, which permits migration to higher word-width and hence resolutions come closer to analog [3, 4]. However, the high cost of domain conversion from analog to digital and vice versa, increases with increased design complexity, as the “real world” at the macro level is analog. It therefore becomes imperative, to re-consider analog designs, particularly in the case of applications that can be accomplished efficiently in analog domain without migration to digital domain. Some of these devices would include communication devices (e.g. analog RF transmitter, receivers, cellular phones, micro-sensors, high-definition TV, etc.), biologically inspired circuits, medical (like ECG, EEG, pacemakers etc.), ubiquitous sensing, environmental monitoring, automotive industrial and high efficiency lighting applications [5-8]. Appreciating, these efforts have been made in the past decade towards design of reconfigurable, accurately prototype able analog solutions. Analog circuits aim to preserve the accuracy and precision in the signal amplitude and processing time. Thus, analog designing is a process that follows a sequence of steps, in which a trade-off between time and cost of design fabrication has to be maintained. Additionally, the performance of analog circuits are also prone to degradations due to analog fabrication process variations, imperfections and mismatches in CMOS devices. Therefore several efforts to reduce limitations of analog designs by introducing on-chip tuning ability/reconfiguring ability in analog circuits have been
developed. In this context, it would be important to evolve a methodology to overcome the known shortcomings of analog domain.

1.2 Efforts towards On-chip Reconfigurable Analog Circuits

In the last decade, a range of solutions to improve the performance of analog circuits and to upgrade the designs from their shortcomings, have been developed. Several trimming networks and algorithms are used in sophisticated analog designs like analog to digital converter circuits, phase locked loop, low voltage amplifiers, etc. Digital circuitry like resistive ladder, resistor band selector circuit, and piezoelectric resonator circuits have been employed, to introduce on-chip tuning ability of frequency in oscillators and filter circuits [9]. Additionally, RF and analog/mixed signal design have also been introduced in silicon technology [10]. Dynamic programming optimization chip has been developed to correct device mismatches and imperfections with the help of CMOS current mode analog circuits [11]. A number of laser trimming techniques and calibration schemes have also been developed. A radix based digital calibration technique, statistical based calibration, and advance adaptive digital calibration technique, produce ability to correct mismatches in analog devices [12]. Several digital to analog circuit designs have also been proposed, which require resistive laser trimming (an inverted R-2R ladder) to calibrate mismatches occurred in devices [13]. Furthermore, to introduce post-fabrication tuning ability in analog domain and for mismatch corrections, some special layout technique based devices have also been proposed. Such digital designs are less prone to device imperfections and also offer design flexibility and reconfiguring ability. However, digital implementation leads to increase in the chip area and power consumption. Thus with scaling down approach in the process technology, designers look forward towards compact analog based solutions. Additionally, for a device, where, in place of discrete switching, a continuous and high resolution type of programming is required, analog based tunable circuitry is beneficial. Inspired by the success of digital FPGAs, field programmable analog array or FPAA bring in the concept of reconfigurable rapid prototyping for analog domain. These FPAA/RASP (reconfigurable analog signal processor) rely on combinational
logic blocks (e.g. capacitors, resistors, buffers, integrators, OTA, other current mode devices, etc.) and signal routing/switching network (e.g. transistor, switched capacitors, etc.) to rapidly prototype analog circuits, thus, saving on the time and cost of fabrication of ASIC [14-18]. Furthermore, current mode modified FPAAAs and improved RASPs have also been developed [19-22], for operations at a higher frequency. Subsequently, a RASP 2.8 by Hasler et al., consisting of floating gate (FG) elements as switching network for prototyping designs on board, have also been developed [23]. It eliminates the need for extra memory to store the configuration of the switches. The large switching network can occupy large chip area, and can cause signal delay, which can affect real-life continuous-time signals processing sensitive designs when used under extreme conditions (temperature, noise, loads, supplies, process etc.) [16, 24]. With limitation of bandwidth, diverse range of applications, ranging from biologically inspired/medical devices to high frequency communication devices, dedicated application specific analog ICs (due to higher accuracy) are required. In addition to these, ASIC designs exhibit smaller packaging and lower power consumption. However, unlike FPAA advantages, a dedicated analog IC lacks in reconfiguring ability, rapid prototyping ability, etc. Thus, the focus of this thesis is to understand and reduce the major shortcomings of application specific analog IC designs and to explore ways to make it more resilient. A concept/methodology for analog ASIC designing has been proposed, which utilizes on-chip programming ability feature of a special type of Metal Oxide Semiconductor Field-Effect Transistor, called Floating gate MOSFET (FGMOS).

1.3 Proposed Design Solution to overcome limitations

1.3.1 Literature on Floating-gate Transistor

The floating gate (FG) concept and floating gate MOSFET (FGMOS) devices have been used, from decades, in EPROMs [24], EEPROMs and flash memories, as non-volatile memory elements. They are also used as neuronal computational element in neural networks [25-27], analog storage element [28], e-Pots, and in single-transistor DACs. All these devices are utilizing FGMOSs as non-volatile memory, however its applications can be extended with
controlled type of FG charge programming. Recently a lot of different simulation models have been developed for FGMOS, with which controlled programming of charge at the FG can be estimated, which bring back the focus and interest for them in today’s technology world [29-31]. Thomsen and Brooke’s demonstration employs electron tunneling in a standard CMOS double-poly process [32]. Shibata and Ohmi described FGMOS as neuron-MOS [26]. The development of programmable analog floating gate memory array also originates the application of FGMOS in audio recording applications [33]. FGMOSs have been described as multiple-input floating-gate MOS (FGMOS) transistors, which can be used in multiple-input floating gate differential amplifier, a four-quadrant floating-gate multiplier, simple D/A converters, LC oscillator, and trans-linear circuits, etc. [34-36]. In addition, continuous tuning of trans-conductors, hysteresis tunable comparators which use FGMOSs has also been developed [37, 38]. Furthermore, the feature of tunable resistance/conductance across FGMOS has been explored in wide range of applications like they are used to design various filters [39, 40]. FGMOS were also defined like a single-transistor synapse, which emulate some of the computational and adaptive properties of biological synaptic elements [41]. As a result of this, lately there has been a considerable interest in building networks of continuously programmable adaptable floating-gate synapses. The paper [42] classified applications of floating gate device into broadly three aspects where they are used; as analog memory element, as capacitive-based circuit element and as adaptive circuit element. Therefore with development of FG device simulation models and techniques for its fabrication, a wide and significant range of its applications can be explored.

### 1.3.2 Floating Gate Transistor (FGMOS)

FGMOS transistors are just like the conventional MOS transistors with an additional gate, called floating gate. A floating gate (FG) is a second polysilicon gate surrounded by silicon dioxide, which make it perfectly insulated. FG can only be connected to other layers through capacitor, or in other words, FG exists when there is no DC path to a fixed potential. Floating gate is constructed using double poly structure, first poly for control gate and other for FG, and FG is electrically isolated (as covered by oxide), thus charge once introduced at the floating gate,
remains trapped within it. However, quantum processes such as Fowler-Nordheim tunneling and Hot-electron injection, are used to alter this charge at the floating gate [29, 30]. The charge present at the floating gate influences the value of respective FGMOS's threshold voltage. Therefore, with desirable and precise modification of charge onto the floating gate, the threshold voltage, and thus the operating conditions of the FGMOS can be programmed/reconfigured.

1.3.3 Floating Gate Charge Modification/Programming Techniques

In non-volatile memory devices, the information/charge stored on the floating gate can be erased by exposing the gate to the ultraviolet radiation. It erases the entire information in one go, thus this method lacks in the programming of charge. Hence to program this charge with precision, two basic techniques Fowler-Nordheim tunneling and Hot electron injection have been used. Figure 1.1 illustrates the effect of two mechanisms (performed in floating gate N-type MOSFET, FGNMOS), which shows that the floating gate of FGMOS is essentially a capacitance, where injection of electrons onto the floating gate causes reduction of charge at the FG and thus, decrease in the threshold voltage of FGMOS (the I-V curve shifts to the left in FGNMOS and shifts to the right in FGPMOS). Whereas, in the tunneling process, electrons are removed from the floating gate resulting in increased positive charge on the floating gate. This increases the threshold voltage of FGMOS (thus shifts the I-V characteristics to the right in FGNMOS and shifts it to the left in FGPMOS).

In Fowler-Nordheim tunneling, a high potential (called tunneling voltage $V_{\text{tun}}$) is provided at a tunneling junction, which is connected via capacitor, as shown in Figure 1.2. This capacitance is formed by MOS capacitor (formed on n-well, where drain source and substrate of PMOS have been shorted to tunneling junction however, the gate is connected to the floating gate, illustration is given in Chapter 2). The high potential (>12V) at tunneling junction, develops electric field in oxide film, which enhances the energy of carriers and decreases the effective of barrier width, such that they tunnel out from the floating gate. The amount of charge transferred in tunneling depends on the oxide thickness (oxide thickness, $t_{\text{ox}}$, used in fabrication is about 12.5nm) and the potential difference between MOS capacitive plates (i.e., between
tunneling junction and the floating gate). On the other hand in hot-electron injection mechanism electrons get accelerated (through hole impact ionization) and attain an energy level that is enough to overcome the Si – SiO₂ barrier (>3.2eV), and thus carrier get injected to the floating gate [30]. To accelerate carriers which get injected to the floating gate, the potential difference between the drain and source must be kept greater than 5 V/μm and the potential across oxide (floating gate and drain) must also be in a direction that enhances the injection. The injection of charge can be performed on the floating gate, either directly or indirectly, which have been explained in section 1.3.4 on type of programming. FGMOS is usually operated in sub-threshold region (such that the current should be in μA range), because the tunneling and injection currents values are very small (ranged in fA), thus to program their threshold voltage they are operated in this region.

![Diagram](image)

Figure 1.1: $I_d$-$V_{gs}$ characteristic plot of FGNMOS, which shows the effect of tunneling and injection quantum processes on its characteristics (threshold voltage). It illustrates that the initial threshold voltage $= V_T^{REF}$ and with tunneling, it increases to $V_T^1$, however, with injection, it decreased to $V_T^0$.

1.3.4 Type of Programming

There are two basic types of programming, direct or indirect. In direct method, the FGMOS is disconnected from the circuitry and then, the injection of charge is performed by supplying required potential difference between the drain and source of the respective FGMOSs. In hot-
electron injection, the charge (electrons, e\textsuperscript{-}) get injected to the floating gate, as shown in Figure 1.2. To achieve this appropriate switching circuitry is used to connect and disconnect the normal working circuitry from the programming circuitry (FGMOSs) [31]. In this process, the count of transistors in circuit increases about four times, as compared to the original circuit. The process of disconnection decreases the available time of operation. For run-time programming, reduced transistor count, reduced number of parasitic capacitances and better operational speed, direct type of programming may not be a preformed option. On the other hand, in the indirect method of programming, programming of charge at the floating gate is performed using programmer FGMOS whose floating gate is common to the floating gate of FGMOS and hence, eliminates the need of detaching the FGMOS from its circuitry, while programming. For injection the required drain to source potential difference of programmer FGPMOS and in tunneling a high potential at the tunneling junction is established, as shown in Figure 1.3(a), to program charge at the common floating gate. In addition, the process of injection (hole impact ionization) shows better efficiency in performance when it is performed in PMOS than NMOS. To design a floating gate in N type MOSFET, indirect method of programming is preferred, where for injection of carrier at the common floating gate, a programmer FGPMOS is used, as illustrated in Figure 1.3(b). However, threshold voltage programming of FGNMOS using programmer FGPMOS as PMOS and NMOS are complementary to each other, thus, their operation with common biasing conditions, is very challenging to attain, simultaneously. Restricting the FGMOS operation to sub-threshold region is therefore desirable as it simplifies the current-to-current ratio. In this regard careful operating conditions (biasing) have to be considered such that both FGNMOS and FGPMOS can operate at sub threshold region, simultaneously (experiment results of fabricated FGNMOS demonstrated in Chapter 2). The chip area consumed by indirectly programmable FGMOS devices, illustrated in Chapter 2, is about 130×90 µm\textsuperscript{2}. FGMOS devices can be used as non-volatile on-chip programmable analog translinear element. They can be used in various significant applications, which act as a building block of our research work.
Figure 1.2: Depicts directly programmable FGPMOS where injection (required drain to source potential of FGPMOS, for injection of electrons, i.e., decrease of charge at floating gate) and tunneling (high potential at tunneling junction, $V_{tunnel}$, which causes tunneling of electrons, i.e. increase of charge at floating gate) is performed directly on FGPMOS, after disconnecting it from the main circuit. And the floating gate is fabricated using double polysilicon technology, which is represented as capacitance at input between gate and floating gate.

Figure 1.3 (a) Depicts indirectly programming of FGPMOS using programmer FGPMOS (injection of electrons at the floating gate with the help of required potential difference at drain and source at programmer FGPMOS and tunneling of electrons from the floating gate with the help of very high potential, $V_{tunnel}$ at tunneling junction); and (b) Shows Indirect programming of FGNMOS using programmer FGPMOS, where injection mechanism has been carried out by programmer FGPMOS and tunneling through $V_{tunnel}$, thus, the charge at the common floating gate has been programmed, and hence, threshold voltage (Characteristics) of FGNMOS has been programmed.
1.4 Objectives of the research work

The focus of this thesis is to understand the major shortcomings of application specific analog IC designs and to come up with a methodology that can overcome the limitations. The main objective is to propose innovative methods that can provide control on offsets, which occur during fabrication processes, due to CMOS device mismatches and imperfections. This is achieved by introducing features like, reconfiguring ability, post fabrication tuning ability, adaptability, stability, and accurate prototyping ability in CMOS based analog ICs. Therefore to achieve the objectives, the concept of on-chip tuning ability of MOSFET’s threshold voltage using FGMOS transistors, has been employed in designing CMOS based reconfigurable/on-chip tunable analog ICs. Efforts are made to fabricate FGMOS transistor devices such that these transistors can be characterized and on-chip programming/tuning ability of FGMOS’s threshold voltage can be verified. Programming of threshold voltage of FGMOS enables the analog designers to overcome some basic limitations like device mismatch or DC offset [43, 44] by introducing post-fabrication prototyping/reconfiguring ability in analog domain. To implement FGMOS in several CMOS based analog circuit designs and to simulate such designs, FGMOS simulation models need to be designed, and generalized for all simulation tools like, T Spice or Virtuoso. Implementation of FGMOSs in CMOS based analog designs with the help of its simulation model shows that with on-chip tuning ability of FGMOSs, several enhanced features like, on-chip programming/reconfiguring ability and adaptability can be introduced in analog ICs. Imperative analog devices like on-chip tunable RF Active inductor, tunable RC Oscillator, tunable Band-pass filter, on-chip programmable Controller circuits (current conveyor, op-amp, operational transresistance and transconductance amplifiers), and on-chip programmable Voltage reference circuit can be designed using FGMOS transistors. Hence the main objective is to generalize the utilization of FGMOS technology in fabricating reconfigurable analog ASICs. A new design methodology for analog circuits has been proposed, such that the design specifications of analog devices can be accurately prototyped/reconfigured to the desired value at the user’s end, with the help of post-fabrication programming of circuit FGMOS’s
characteristics. If indeed this is possible, it can help alleviate the problem of maintaining a large inventory of devices over a variety of specifications, besides, bringing down the cost per chip. Thus, there is a real possibility of building generic devices with field programmability feature to provided wide, continuous and independent variation of design specifications. This not only helps to overcome the limitations of accurate prototyping ability, but also provides control on variability in specifications over a fair range. Furthermore, when tuning (of charge/threshold voltage) feature is clubbed with feedback, then adaptive feature (self-adaption of charge at the floating gate) can also be introduced, which develop scope for future research work.

1.5 Thesis Outline

The thesis is framed in broadly five chapters. Chapter 2 incorporates simulation, design, fabrication, and characterization of FGMOS. It discusses on-chip programming/tuning ability of FGMOS’s threshold voltage, and estimates programming range and resolution from experimental results. FGMOS devices have been fabricated using C5 0.35µm, ON-Semiconductor technology from MOSIS fabrication Services, USA, under educative program. These fabricated FGMOS devices have been characterized and programmed via injection and tunneling of charge, using Keithley Semiconductor Characterization System (Keithley SCS-4200) in VLSI Design lab, DEI.

Chapter 3 focuses on tunable analog IC designs, using on-chip tunable FGMOS feedback resistor. The FGMOS active resistor can be tuned with fairly high precision as threshold voltage of FGMOS can be programmed by means of on-chip programming using external voltages. We also evaluate programming resolution, where programming resolution refers to the minimum voltage change in tunneling voltage or injection voltages that can bring change in the characteristic plot (threshold voltage) of FGMOS. To demonstrates its effectiveness, a tunable active resistor has been used in a clock generator circuit [47], which produces clock whose frequency can be precisely, continuously, non-volatile type of tuning in range the from 0.85 MHz to 10 MHz. The proposed design has been published in [48, 49]. Additionally, the application of tunable FGPMOS resistor has also been extended to RF design.
A fine tuned RF active inductor has also been simulated and fabricated, which is a gyrator based high Q tunable inductor design [50]. In proposed design, instead of feedback (digitally trimmed) resistor an on-chip tunable FGMOS resistor has been used. At a particular biasing and sizing condition, it produces inductance tuning range from 3nH to 8nH operating in the range of 0.85GHz to 1.25GHz. The proposed design has also been published in [51].

Chapter 4 proposes a new design methodology for analog circuit designing. The capacity to fine tune and field program the FGMOS threshold voltage $V_T$ brings into focus a very interesting new dimension in the design of ASICs. The conventional analog design cycle of ASICs revolves along building the functionality and optimizing of W/L ratios of the constituent MOSFETs such that desired specifications of the design can be achieved. The variability in parameters, post-fabrication deviations, limits the capacity for accurate prototyping of analog circuits using the conventional process. However with the implementation of FGMOSs in design, the design specifications are re-derived in terms of threshold voltages of the respective FGMOSs, and thus they can be set to desired values after fabrication. This hold potential for prototyping of designs to become simpler and faster. The proposed methodology has been published in [52, 53]. To illustrate and verify the proposed design methodology, four basic programmable controlled devices (CCCII, OTA, OTRA, and Op-amp) have been designed according to the proposed design cycle. The related work has been published in [54-57].

Chapter 5 discusses how the tuning feature in analog IC when clubbed with an appropriate feedback circuit, to bring in a feature of adaptability to the analog circuit designs. A CMOS based on-chip programmable voltage reference circuit has also been designed using FGMOSs and published in [58], which also show self-adaption to changes like temperature, power supply etc. A self adaption of charge at floating gate has been studied [59] and simulated using proposed FGMOS simulation model, which can enhance the applicability of floating-gate devices in capacitor-based continuous-time filters, sensor interface circuits, etc. An application of self adaptive FGMOS has also been simulated [60]. Therefore the foremost intention is to generalize the augmentation of features like tuning ability, on-chip programming ability/reconfiguring ability, accurate prototyping ability and adaptability in analog devices. In
the work these features have been developed using FGMOSs. The concept/designs can be
generalized using other analog compact solution and hence develop interest in analog devices.