STUDY AND COMPARISON OF CHARACTERISTIC PARAMETERS OF ASYMMETRIC HALO, UNIFORMLY DOPED SINGLE HALO DUAL MATERIAL GATE, DOUBLE HALO DUAL MATERIAL GATE AND DOUBLE GATE MOSFETS

4.1 INTRODUCTION

The channel engineering techniques minimise the hot electron injection in short-channel metal–oxide–semiconductor field-effect transistor (MOSFET). The basic principle of the pocket-implanted devices is to keep the depletion layers at a minimum by increasing the substrate doping at both the ends of the device. So, the short-channel effects (SCE) arise as a result of the two-dimensional (2D) potential distribution and high electric fields in the channel region (Baishya, Mallik, and Sarkar 2006). In this article, an analytical model of the subthreshold surface potential is derived assuming the linear profile of the pocket doping. From Tsormpatzoglou, Dimitriadis, Clerc, Pananakakis, and Ghibaudo (2008), it is observed that the linear pocket doping gives a better result for the threshold voltage. Here, the one-dimensional (1D) pocket profile across the channel has been transformed into an effective doping concentration expression which is used in the pseudo-2D Poisson’s equation, formulated by applying Gauss’s law to a rectangular box covering the entire depletion layer depth in the channel.

A dual-material gate (DMG) MOSFET can suppress SCE effectively (Baishya, Mallik, and Sarkar 2006a,b; De, Sarkar, and Sarkar 2008). In the DMG MOSFET, the work function of the metal corresponding to gate1 (M1) is greater than that for gate2 (M2) and hence the threshold voltage corresponding to M1 (Vt1) is greater than that corresponding to M2 (Vt2). This has the inherent advantage of improved gate transport efficiency by modifying the electric field profile along the channel. Due to different work functions of
two gates, the surface potential profile is a step function, which ensures a reduction in the short-channel effects and screening of the channel region under the M1 from the drain potential variations. To reduce the short channel effects, the channel engineering approach like the single-halo (SH) also known as the lateral asymmetric channel or double-halo (DH) implants are used (Sarkar, De, Nagarajan, Sarkar, and Baishya 2008). The channel engineering and the gate engineering techniques are combined to form novel device structure like the single halo dual material gate (SHDMG) and double-halo dual material gate (DHDMG) MOSFETs. An accurate model of subthreshold surface potential, threshold voltage and drain current is proposed for the DHDMG and the SHDMG MOSFETs.

4.2 SURFACE POTENTIAL OF ASYMMETRIC HALO

The pocket-implanted n-MOSFET structure shown in Figure 4.1 is used to develop and implement the model. Reverse short-channel effect (RSCE) is caused due to the pocket implantation, done by adding impurity from both the source and the drain ends. The maximum pocket doping concentration is \( N_m \), which gradually decreases linearly towards the substrate concentration \( N_S \) with a pocket length \( L_p \) from both the source and the drain ends. So, the doping concentration decreases from the maximum value at the source and the drain ends to the substrate doping value, linearly along the channel, as shown in Figure 4.2(a) and (b). \( N_m \) and \( L_p \) play important roles in determining the RSCE (Sarkar, De and Sarkar, 2011).

All the device dimensions are measured from the oxide–silicon interface. At the source side, the pocket profile is given as

\[
N_{S_X} = N_S (x / L_p) + N_m [1 - (x / L_p)]
\]

(4.1)
Figure 4.1: n-MOSFET pocket implanted structure.

The drain-side profile is given in the following equation

\[ N_{dx} = N_S \left\{ \frac{(L/L_p) - (x/L_p)}{1 \pm \left( x/L_p - (L/L_p) \right)} \right\} + N_m \left[ 1 + \left( x/L_p - (L/L_p) \right) \right] \]  

(4.2)

Here, \( x \) indicates the distance along the channel. In the model, the pockets are assumed symmetrical at both ends.
Figure 4.2 (a,b): Pocket implant concentration plots v/s the channel length curves for the increasing $L_p$ and $N_m$ respectively.

Since at the source side, the doping concentration is $N_{sx}$, at the drain side $N_{dx}$ and the substrate has concentration $N_s$, the average effective concentration is given by

$$N_{eff} = (1/L) \int_0^L \left[ N_{sx} + N_{dx} + N_s \right] dx \quad (4.3)$$

Substituting the values of $N_{sx}$ and $N_{dx}$ from (4.1) and (4.2) in (4.3) and after integration, we get

$$N_{eff} = N_s \left\{ 1 - \left( L_p / L \right) \right\} + N_m \left( L_p / L \right) \quad (4.4)$$

Application of Gauss’s law to a rectangular box in the channel depletion region yields the following 1D equation which can be analysed analytically:

$$\varepsilon_{si} \frac{d^2 \psi_s}{dx^2} - \frac{C_{ox}}{Y_d} \psi_s = qN_{eff} - \frac{C_{ox}}{Y_d} V'_{GS} \quad (4.5)$$

where $V'_{GS} = V_{GS} + V_{SB} - V'_{SB} \psi_s(x)$ is the surface potential with respect to interior of the substrate bulk, $V_{SB}$ is the source-to-body voltage, $V_{GS}$ is the gate-to-source voltage, $t_{ox}$ is the gate oxide thickness, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area,
$N_{eff}$ is the average effective concentration, $V_{FB}$ is the flat-band voltage, $Y_d$ is the depletion layer depth and $\varepsilon_{si}$ and $\varepsilon_{ox}$ are the dielectric permittivities of Si and SiO$_2$ respectively.

**Fringing capacitance model:**

An accurate model must take into account the fringing effect for perfect estimation of surface potential. The fringing potential due to the inner fringing capacitances is introduced in the model.

![Image of fringing capacitance components](image)

Figure 4.3: Fringing Capacitance Components C1, C2, and C3.

C1 is the outer-fringing-field capacitance between the gate and the source or the drain electrode. C2 is the direct overlap capacitance between the gate and the source or the drain junction. C3 is the inner-fringing-field capacitance between the gate and the side wall of the source or the drain junction. The expressions of C1, C2, and C3 are given in details in (De et al. 2008; Sarkar et al. 2008). Here $\alpha$ is the slanting angle of the gate electrode in radians, $T_{GATE}$ is the thickness of the gate electrode as shown in Figure 4.3.

Further, $C_F$ is the maximum value of the inner-fringing capacitance component C3. Hence from Park, Ko, and Hu (1991), De et al. (2008) and Sarkar et al. (2008),

$$Q_{D,F} = -C_F \cdot \frac{V_{DS} - V_{DS}}{1 + \exp\left(-\frac{V_{GB} - V_{FB}}{30\phi}\right)} = -C_F \cdot V_{fd}$$  (4.6)
\[ Q_{s,F} = -C_f \cdot \frac{V_{GST} - V_{GS} + V_{FB} + 2\phi_f + \sqrt{2\phi_f - 3\phi_f}}{1 + \exp\left(\frac{-V_{GB} - V_{FB}}{3\phi_f}\right)} = -C_f \cdot V_{fs} \]  

(4.7)

Here \( V_{DS} \) = drain to source voltage, \( V_{GS} \) = gate to source voltage, \( V_{GB} \) = gate bias and \( V_{FB} \) = flat-band voltage. \( V_{DS} \) is obtained from Park et al. (1991), \( \phi_f \) = Fermi potential of Silicon. \( V_{GST} = V_{GS} - V_T \), where \( V_T \) is the threshold voltage. \( \phi_i \) = Thermal voltage. \( V_{fs} \) = the inner fringing potential in the source end and \( V_{fd} \) = the inner fringing potential in the drain end. \( Q_{D,F} \) = charge induced in the drain due to inner fringing capacitance and \( Q_{S,F} \) = charge induced in the source due to inner fringing capacitance.

An empirical model for the depletion layer depth is proposed as \( Y_d(x) = (ax + b)^2 \), which is essential for solving (4.5), with the source and drain end values given by

\[
Y_d(0) = X_j + \sqrt{2\varepsilon_{ni} (V_{SB} + V_{bi} + V_{fs}) / qN_{eff}} = X_j + X_{rs} \tag{4.8}
\]

and

\[
Y_d(L) = X_j + \sqrt{2\varepsilon_{ni} (V_{SB} + V_{bi} + V_{fd}) / qN_{eff}} = X_j + X_{rd} \tag{4.9}
\]

respectively. \( X_j \) is the junction depth,

\[
X_{rs} = \sqrt{2\varepsilon_{ni} (V_{SB} + V_{bi} + V_{fs}) / qN_{eff}} \tag{4.10}
\]

and

\[
X_{rd} = \sqrt{2\varepsilon_{ni} (V_{DB} + V_{bi} + V_{fd}) / qN_{eff}} \tag{4.11}
\]

are the depth of penetrations of the depletion layers into the channel/substrate due to the built-in potential \( V_{bi} \) (between the \( n^+ \)-source/drain and the \( p \)-type channel/substrate) and the reverse bias \( V_{SB} \) and \( V_{DB} \) at the source and drain ends respectively, \( L \) is the effective channel length defined as the distance from the edge of the source to the edge of the drain as shown in Figure 4.1. In general, due to the two pocket in this case, we have to divide the channel into five regions so far as the depletion layer is concerned. Two bias dependent fitting parameter \( \zeta_s = 2(V_{sb} + V_{bi} + V_{fs}) / V_{bi} \) for the source side and \( \zeta_d = 2(V_{db} + V_{bi} + V_{fd}) / V_{bi} \) for the drain side is used to take into account the other fringing capacitances and various leakage capacitances. \( \psi_s \) in all the five regions may easily be computed by finding \( \psi_{s(t)} \) for all the five regions.
4.2.1 THRESHOLD VOLTAGE AND DRAIN CURRENT MODEL OF ASYMMETRIC HALO AND UNIFORMLY DOPED DHDMG

Using the above surface potential model, the threshold voltage $V_T$ which is the gate voltage $V_{GS}$ at which the minimum value of the subthreshold surface potential

$$\psi_{S,\text{min}} = 2 \phi_F + V_{SB}$$

(4.12)

is found out. But $\psi_{S,\text{min}}$ occurs at a particular value of $x$ defined as $x_{\text{min}}$. For our purpose the value of $V_{GS}$ for which the minimum value of surface potential is equal to $2 \phi_F + V_{SB}$ is found out for different channel length, substrate doping, etc. Now $x_{\text{min}}$ corresponding to $\psi_{S,\text{min}}$ is approximated at the junction of regions 2 and 3 or regions 3 and 4. Hence, an iterative numerical method is applied to find the value of threshold voltage.

It is seen that the drain current $I_D$ depends on the drain-to-source voltage $V_{DS}$ strongly for the short channel devices. Also the conduction layer depth of the channel depends on the threshold voltage. Taking the positive direction of $x$ as reference as in Figure 4.1, the drain current density is given by

$$J_n = -q \mu_n \phi_i \left\{ \left( -n/\phi_i \right) \left( d\psi_S / dx \right) + (dn/dx) \right\}$$

(4.13)

as in [3].

Here $n$ = inversion layer electron density, $\mu_n$ = electron mobility in inversion layer. Since the doping concentrations at both ends, $N_S(x)$ and $N_d(x)$ vary with $x$ and since $N_S$ is the substrate doping, we take the average concentration $N_{\text{eff}}$ for finding $J_n$. So after multiplying both sides of (4.13) by $\exp(-\psi_S/\phi_i)$ and then integrating,

$$J_n = -q \mu_n \phi_i N_{\text{eff}} \left\{ \exp(-\psi_S(L)/\phi_i) - \exp(-\psi_S(0)/\phi_i) \right\}/ \int_0^L \exp(-\psi_S(x)/\phi_i) dx$$

(4.14)

The effective conduction layer depth in depletion or weak inversion is given by

$$\delta = \phi_i \sqrt{\varepsilon_S} / \left\{ 2q N_{\text{eff}} (2\phi_{F,\text{av}} + V_{GT} / 1.5) \right\}$$

(4.15)

where $V_{GT} = V_{GS} - V_T$. Similarly,
\[ \alpha = \exp[0.27\{\{E_s/(2^*q)\} - \phi_{FHV}\}/\phi] - \{(2^*V_{GB})/(\phi_{FHV} + \phi)\}] \]  (4.16)

The corrected drain current is obtained by integrating the current density over the cross section of the conducting channel, given as

\[ I_{DS} = J_n * W * \delta * \alpha \]  (4.17)

where \( W \) is the device channel width.

4.2.2 SUBTHRESHOLD SURFACE POTENTIAL OF UNIFORMLY DOPED DHDMG

An n-channel Double-Halo DMG-MOSFET structure is shown in Figure 4.4.

Figure 4.4 An n-channel Double-Halo DMG-MOSFET structure.

By applying Gauss’s law to the box shown in Figure 4.5 and neglecting the inversion layer charges in the channel depletion region, a pseudo-2D Poisson’s equation can be obtained as follows:

\[ \varepsilon_s \frac{d^2\psi_s}{dx^2} - \frac{C_{ox}}{Y_d} \psi_s = qN_a - \frac{C_{ox}}{Y_d} V_{GS} \]  (4.18)

where the symbols have their usual significances (Baishya, Mallik, and Sarkar 2006; De et al. 2008; Sarkar et al. 2008). The flat-band voltages for the gate metals are given by

\[ V_{FB1} = (W1 - W_{si})/q. \]  (4.19)

\[ V_{FB2} = (W2 - W_{si})/q \]  (4.20)
where $W_1$ and $W_2$ are the work functions of the gate metals and $W_{si}$ that of the silicon substrate respectively. It is considered that $W_1 > W_2$.

Figure 4.6 Typical variation of the depletion layer depth $Y_d(x)$.

The typical variation of the depletion layer depth for the Double Halo Dual Material Gate MOSFET is shown in Figure 4.6. A model is proposed taking the variation of depletion layer width as $Y_d(x) = (ax + b)^2$ where the source and the drain end values are given by

\[ Y_d(0) = X_j + \sqrt{2\varepsilon_{si}(V_1)(qN_p)} = X_j + X_{rs} \]  \hspace{1cm} (4.21)

and

\[ Y_d(L) = X_j + \sqrt{2\varepsilon_{si}(V_7)(qN_p)} = X_j + X_{rd} \]  \hspace{1cm} (4.22)

respectively where, $V_1 = V_{SB} + V_{bi}$, $V_7 = V_{DB} + V_{bi}$, $V_{bi}$ is the built-in potential of the substrate. $V_{SB}$ and $V_{DB}$ are the source and the drain bias respectively, $N_a$ is the acceptor ion concentration, $X_{rs} = \sqrt{2\varepsilon_{si}(V_1)(qN_p)}$ and $X_{rd} = \sqrt{2\varepsilon_{si}(V_7)(qN_p)}$ are the depth of penetrations of the depletion layers into the channel / substrate due to the built-in potential $V_{bi}$ (between the n$^+$-source/drain and the p-type channel/substrate) and the reverse bias $V_{SB}$ and $V_{DB}$ at the source and the drain ends. The channel is divided into six regions $R_1, R_2, R_3, R_4, R_5, R_6$ with the known values at the two ends as shown in Figure 4.6. Two bias dependent fitting parameters $\zeta_s = 1.5V_1 / V_{bi}$ for the source end and $\zeta_d = 1.5V_7 / V_{bi}$ for the drain end are considered for obtaining a best fit model of surface potentials profile with ISE TCAD.
The depth of the depletion layer(y) for the six regions are as follows:

Region-I : \(x_1 = 0 < x \leq x_2 = L_p\) The corresponding y values are

\[y_1 = \left\{X_j + \sqrt{2\varepsilon_s V_j / (qN_p)} \right\} / \zeta_s \text{ and}\]

\[y_2 = Y_{sp1} = \sqrt{2\varepsilon_s \psi_{sp1} / (qN_p)}\]

with the end potentials \(V_1\) given and \(V_2\) to be evaluated where

\[\psi_{sp1} = \left( -\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p^2}{4} + V_{GB} - V_{FBP}} \right)^2,\]

\[\gamma_p = \sqrt{2\varepsilon_s N_p / C_{ox}}, V_{FBP1} = V_{FBP} - V_{FB1}\]

and

\[V_{FBP} = -0.56 - \varphi_l \ln \left( \frac{N_p}{n_i} \right)\]

Region-II : \(x_2 < x \leq x_3 = x_{ns}\) : The corresponding y values are

\[y_2 = Y_{sp1} \text{ and } y_3 = Y_{sp2} = \sqrt{2\varepsilon_s \psi_{sp} / (qN_p)}\]

where \(\psi_{sp} = \left( -\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p^2}{4} + V_{GB} - V_{FBP}} \right)^2\)

Region-III : \(x_3 < x \leq x_4 = L_1\) : The corresponding y values are \(y_3 = Y_{sp}\)

\[y_4 = Y_{s1} = \sqrt{2\varepsilon_s \psi_{s1} / (qN_a)}\]

where \(\psi_{s1} = \left( -\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}} \right)^2,\]

\[\gamma = \sqrt{2\varepsilon_s N_a / C_{ox}}\]

Region-IV : \(x_4 < x \leq x_5 = (L_1+L_2)0.65\) : The corresponding y values are \(y_4 = Y_{s1}\) and \(y_5 = Y_{sp}\)

Region-V : \(x_5 < x \leq x_6 = L-L_p\) : The corresponding y values are \(y_5 = Y_{sp}\)

\[y_6 = Y_{sp2} = \sqrt{2\varepsilon_s \psi_{sp2} / (qN_p)}\]

where \(\psi_{sp2} = \left( -\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p^2}{4} + V_{GB} - V_{FBP2}} \right)^2,\]

\[V_{FBP2} = V_{FBP} - V_{FB2}\]

Region-VI : \(x_6 < x \leq x_7 = L\) : The corresponding y values are \(y_6 = Y_{sp2}\) and \(y_7 = \left\{X_j + \sqrt{2\varepsilon_s V_j / (qN_p)} \right\} / \zeta_d\)
The surface potential $\Psi_s(x)$ can be determined as by Baishya et al. (2006a,b, 2007), De et al. (2008) and Sarkar et al. (2008).

4.2.3 SURFACE POTENTIAL, THRESHOLD VOLTAGE AND DRIFT-DIFFUSION THEORY BASED DRAIN CURRENT MODEL OF UNIFORMLY DOPED SHDMG

Figure 4.7 The structure of the n-channel Single-Halo DMG-MOS transistor.

The same model is applied for the Single-Halo Dual Material gate MOSFET, the structure of which is shown in Figure 4.7.

Figure 4.8 Typical variation of the depletion layer depth $Y_d(x)$. 

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The typical variation of the depletion layer depth is shown in Figure 4.8. The channel is divided into five regions $R_1$, $R_2$, $R_3$, $R_4$, $R_5$ with known values at the two ends with the source and the drain end values given by

The threshold voltage $V_T$ defined as the gate voltage $V_{GS}$ at which the minimum value of the subthreshold surface potential is obtained is given as

$$\psi_{S,\text{min}} = 2*\phi_F + V_{SB} \quad (4.23)$$

The drift-diffusion model for drain current that widely used for long-channel MOSFETs, give drain current density for an nMOS transistor as (Tsormpazoglou et al. 2008).

$$J_n = -q\mu_n\phi_F N_a e^{-\psi,(L)}/\phi_F - e^{-\psi,(0)/\phi_F} \int_0^L e^{-\psi,(x)/\phi_F} dx \quad (4.24)$$

In weak inversion, the effective channel conduction layer thickness, estimated as the distance from the interface to the location where the potential has changed by $\phi_t$ can be approximated by

$$\delta = \phi_t \sqrt{\frac{\varepsilon_{si}}{2qN_a \left(2\phi_F + V_{GT} / \eta\right)}} \quad (4.25)$$

Where $V_{GT} = V_{GS} - V_T$ is the gate overdrive voltage and $\eta$ is a fitting parameter.

The corresponding drain current is obtained by integrating the current density over the cross section of the conducting channel, given as

$$I_{sub} = J_n W \delta \quad (4.26)$$

where $\delta$ is the effective channel conduction layer thickness, $W$ is the device channel width and $\mu_n$ is the electron mobility in the inversion layer.

### 4.3 SIMULATION RESULTS AND COMPARISON

The polysilicon gate MOSFET structure shown in Figure 4.1 is used to verify the surface potential model against the 2D numerical device simulator DESSIS of ISE TCAD. The gate, source and drain contacts of the MOSFET are made of n-type polysilicon and the body contact of p-type polysilicon.
Figure 4.9. Surface potential profiles with $L_P=16$ mm, $N_{eff}=1.2\times10^{18}$ cm$^{-3}, N_i=6\times10^{17}$ cm$^{-3}$ under the applied bias $V_{SB}=V_{GS}=0$V: $L=80$ and 100 nm, $V_{DS}=1$V are used.

Figure 4.10. Threshold voltage vs. channel length curves for the various drain biases at zero substrate bias as in references (Zhou et al. 1999; Sarkar, De, and Sarkar 2011).

From Figure 4.9, it is evident that the surface potential minima shifts upwards as the channel length is decreased from 100 to 80 nm, keeping the drain bias fixed at 1V. This occurs as a result of widening of the depletion layer under the gate.

The simulated $V_T$ versus L curves have been drawn for this new model for the different
drain and substrate biases. From Figure 4.10, it is observed that with an increase in the drain voltage from 0 to 2 V, both RSCE and SCE take place at a larger channel length due to the drain-induced barrier lowering (DIBL) effect.

![Graph showing threshold voltage vs. drain voltage plots for L=50nm and 100nm with source-to-body voltage of 0V. Neff = 6x10^{17} cm^{-3} is considered under the applied bias V_{BS} = 0V and V_{DS} = 0.5 V.]

Figure 4.11. Threshold voltage vs. drain voltage plots for L=50nm and 100nm with source-to-body voltage of 0V. Neff = 6x10^{17} cm^{-3} is considered under the applied bias V_{BS} = 0V and V_{DS} = 0.5 V.

The DIBL effect is more for smaller channel lengths. As the drain bias increases, the threshold voltage (Figure 4.11) becomes negative. For shorter channel length since the electric field is very high, the potential barrier is lowered.

Our linear pocket profile model exhibits better results of suppressing the SCE compared to the other models for the pocket profiles based on Gaussian (Zhou, Lim, and Lim 1999) and hyperbolic cosine functions (Zhou, Lim, and Lim 2000), as can be observed from Figure 4.12(a).
Figure 4.12. (a) Threshold voltage vs. channel length plots for linear, Gaussian and hyperbolic cosine pocket profiles. (b) Effective carrier concentration with channel lengths for linear, Gaussian and hyperbolic cosine pocket profiles for $N_p=1.75 \times 10^{18}$ cm$^{-3}$, $L_p=25$nm and $N_i=4.2 \times 10^{17}$ cm$^{-3}$.

The effective carrier concentration increases smoothly along the linear pocket profile as the channel length decreases, as shown in Figure 4.12(b), while for hyperbolic cosine function, it starts to increase after 200 nm. But the SCE starts before 0.1 mm. So, for hyperbolic cosine model, first SCE starts and then RSCE takes place. However, for Gaussian function, the effective carrier concentration increases more rapidly than that for linear model. So, we observe that RSCE is stronger. In this case, the threshold voltage increases up to 40 nm.
Figure 4.13. Comparison of experimental data from Yu et al. (1997) with the simulated results of our proposed model.

In Figure 4.13, we tried to compare experimental data obtained from Yu, Wann, Nowak, Noda, and Hu (1997) with our simulated data for the device parameters given in Yu et al. (1997). From the plots, it is clear that our simulated data almost matches the experimental data.

Figure 4.14. Drain current vs. gate voltage for a typical 130nm technology node device with $L=100$ nm, $V_{SB}=0$V and two drain voltages with (1) $N_{eff} =1.7\times10^{18}$ cm$^{-3}$ and $N_s = 9\times10^{17}$ cm$^{-3}$ (2) $N_{eff} =1.2\times10^{18}$ cm$^{-3}$ and $N_s = 6\times10^{17}$ cm$^{-3}$. 
Figure 4.15. Surface potential vs. channel length of DHDMG for three different values of the $V_{DS}=0.25$, 0.5, and 2V for $L=100$nm and two different doping concentrations of $N_a=1\times10^{17}$ and $4\times10^{17}$ cm$^{-3}$ and $N_p=1.2\times10^{18}$ cm$^{-3}$ against the applied voltages $V_{GS}=0V=V_{GB}=V_{SB}$.

It is observed from the plots that due to the reduction of the SCEs, an increased drain voltage reduces the subthreshold drain current (Figure 4.14) and increases surface potential (Figure 4.15).

Figure 4.16. Surface potential vs. channel length for DHDMG taking $L=40$, 80 and 100nm and $t_{ox}=1.5$, 2 and 3 nm, keeping $N_a=1\times10^{17}$ and $N_p=1.2\times10^{18}$ cm$^{-3}$ fixed.

The proposed structure shown in Figure 4.4 is used to verify the model against the 2D numerical device simulator DESSIS. Two different metals M1 and M2 are used. The
typical parameters for the oxide thickness, the junction depth and the channel length are $t_{ox}=3.5$ nm, $X_J=40$nm and $L=100$nm which are representative for a typical 130-nm device, along with $V_{SB}=0$V are used. Similarly, unless or otherwise specified, equal values for $L_1$ and $L_2$ with typical work functions $W_1=4.25$ eV and $W_2=4.1$ eV are used in this study. For an n-channel MOSFET, $W_1 > W_2$ is considered (Kumar and Chaudhry 2004).

It is seen that as $t_{ox}$ decreases, the oxide capacitance increases, the gate control increases and the surface potential (Figure 4.16) decreases. Further reduction of $t_{ox}$ causes quantum tunneling effects to come into the picture. As a result, the model performance gets degraded with further decrease of $t_{ox}$. Instead high-k gate dielectric materials can be used having higher value of permittivity. Since the permittivity is very high, the value of gate capacitance is high even for higher value of dielectric thickness.

![Diagram](image)

**Figure 4.17.** Surface potential vs. channel length of DHDMG for three different values of the $V_{DS}=0.1$, 0.3, and 0.8V for $L=40$nm and doping concentrations of $N_d=1\times10^{17}$ and $N_p=1.2\times10^{18}$ cm$^{-3}$ against the applied voltages $V_{GS}=0$V=$V_{GB}=V_{SB}$. 

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Figure 4.18. Subthreshold drain current vs. gate bias of DMG, SHDMG, DHDMG and short channel MOSFET with $V_{DS}=0.5\,\text{V}$ and fixed doping of $N_a=4\times10^{17}$ and $N_p=1.2\times10^{18}$ cm$^{-3}$ for $V_{GS}=0\,\text{V}=V_{GB}=V_{SB}$.

Figure 4.19. Surface potential vs. channel length of DHDMG for two different values of the $V_{DS}=0.1, 0.3\,\text{V}$ for $L=26$ and 36 nm and doping concentrations of $N_a=1.2\times10^{17}$ and $N_p=2\times10^{18}$ cm$^{-3}$ against the applied voltages $V_{GS}=0\,\text{V}=V_{GB}=V_{SB}$.

As is evident, the drain current is increased in SHDMG compared to a short-channel MOSFET (Figure 4.18). This is due to the increased electron velocity at the source end due to the halo implant and thus improved carrier transport efficiency of the DMG technology. The improvement is very prominent in the subthreshold regime, thus making
the device applicable for low-power subthreshold analogue circuits. For DHDMG, the improvement is more than SHDMG for obvious reasons. This potential model is further applied to compute the threshold voltage for DHDMG-MOSFET. It is seen that the roll-off in case of DHDMG starts from around 40 nm.

Figure 4.20. Threshold voltage vs. channel length plots of DHDMG, DG and short-channel MOSFET for substrate doping $N_a=6\times10^{17} \text{ cm}^{-3}$, $V_{DS}=0.5 \text{ V}$.

The DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off current. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes, this parasitic effect can be accounted for by a threshold voltage reduction, as shown in Figure 4.20. It is found that the DHDMG exhibits considerable suppression of the threshold voltage roll-off.
Figure 4.21 Comparison of subthreshold drain current versus gate bias of SHDMG and DHDMG MOSFETs for $L = 50$nm and 100nm with $V_{DS} = 1$V and fixed doping of $N_a = 4 \times 10^{17}$ and $N_p = 1.2 \times 10^{18}$ cm$^{-3}$ against the applied voltages $V_{GS} = 0$ V = $V_{GB} = V_{SB}$.

Figure 4.21 illustrates the increase in subthreshold drain current with increment in Halo implant doping.

Figure 4.22 Comparison of subthreshold drain current versus gate bias for DMG, SHDMG and DHDMG MOSFETs for $L = 50$nm and 100nm with $V_{DS} = 0.5$V and fixed doping of $N_a = 4 \times 10^{17}$ and $N_p = 1.2 \times 10^{18}$ cm$^{-3}$ against the applied voltages $V_{GS} = 0$ V = $V_{GB} = V_{SB}$.
Figure 4.23. Variation of DIBL coefficient with channel length for (Tsormpatzoglou et al. 2008) taking $t_{ox}=2$ nm and $t_{Si}=20$nm and DHDMG device taking $t_{ox}=2$ nm, keeping other parameters unchanged as Tsormpatzoglou et al. (2008).

It is seen from Figure 4.23 that the DIBL effect is reduced considerably in our model compared to Tsormpatzoglou et al. (2008) due to the introduction of the two halos along with DMG.

**Natural length:**

The natural length which characterises the SCE is given from Suzuki, Tanaka, Tosaka, Horie, and Arimoto (1993) and Sharma and Kumar (2008) as

$$\lambda = \sqrt{\frac{\varepsilon_{Si}t_{ox}X_j}{2\varepsilon_{ox}}}$$

(4.27)

A small natural length corresponds to superb SCE immunity. It is seen from Sharma and Kumar (2008) that when the ratio of the effective channel length to the natural channel length is greater than 2, then short-channel immunity is ensured. $\lambda$ for DHDMG is found taking $t_{ox}=3.5$ nm, $X_j=40$nm and $L=100$nm which are representative for a typical 130-nm device. Substituting these values $\lambda$ comes approximately 14.6 nm. So, the ratio becomes $100/14.6=6.8$. When $L=80$ nm, $\lambda$ for DHDMG is 11.7nm and the ratio is 6.84. For 40nm effective length, the ratio is 5. So, our model is very much immune to SCEs up to 40nm effective channel length. Below 40 nm, the quantum effects will predominate and our device performance will be degraded.
4.4 SUMMARY

An analytical surface potential model for ultra-thin oxide asymmetrically doped pocket implanted and symmetrically pocket implanted DMG MOSFET is developed by solving the pseudo-2D Poisson’s equation operating up to 40nm regime. The asymmetrically doped pocket implanted model is developed assuming two linear pocket profiles along the channel at the surface of the MOS device from the source and the drain edges. In this model, the varying depth of channel depletion layer is accounted for along with the inner fringing potential in the source and the drain ends. The well-known reverse SCE has been observed through the proposed model. The analytical models of surface potential and threshold voltages of the DHDMG and SHDMG are also derived and subthreshold I–V characteristics are examined. The novel device shows better performance with respect to the SCE than double gate or DMG. Based on the surface potential model, the drain current has been predicted by modifying the expression for channel conduction layer depth. Therefore, this model is very useful for circuit simulation and can be applied for analysing the MOSFET amplifiers where the device is operated in the subthreshold region.

References


