CHAPTER IV

p-n JUNCTION CAPACITANCE OF TRANSISTORS
4.1. Introduction

Junction space-charge capacitance is an important parameter in determining the high frequency performance of a transistor. In the transition region of a p-n junction there is a net local negative charge on the p-side of the junction due to ionized acceptors and a net local positive charge on the n-side due to ionized donors. These charges, within the temperature range of interest, are fixed, i.e., they are not free to move. These bound charges set up a potential difference across the junction even in the absence of any applied external voltage. Thus an effective capacitance is associated with a p-n junction and the transition region can be thought of as a parallel-plate capacitor. The width of the transition region is a nonlinear function of voltage across the junction, the exact law of variation being dependent upon the impurity distribution in that region. Thus different impurity distributions in the transition region of a junction result in different voltage dependence of capacitance.

Although capacitances of abrupt, graded and to some extent diffused p-n junctions were studied in details, the capacitance of certain newly developed diffused junctions showing widely different dependence on voltage had not been studied. It is the purpose of this chapter to present the results of such a study. But before we proceed to do so, we would make a brief review of the studies made so far on the capacitance of different types of junction. This is given in the first few sections while the studies made by the present author are reported in the last section of this chapter. In view of the fact that in a transistor, the collector-base junction capacitance is of greater importance than the emitter-base junction capacitance so far as high frequency performance is concerned we shall confine our attention to a study of the collector-base junction capacitance of transistors.
4.2. Capacitance of Abrupt and Graded p-n Junctions

Schottky [1939, 1942, (Summary by Joffe 1945)], in connection with dry solid rectifiers first developed the theory of abrupt p-n junction capacitance. With the publication of the Shockley (1949) theory of p-n junction, and the first successful fabrication of the alloyed-junction diode, the Schottky theory of p-n junction capacitance has been accepted. The capacitance $C_{tca}$ of an abrupt p-n junction according to this theory is given by

$$C_{tca} = A_c \left[ \frac{q \epsilon N_a N_d}{2(N_a + N_d)(\phi + V_c)} \right]^{1/2} \quad \ldots \quad (4.1)$$

where $A_c =$ area of the junction,
$q =$ electronic charge,
$\epsilon =$ dielectric constant of the material,
$N_a, N_d =$ acceptor and donor concentrations in p-type collector and n-type base sides of the junction,
$\phi =$ junction barrier potential, and
$V_c =$ applied collector-base voltage.

Generally, resistivity of the base region is much higher than the collector region in an alloy junction transistor so that $N_a \gg N_d$ and the depletion layer mostly penetrates into the base. For such cases, Eqn. (4.1) simplifies to

$$C_{tca} = A_c \left[ \frac{q \epsilon N_d}{2(\phi + V_c)} \right]^{1/2} \quad \ldots \quad (4.1a)$$
The above expressions for junction capacitance can be written as

\[ C_{\text{ca}} = K_a (\phi + V_c)^{-1/2} \]  \hspace{1cm} (4.2)

where \( K_a \) = a constant. From Eqn. (4.2) it is seen that junction capacitance varies inversely as the square root of applied voltage.

Several authors (Torrey and Whitmer 1948, Angello 1949) pointed out that there was only approximate agreement between theory and experiment of the capacitance-voltage characteristic of an abrupt p-n junction. This approximate agreement is considered (Rose and Spenke 1949) to be due to the quality of rectifiers and not due to approximations in the theory. Kroemer (1956) showed that in many practical cases some diffusion takes place at the junction so that the junction is not really abrupt. If the region of deviation from abruptness is narrow enough, it will lie entirely inside the depletion region, at least above a certain critical voltage \( V_a \). In case of such junctions, called 'pseudo-abrupt' junctions, Kroemer showed that the capacitance still follows an equation like (4.2) for \( V_a > V_a \), but \( \phi \) has to be replaced in Eqn. (4.2) by a quantity \( \phi^* \) which is no longer the true contact potential, but differs from it depending on the manner in which the transition from p to n takes place. Thus Eqn. (4.1) holds good so far as the voltage dependence of capacitance is concerned, although use of the same equation for determination of junction barrier potential might be objectionable.

Shockley's theory (1949) of p-n junction gives an expression for junction capacitance \( C_{\text{tg}} \) in the case of a linearly graded p-n junction, as
where \((N_a + N_d)/W\) is the slope of linear impurity grading. Eqn. (4.3) can be written as

\[
C_{tca} = A_c \left[ \frac{N_a + N_d}{W} \cdot \frac{q \varepsilon^2}{12(\phi + V_c)} \right]^{1/3} \quad \ldots \quad (4.5)
\]

Experiments on linearly graded p-n junctions showed that the relation (4.5) is generally true.

Recently Chang (1966) analysed the problem of space-charge density and capacitance of an abrupt p-n junction and solved the same in closed-form solution. His results of exact analysis neither agree with the Schottky theory nor with experimental results. He obtained an expression for the space-charge capacitance of the form

\[
C_{tca} = A_c \left[ \frac{q \varepsilon N_d}{2(\phi + V_c) + (2kT/q)\left(N_d/eN_a - 2\right)} \right]^{1/2} \quad \ldots \quad (4.5)
\]

where \(k = \) Boltzmann's constant,

\(T = \) Absolute temperature, and

\(e = \) Base of the Napierian logarithm.
The second term in the denominator on the right hand side of Eqn. (4,5) is lacking from the Schottky approximate solution. The magnitude of this term may be very large in asymmetrical p-n junctions, where $N_a$ can be orders of magnitude larger than $N_d$. For example, if $N_a/N_d = 10^4$, as is the case in a typical germanium alloy junction transistor, the applied voltage has to be as large as say about -95 volts so that the magnitude of the first term may be comparable with that of the second. Below this, the capacitance will not depend appreciably on voltage. Thus, Chang observed that the space-charge capacitance of asymmetrical junctions is nearly constant in negative bias condition.

Kleinknecht (1967) pointed out that the reason for Chang's apparently puzzling result lies in the evaluation of the charge on a plate of the capacitor, for which he included in an otherwise elegant calculation, not only donors and electrons but also holes in the integration of charge density. In asymmetric junctions, the contribution to space-charge by holes at the edge of the depletion layer on the n-side is considerable. Kleinknecht argued that on variation of the bias voltage, these holes do not flow in and out through the n-type side contact, but rather, through the contact on the p-type side. Consequently, they cannot be counted with the charge on the capacitor plate. This effect is, naturally, significant only if the asymmetry is large enough to make the hole density at the edge of the depletion layer larger than the donor density. By generally following Chang's approach, with simple but valid approximations, he showed that the Schottky formula for junction capacitance, except for the value of $\phi$, remains unchanged for an asymmetric junction.

4.3. Capacitance of Diffused p-n Junctions

The developments of "solid-state diffusion" (Biondi 1958), "epitaxial"
technique (Theuerer et al. 1960, Marinace et al. 1960, Siglar and Watelski 1961), and "planar" technology (Hoerni 1960) made available new types of transistors. The impurity distribution in the transition region of a diffused p-n junction is different from those of abrupt and linearly graded p-n junctions. Naturally, the voltage dependence of the capacitance of diffused p-n junctions is expected to be different from those of abrupt and linearly graded p-n junctions. Several authors (Kroemer 1956, Pritchard 1959, Lawrence and Warner 1960, Root 1960) have studied the capacitance-voltage characteristics of such junctions and shown that they behaved differently although for certain ranges of voltage linear graded junction and abrupt junction approximations could be applied. Kroemer conducted an investigation which provides an explanation for the observed characteristics. He assumed an arbitrary impurity distribution in the transition region. When the space-charge layer terminates upon a semiconductor of constant impurity concentration, the capacitance-voltage characteristic is shown to correspond to abrupt junction characteristic.

In the case of diffusion of an impurity into a semiconductor with the assumption of a concentration-independent diffusion coefficient and a constant volume-concentration at the surface, the solution of the one-dimensional diffusion equation shows (Barrer 1941) that the impurity distribution in the transition region is given by the complementary error function. For the case of impurity diffusion in which a fixed amount of the diffusant is deposited on the surface from which the diffusion proceeds, the solution of the one-dimensional diffusion equation shows that the impurity distribution in the transition region is given by the Gaussian function.
It appears that Lawrence and Warner (1960) first made a study of diffused p-n junctions considering both gaussian and complementary error function distribution of impurity in the transition region and showed graphically that for low applied voltage, such junctions behave as linearly graded junctions, the behaviour gradually changing to that of an abrupt junction at high voltage. They presented charts showing transition from graded to abrupt junction behaviour. The transition from graded to abrupt junction behaviour extends over about a decade of voltage when the depletion layer widens on both sides of the junction. For depletion layer widening on a single side of the junction, the transition extends over several decades of voltage.

Root (1960) independently analysed diffused p-n junctions with complementary error function distribution of impurity in the transition region and arrived at conclusions similar to Lawrence and Warner. Like Lawrence and Warner, Root demonstrated this change in junction capacitance behaviour graphically. He offered an explanation for the behaviour of diffused p-n junctions from his graphical data which indicates that initially the junction acts like a graded junction and at higher voltages, depletion layer widening on one side reaches the material of constant impurity concentration, while widening on the other side essentially ceases because of high concentration encountered. Thus at high voltage the diffused p-n junction behaves like an abrupt junction.

Several other authors (Kennedy and O'Brien 1961, 1962, Breitschwardt 1965) investigated different aspects of diffused p-n junctions, such as junction depth, impurity gradient, depletion layer width, impurity level, etc. at the junction for a variety of diffusion parameters and initial impurity concentration in the semiconductor material. But none offered any analytic expression showing the
4.4. Temperature Dependence of Capacitance

There is no marked temperature dependence of junction capacitance because the distribution of stationary ions does not depend on temperature. At a given voltage, Aukerman et al. (1965) observed a 4% lowering of capacitance value at 78°C relative to that at room temperature. This capacitance change has not been fully accounted for. The aforesaid authors showed that the temperature dependence of dielectric constant accounts for only about 1% per cent change in capacitance and dimensional change does not account for any variation of capacitance at all.

4.5. Anomalous Capacitance-voltage Characteristic of Collector-base Junction of Transistors

From the discussions in the preceding sections of this chapter, it is seen that for certain types of junctions such as alloy (step) and grown (linearly graded) junctions, exact theoretical expressions for such capacitances are known. In the case of diffused junctions, it has been seen that the junction behaviour can be approximated to that of a linearly graded junction at low voltage which gradually changes over to that of a step junction with increase in the voltage. But junction capacitance of different diffused junction transistors fabricated by modern techniques exhibit widely different dependence on voltage, e.g., junction capacitance has been experimentally found to vary inversely as the 10th or even higher root of reverse bias voltage. As the peculiar behaviour of capacitance of such junctions could not be explained with the help of the existing knowledge
about them, an attempt has been made here to provide a satisfactory explanation for the same.

In sub-section 4.5.1 capacitance-voltage characteristics and the different impurity distribution profiles in the space-charge region of the abovementioned junctions are examined in the light of a generalized expression for junction capacitance. This is followed in sub-section 4.5.8 where some plausible suggestions capable of explaining the observed capacitance-voltage characteristic satisfactorily, are put forward. The section concludes with a discussion in sub-section 4.5.3 on different suggestions put forward and their application in explaining different experimental results.

4.5.1. Generalized Expression for Junction Capacitance

Norwood and Shatz (1968) derived a general expression for junction capacitance from which any dependence of capacitance on voltage can be obtained. This is given by

$$ C_{tc} = A_{c} \left[ \frac{q B c^{(n+1)}}{(n+2)(\phi + V_{c})^{1/(n+2)}} \right] $$

In deducing Eqn. (4.6) they assumed a generalized impurity distribution in the space-charge layer of the form

$$ N = N_{a} - N_{d} = B X^{n} $$

and the boundary conditions were chosen as

$$ \begin{cases} \phi(0) = 0 \\ \phi(w) = \phi + V_{c} \end{cases} $$
Fig. 4.1. Typical impurity distributions predicted by Eqn. (4.7) for different values of $n$. 
Fig. 4.2. Typical impurity distributions around p-n junctions — (a) diffused junctions, (b) epitaxial diffused junction.
where \( B = N_0 \) (fig. 4.1) for \( n = 0 \),

\[ X = \text{normalized distance from the junction, and} \]

\[ \phi(x) = \text{potential at a distance } x \text{ from the junction.} \]

From Eqn. (4.6) it is easily seen that we can have any dependence of capacitance on voltage depending on the value of \( n \). The different impurity profiles for some typical values of \( n \) are illustrated in Fig. 4.1. Also, from Eqn. (4.6), we note that for capacitance varying inversely as higher roots (higher than the third root) of voltage \( n \) must be greater than 1.

Fig. 4.2(a) shows the impurity distribution around a diffused junction while Fig. 4.2(b) shows the distribution for an epitaxial diffused junction. In the case of both these types of junctions it has been suggested (Motorola 1963) that the depletion layer penetrates mostly into the collector. A comparison of impurity profiles of Fig. 4.2 with those of Fig. 4.1 shows that the distribution of impurity in the collector region corresponds to value of \( n \) lying between 0 and 1. Taking the mean value for \( n \), i.e., \( n = 0.5 \) the expression for junction capacitance \( C_{tcd} \) is given by

\[
C_{tcd} = K_d \left( \phi + V_c \right)^{-0.4} \quad \text{... (4.9)}
\]

where \( K_d \) is a constant. The voltage dependence of capacitance as given by Eqn. (4.9) is in agreement with that given in the literature. (General Electric Co. 1962, Lowen and Rediker 1960, Aukerman et al. 1965).

It may be noted in this connection that at low reverse bias voltage, the width of the depletion layer being small, the impurity distribution in the
layer would appear to be linear. Accordingly, \( n \) may be taken to be equal to 1 and the junction behaviour would approximate to the behaviour of a linearly graded junction. With increase in reverse bias the depletion layer widens resulting in a changed impurity distribution pattern across the junction. The value of \( n \) consequently change from 1 to a lower value and the junction capacitance behaviour is altered as shown by earlier workers (Lawrence and Warner 1960, Root 1960).

From the above discussion it is obvious that impurity distribution normally encountered in the collector region around a diffused junction as shown in Fig. 4.2(a) and 4.2(b) cannot explain any value of the exponent on the right hand side of Eqn. (4.6) less than 1/3. As already stated, however, there are junctions, in epitaxial transistors in particular, whose capacitance-voltage characteristics show (Motorola 1963) an inverse 10th root dependence of capacitance on reverse bias. In fact, experimental measurements in this laboratory indicated that the dependence may vary from near cube root to higher roots such as 14. In the following sub-sections, we shall consider some plausible suggestions for explaining such apparently unusual behaviour of junction capacitance with voltage.

4.5.2. Some Suggestions for Explaining the Aforesaid Apparently Unusual Variation of Capacitance with Voltage

It is clearly seen from Eqn. (4.6) that the apparently unusual dependence of capacitance on voltage as mentioned in the preceding sub-section would be expected with values of \( n > 1 \). For example, the 10th root dependence is expected with \( n = 8 \). From Figs. 4.2(a) and 4.2(b) it is interesting to note that the impurity distributions in the base region correspond to profiles having \( n > 1 \).
Fig. 4.3. Impurity distribution around an epitaxial diffused junction when impurities from the substrate do not diffuse into the epitaxial layer during the growth of the latter over the former, and the junction is formed close to the epitaxial-substrate interface.
Fig. 4.4. Impurity distribution around an epitaxial diffused junction when impurities from the substrate diffuse into the epitaxial layer during the growth of the latter over the former. Continuous and chain curves in the base depict respectively the Fickian and non-Fickian impurity diffusion into the epitaxial layer through the surface during the formation of junction.
Therefore, if we assume that the depletion layer in such types of junction penetrates into the base region, then the experimentally observed phenomenon of capacitance varying inversely as the 10th root or such other higher root of voltage can be explained.

The abovementioned assumption implies tacitly that the base material resistivity is much higher than the collector material resistivity around the junction so that depletion layer penetration occurs into the base region. A plausible situation in which such a possibility may arise is shown in Fig. 4.3 where the junction is formed close to the epitaxial-substrate interface. In such a case, base region resistivity around the junction would be much higher than the collector region resistivity and the depletion layer would in consequence mostly penetrate into the base region.

We shall now consider an alternative suggestion based on the premise that the depletion layer penetrates into the collector region. Thomas et al. (1962) has shown that diffusion of impurity into the epitaxial layer from the substrate during the growth of the former over the latter gives rise to a non-uniform impurity distribution in the epitaxial layer (with concentration decreasing towards the surface). When such an epitaxial layer is subjected to diffusion for the formation of junctions, the impurity distribution around the junction is as shown by the solid line curve in Fig. 4.4 (Breitschwardt 1965). From this curve it is evident that, except for a small region near the junction which may be reasonably approximated by the dotted curve, the impurity distribution in the collector region may be considered to correspond to a profile having $n > 1$. Thus, in the case of the abovementioned type of impurity distribution, any dependence of capacitance on voltage can be explained with an appropriate value of $n$, provided the depletion layer penetrates into the collector region.
Atalla and Tannenbaum (1960) showed that the impurity distribution in a semiconductor may undergo a redistribution in a region near the surface during the growth of an oxide layer over it. The extent of redistribution may range from pile-up to depletion depending on the segregation coefficient of the impurity at the semiconductor-oxide interface, diffusion coefficient of the impurity in both the semiconductor and the oxide and on the rate and time of oxidation. Thus the process of protective oxide layer formation in certain types of transistor might aid in causing the impurity distribution in the collector region to assume a profile corresponding to \( n > 1 \), and consequently, capacitance varying inversely proportional to higher roots of reverse bias voltage might result. High temperature operations, such as, 'vacuum bakeout' used in the manufacture of transistors, may also contribute to this process.

4.5.3. Discussions

Of the various suggestions put forward above for explaining the aforementioned capacitance-voltage characteristic of p-n junctions, the first one, viz., that the junction is formed close to the epitaxial-substrate interface and consequently the depletion layer penetrates into the base, seems to be less probable in view of the following facts. Firstly, this would result in a junction breakdown voltage considerably lower than the designed value and hence would reduce considerably the advantages of using epitaxial layer in transistor fabrication. Secondly, since the position of the junction below the surface can be accurately determined (Lawrence and Warner 1960, Thomas and Boothroyd 1966) the possibility of an error in junction position calculation is highly unlikely unless some other phenomena step in to cause the formation of the junction near the epitaxial-substrate interface.
Fig. 4.5. The diffusion profiles for Fickian (curve II) and non-Fickian (curve I) impurity diffusions.
Weisberg and Blanc (1963) has shown that when impurities diffusing through the surface to the epitaxial layer for junction formation exist in a substitutional-interstitial equilibrium, the diffusion coefficient becomes a function of concentration resulting in a diffusion profile that has a very sharp diffusion front as indicated in Fig. 4.5 (curve I). The usual distribution is shown by curve II in the same figure. Aukerman et al. (1965), however, argued that near the junction, the aforesaid profile was not quite valid and suggested that the concentration should decrease approximately linearly instead of dropping sharply. They attributed this variation to the facts that the substitutional diffusion coefficient and the charge carrier density near the junction were not equal to zero as assumed by Weisberg and Blanc in their analysis. In that event, the base impurity profile shown by solid line curve in Fig. 4.4 may undergo a modification and may take a shape as shown by the chain curve in the same figure.

If the impurities exist in a substitutional-interstitial equilibrium resulting in a non-Fician distribution, the junction depth would be less (Weisberg and Blanc 1963) compared to that calculated for a Fician distribution, making formation of junction near the epitaxial-substrate interface even more improbable. Also, the impurity profile for a non-Fician distribution corresponds to \( n < 1 \), and hence is incapable of explaining the observed capacitance-voltage characteristic.

It is thus seen that the mechanism mentioned in the second suggestion aided by impurity redistribution during protective oxide layer formation or subsequent high temperature operations or both, seems to be more plausible and capable of explaining the experimental results satisfactorily.
It may be mentioned here that the presence of an inversion layer on the surface of certain transistors is known (Lindmayer and Wrigley 1965) to give rise to unusually high values of junction capacitance and to show a nonlinear capacitance-voltage characteristic when plotted on a log-log graph paper. This is believed to be due to increased effective junction area as a result of inversion on the surface which gradually decreases with applied reverse bias voltage. At high reverse bias voltage, however, the inversion area is pinched off and the usual capacitance-voltage characteristic with normally expected capacitance value is observed. Our measurements on the transistors under investigation did not show any characteristic indicating the presence of an inversion layer on the surface.

Measurement of capacitance as a function of reverse bias voltage for different types of mesa and planar transistors showed different capacitance-voltage characteristics which indicated that the value of \( n \), in general, was different for different types although the fabrication technique was the same. An explanation for this difference may be obtained by referring to Fig. 1 which shows that for higher values of \( n \), the different impurity profiles are rather closely spaced so that the variation in the value of \( n \) may well be due to spread in the production-controlled parameters (Breitschwardt 1965). Also, different transistors of the same type showed different values of \( n \) which might be attributed either to the above factor or to the presence of defects (lattice) (Horak 1969) in the semiconductor or to both.