Chapter 5

Deposition and Characterization of La$_2$O$_3$ gate dielectric p-GaAs

5.1 Introduction and Motivations for using La$_2$O$_3$ as high-k dielectric

In making a choice among so many high-k materials; a sufficiently high dielectric constant, large band-gap, both conduction and valence band offset from substrate and thermodynamic stability are the key requirements for gate insulator application. To perform a low EOT, high-k gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Compared to other high-k materials, Lanthanum oxide (La$_2$O$_3$) is electrically hopeful for the gate insulator of the future MOSFET. La$_2$O$_3$ has the largest band gap of the rare earth oxides at $E_g > 5$ eV, while also having the lowest lattice energy, with very high dielectric constant, $K = 27$ [1, 2]. In addition symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon. La$_2$O$_3$ has a high melting point of about 2588 K, which usually indicates less self-diffusivity and high stability. The density of La$_2$O$_3$ is also very high (6.51 g/cm$^3$), which is good enough to prevent diffusion through the oxide. Because of the expected high temperature excursion during CMOS processing thermodynamic stability against silicon is of primary consideration. From the evaluation of the available solid-state thermodynamics data it can be concluded that La$_2$O$_3$ is stable in contact with silicon at 1000 K. However, this stability is expected under
equilibrium conditions [3]. The exact phase diagram of the lanthanum - oxygen system is not known. The cubic structure of La\(_2\)O\(_3\) is shown in figure 5.1. A tentative to calculate the La-O phase diagram has been published by Grundy et. al. [4]. In general, the lanthanum oxide exists in several modifications depending on the temperature. The crystallographic data are given in Table 5.1 [5]. The only stable polymorphic form La\(_2\)O\(_3\) at room temperature is \(\alpha\)-type. In a mixture with lanthanum metal the equilibrium composition of the lanthanum oxide is sub-stoichiometric, an effect that is due to the formation of oxygen vacancy. The major drawback of lanthanum oxide, as all others rare earth metal oxide, is its high sensibility to humidity. Moisture adsorption leads to film degradation and solutions to this problem have to be found when La\(_2\)O\(_3\) is to be used as gate dielectric.

Table 5-1: Crystal structure for La-O system after [5].

<table>
<thead>
<tr>
<th>Phase</th>
<th>T [K]</th>
<th>Structure</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\alpha)-La(_2)O(_3)</td>
<td>&lt; 823</td>
<td>cub</td>
<td>Mn(_2)O(_3)</td>
</tr>
<tr>
<td>(\beta)- La(_2)O(_3)</td>
<td>823-2273</td>
<td>hex</td>
<td>La(_2)O(_3)</td>
</tr>
<tr>
<td>(\gamma)- La(_2)O(_3)</td>
<td>2273-2373</td>
<td>hex</td>
<td>(?)</td>
</tr>
<tr>
<td>(\delta)- La(_2)O(_3)</td>
<td>&gt; 2373</td>
<td>cub</td>
<td>La(_2)O(_3)</td>
</tr>
</tbody>
</table>

As it can be seen, the present status of La\(_2\)O\(_3\) still presents some serious issues before its implementation as the gate oxide for next-generation transistors. However, and because of the good results having obtained so far, La\(_2\)O\(_3\) is being considered as a possible candidate not only for the replacement of SiO\(_2\) but also for HfO\(_2\)-based materials since Hf-based high-k materials are surpassed by La\(_2\)O\(_3\) in terms of ultra-low leakage current density levels for the smallest EOT ever obtained. Moreover, lanthanum oxide (La\(_2\)O\(_3\)) offers high quality surface passivation of Ge with low interface state density [6-8]. Formation of stable La-O-
Si/Ge interface layers has been reported for Si/Ge combination with rare earth high-k dielectrics [9-11]. The La$_2$O$_3$ has been studied mainly for Si- and Ge-based devices while there is considerably less work related to the properties of La$_2$O$_3$ deposited on GaAs substrates [12-14].

In the Chapter, we have studied a systematic investigation of the dielectric quality of La$_2$O$_3$ and its interface properties with and without Si passivated p-GaAs in detail as a function of subsequent post deposition annealing (PDA) conditions. The film composition and interfacial microstructure are investigated by using x-ray photoelectron spectroscopy (XPS), secondary ion-mass spectroscopy (SIMS), high-resolution transmission electron microscope (HRTEM), and electrical measurements.

![Figure 5.1: Crystal structure of La$_2$O$_3$.](image)

**5.2. Experimental**

Metal-oxide-semiconductor (MOS) capacitors were fabricated on Zn doped p-GaAs (100) with a carrier density of $\sim 1 \times 10^{16}$ cm$^{-3}$. The wafers were degreased using isopropanol; the surface native oxides were removed by diluted 10% HCl etching for 3 min, and dipped in NH$_4$OH for 5 min to remove elemental As.
La$_2$O$_3$ dielectric layer was deposited at room temperature by RF sputter deposition using La$_2$O$_3$ target and 80 W RF power in an Ar ambient at 3 mTorr working pressure. For some wafers, a thin layer of Si IPL was deposited by sputtering using Si target and 100 W RF power, prior to La$_2$O$_3$ deposition. Post deposition annealing (PDA) was carried out in N$_2$ ambient at three different temperatures (400 °C, 500 °C and 600 °C) for 1 min by rapid thermal annealing (RTA). The gate dielectric and interfacial layer thicknesses were determined using a high resolution transmission electron microscope (HRTEM), model JEOL 2100 operating at 200 kV. For comparison, we have annealed the La$_2$O$_3$/GaAs
structures only at 500 °C. The high-resolution x-ray photoelectron spectroscopy (XPS) measurements were performed under a UHV condition at room temperature with VG ESCALAB 220i-XL XPS system. The take-off-angle was 90° using monochromatic AlKα (1486.7 eV) excitation sources through collecting spectra in constant pass energy (20 eV) mode of the analyzer for data acquisitions with a spot size of 700 µm and a energy step of 0.1 eV. Thermally evaporated Al was used as the top gate electrode (area: 2×10⁻³ cm²). Low resistance ohmic back contact was made by using Ti/Pt/Au alloying on the back side of the wafers. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using an Agilent B1500A semiconductor device parameter analyzer.

**5.3 Physical Characteristics**

**5.3.1 X-ray photoelectron spectroscopy analysis**

High-resolution x-ray photoelectron spectroscopy (XPS) measurements were performed under a UHV condition at room temperature with VG ESCALAB 220i-XL XPS system. The take-off-angle was 90° using monochromatic AlKα (1486.7 eV) excitation sources through collecting spectra in constant pass energy (20 eV) mode of the analyzer for data acquisitions with a spot size of 700 µm and a energy step of 0.1 eV. The high resolution spectra of La 3d, Si 2p, O 1s, As 3d and Ga 3d were baseline corrected using Shirley backgrounds and deconvoluted using Gaussian-Lorentzian (G-L) functions.

Figure 5.3(a) shows O 1s core level spectra of La₂O₃/GaAs and La₂O₃/Si/GaAs gate dielectric stack at the surface. In the O 1s spectra, La-OH binding peak is located at a higher binding energy (533.1 eV) in the La₂O₃/GaAs sample at the surface, with a peak shift of +2.7 eV relative to La₂O₃ (531.2 eV). This corresponds to La-hydroxide formed during the air-exposure of La₂O₃ film.
[15]. The intensity of La-OH peak decreases after introducing Si passivation layer (La2O3/Si/GaAs gate stack), which suggests that the Si IPL prevents the formation of La-hydroxide. The peak at ~532.5 eV associates with the bonding of La-O-Si in La2O3/Si/GaAs stack after introducing Si passivation layer.

In Figure 5.3(a) La-O-Si peaks do not show any noticeable difference for samples annealed at 400 °C and 500 °C, indicating that the interface has not changed very
much. In Figure 5.3 (b) it was observed that the La 3d$_{5/2}$ peak found from the surface of La$_2$O$_3$ at 834.6 eV, which is close to the energy position of the surface La-oxide peak reported earlier [16]. Interlayer growth and Si out diffusion in the La$_2$O$_3$ films after annealing in N$_2$ ambient were examined using the Si 2p core level for the La$_2$O$_3$/Si/GaAs structures shown in Figure 5.3(c). The spectral region of La 4d and Si 2p was found overlapped and decomposed into Si 2p (La-silicate) and La 4d (La-silicate and satellite). The La 4d peak of La$_2$O$_3$ could be assigned to a substantial La-O-Si bond at 103.2 eV and Si-O-La at 101.1 eV. These results reveal that the interlayer has the composition of (La$_2$O$_3$)$_{1-x}$(SiO$_2$)$_x$ (LSO). At the same time, the LSO film minimizes the formation of surface hydroxide.

Out diffusion of As in the high-k dielectric along with the formation of As-O and Ga-O at the high-k/GaAs interface is a critical issue. Figure 5.4(a) shows the core level XPS spectra of Ga 3d after La$_2$O$_3$ deposition with and without Si interlayer passivated p-GaAs substrates. The Ga 3d XPS spectrum can be fitted into two Gaussian peaks located at 19.1 and 20.3 eV are mainly due to Ga-As and Ga-O bonds corresponds to the Ga-As substrate and Ga-O from interlayer at 20.3 eV for Ga$^{+1}$ (Ga$_2$O). The presence of significant gallium oxide is observed for samples without Si passivated GaAs surface. However, for the Si passivated samples, the growth of Ga$_2$O interfacial layers are significantly reduced, as shown in Figure 5.4(a). The results imply that the growth of interfacial Ga$_2$O layer was effectively controlled after Si passivation and similar results of high-k on Si-passivated GaAs substrates have been reported [17, 18]. The spectral region of Ga 3d is overlapped with La 5p and the hydroxide (at 17.5 eV) formed by La was observed only for samples without the Si passivation layer. The absence of any La-OH bond for Si passivated samples confirmed that the incorporation of a Si layer prevented hydroxide formation [19]. The contribution at 18 eV corresponding to the La-O-Si bonds is observed with the Ga-As peak under both
N$_2$ annealing conditions. These results are based on the fact that La in La-O-(Si) would be more ionic than La-O and Si in Si-O-(La) would be more covalent than Si-O [20].

Figure 5.4: XPS (a) Ga 3d and (b) As 3d spectra of La$_2$O$_3$ gate stack deposited on p-GaAs without Si IPL annealed at 500 °C and with Si IPL annealed at 400°C and 500 °C for 1 min in N$_2$ ambient.

Figure 5.4(b) shows the As 3d spectra for thin La$_2$O$_3$ films deposited on p-GaAs substrates with and without Si IPL. The As 3d spectra were fitted with contribution from As-Ga and As-O indicates that the sample is selectively oxidized during deposition. The substrate peak is fitted with As 3d$_{5/2}$ and As 3d$_{3/2}$ spin orbit peaks with a separation of ~0.7 eV [21]. The As-O peaks are fitted with mainly two peaks at a higher binding energy of ~43.6 eV and ~45 eV as shown in Figure 5.4. These two peaks are shifted from As$^0$ with +3.0 eV and +4.1
eV can be attributed to As$^{3+}$ (As$_2$O$_3$) and As$^{5+}$ (As$_2$O$_5$) [22]. In addition, the La-O (La 5s) peak was also present at a binding energy of -5.1 eV with respect to the As 3d$_{5/2}$ peak. Comparing the As-O state it is noted that large amounts of arsenic oxide with both As$^{3+}$ and As$^{5+}$ state present for samples without the Si passivated p-GaAs surface. The intensity of As$^{3+}$ peaks decreases significantly after Si passivation. It was also observed that for Si passivated samples after high temperature N$_2$ annealing, the As$^{5+}$ component is reduced while the As$^{3+}$ component at 43.6 eV is increased. Although, interfacial arsenic oxide is present, the ratio of As$^{5+}$/As$^{3+}$ oxidation states clearly reduced after annealing at 500 °C as shown in Figure 5.4(b).

Figure 5.5: O 1s photoelectron spectrum measured from La$_2$O$_3$/GaAs and La$_2$O$_3$/Si/GaAs structures under different PDA temperature.

We have measured the band gaps for both La$_2$O$_3$/GaAs and La$_2$O$_3$/Si/GaAs gate stacks within the error limit of ~0.05 eV. The band gap was
determined to be ~5.6±0.05 eV for La$_2$O$_3$ and 5.5-5.9 eV for La$_2$O$_3$/Si/GaAs system. O 1s photoelectron energy loss spectra of La$_2$O$_3$/GaAs and La$_2$O$_3$/Si/GaAs gate stacks are shown in Figure 5.5. In the spectra, the onset of band-to-band excitation which corresponds to band gap is defined as an intercept of linear extrapolation of leading edge to background level [23].

The interface diffusion (or reaction) after the post deposition annealing at RTA temperature 500 °C was also investigated from Ga 2p, La 4d, and Si 2p signal as shown in Figures 5.6(a), (b), (c) at different sputtering condition (60-120 sec Ar$^+$ sputter).

From the Ga 2p XPS spectra, it was observed that after sputter the La-O (La 4d) peak increases which imply the increased bond strength of La-O at the interface which could be due to the formation of LSO. Again from the La 4d and Si 2p spectra, it was confirmed that LSO film was formed at the interface. The medium intensity of La-O after 60 s sputter is from silicate with high La concentration (high La-silicate with higher crystalinity), whereas, the higher intensity in IL are assigned as La-silicate with low La concentration (low La-
silicate) [24]. It indicates the presence of a lower La-silicate layer at the interface which is due to the intermixing of Ga and As with the LSO film. Thus, it can be concluded that the IL is mainly composed of La-O-Si with Ga/As originate from the La-rich silicate due to the interface reaction. Si 2p spectra indicate no trace of unoxidized Si in the dielectric stack after post deposition annealing at 500 °C.

5.3.2 HRTEM and depth chemical analysis with ToF SIMS
The ToF-SIMS technique is highly surface sensitive and gives information from the upper layers to the in depth interface structures of the gate stacks. The profiles of Ga, LaO, La, As, O and Si ions are shown in Figure 5.7.

![ToF-SIMS profiles](image)

Figure 5.7: ToF-SIMS profiles of (a) La₂O₃/GaAs, and (b) La₂O₃/Si /GaAs structures under PDA at 500 °C.

The chemical species that present in the La₂O₃ films on the GaAs substrates without Si passivation layer and with Si passivation layer are shown in Figures 5.7 (a) and (b), respectively. The ToF-SIMS analysis provides strong evidence that
incorporation of a Si interfacial layer on GaAs substrates improves the interface stability at La₂O₃/GaAs interface. In addition, the amount of incorporated Ga and As into La₂O₃ films was reduced approximately by one order after introducing the Si IPL, which is consistent with the results obtained from XPS analysis. Slow decay/nearly constant of the signals for O, La and La-O up to the interface indicates almost homogeneous distribution of the La₂O₃ films. Increasing intensity of La along with the Si interfacial layer as shown in Figure 5.7, strongly suggests the formation of La-O-Si at the interface. Formation of La-O-Si was also found in XPS analysis. From the SIMS and XPS analyses, it appears that the sub-oxides of La and Si co-exist with native oxide of GaAs at the interface layer.

To investigate the interfacial layer thickness and more in depth analyses, the cross-sectional HRTEM analysis along with the XPS at different depth of the dielectric stack was carried out to study the thickness of interfacial lanthanum silicate (LSO) films and the interfacial reaction between the LSO film and GaAs substrate. Figure 5.8 shows the effects of the post annealing on the interfacial structure of the La₂O₃/LSO/GaAs structures. The total thickness of the dielectric stack was ~15.2 nm along with the thick LSO film of ~8 nm. This thick LSO film is formed during the post deposition annealing. This high tendency to form the lanthanum silicate, Liang et al. have derived a relationship for the enthalpy \( \Delta H_f = -100.8 + 16.8(z/r) \), where \( z/r \) is the ionic potential, \( z \) is the ionic charge, and \( r \) is the ionic radius in Å. This gives \( \Delta H_f = -59.5 \text{ kJ/mole} \) for the formation of lanthanum silicate [25]. From this calculation, they have concluded that La₂O₃ is very reactive with the underlying Si or SiO₂. We have combined the TEM and SIMS analysis for the La₂O₃/LSO/GaAs structure as shown in Figure 5.8. From the TEM results, it is confirmed that the LSO film has two different chemical compositions and also differently crystallized lanthanum silicate layer. From the
contrast of the film, it is seen that LSO film close to the GaAs substrate is more amorphous lanthanum silicate than the LSO film near the La$_2$O$_3$ layer [26, 27].

Figure 5.8: Combination of HRTEM and SIMS profile of La$_2$O$_3$/LSO/GaAs structures under PDA at 500 °C.

5.3.3 Atomic Force Microscope Analysis

AFM have been proved to be very powerful for the observation of topography and growth mechanism of thin solid films. The AFM used was a Nanoscope III from Digital Instruments (Veeco) system operating in tapping mode and using Nanosensors force modulation probes with pyramidal silicon tips. These probes
have a typical resonance frequency of 325 kHz and force constant of 40 N/m. The scanning area size is 5 μm × 5 μm.

Figure 5.9 shows a three-dimensional AFM image of microwave plasma deposited ultra-thin La₂O₃ films on p-GaAs with different PDA annealing. The results indicate that the ALD La₂O₃ film has excellent uniformity. From this image it is clear that thin La₂O₃ film is well deposited throughout the surface and the as-deposited film is amorphous in nature. Typical measures of surface micro-roughness are the arithmetic mean deviation (Ra) and root mean square deviation (RMS) of a specified area of the surface. These quantities are defined as, 

\[ R_a = \frac{1}{N} \sum_{i=1}^{N} |Z_i - \overline{Z}| \] and 

\[ RMS = \sqrt{\left(\frac{1}{N}\right) \sum_{i=1}^{N} (Z_i - \overline{Z})^2} \]

where \( Z_i \) is the height at the i-th sampling point \((x, y)\), \( N \) is the no of data points and \( \overline{Z} \) is the average of \( Z_i \) i.e. \( \overline{Z} = \frac{1}{N} \sum_{i=1}^{N} Z_i \).

The arithmetic mean deviation (Ra) was found to be 2.56 nm for La₂O₃ directly deposited on p- GaAs. Whereas values were 1.95 nm, 1.69 nm, 1.21 nm and 1.34 nm respectively for Asdeposited, PDA at 400 °C and 500 °C and 600 °C sample of La₂O₃/Si/GaAs structure. On the other hand the root mean square deviation (RMS) of a specified area of the surface was found to be 3.05 nm for La₂O₃ directly deposited on p- GaAs. Whereas values were 2.54 nm, 2.21 nm, 1.89 nm and 1.93 nm respectively for Asdeposited, PDA at 400 °C and 500 °C and 600 °C sample of La₂O₃/Si/GaAs structure. The AFM results suggest that the extremely low RMS value La₂O₃ films present clear crystalline orientation. The superior surface uniformity can have very excellent performance in devices for reducing the carrier scattering, decreasing the hanging bonds and density of the interface.
Figure 5.9: 3-D AFM images of La$_2$O$_3$ layers with and with Si IPL layer and annealed at different temperatures. (a)La$_2$O$_3$/P-GaAs, PDA at 500 °C, (b) As-deposited, (c) PDA at 400 °C, (d) PDA at 500 °C, (e) PDA at 600 °C, for La2O3/Si/GaAs gate stack. The size of all images is 0.5 × 0.5 μm$^2$. 
5.4. Electrical Characteristics

5.4.1 La$_2$O$_3$/Si/GaAs interface analysis

Figure 5.10(a) shows the high-frequency (100 kHz) capacitance-voltage (C-V) characteristics of Al/La$_2$O$_3$/p-GaAs after PDA at 500 °C and Al/La$_2$O$_3$/Si/p-GaAs MOS capacitors after post deposition annealing (PDA) at 400 °C, 500 °C and 600 °C. Improved C-V curve with saturated accumulation capacitance is observed for the La$_2$O$_3$/Si gate stack after PDA treatment compared to directly deposited La$_2$O$_3$ on p-GaAs, indicating the better interface quality. The La$_2$O$_3$/Si gate stack capacitor shows higher accumulation capacitance density ($C_{acc}$) of ~4.4 fF/um$^2$ compared to the directly deposited La$_2$O$_3$ capacitor (~3.6 fF/um$^2$) on p-GaAs, indicates that the thin layer of Si on p-GaAs effectively decreases the Ga and As oxides and suppresses the low-k interfacial layer growth, and leads to increase accumulation capacitance, which is similar to the other high-k/Si/GaAs stacks [28, 29]. The equivalent oxide thickness (EOT) was extracted by fitting the C-V characteristics with the simulated C-V curve that accounts for quantum mechanical effects. The values of EOT are 3.9 nm and 4.8 nm for La$_2$O$_3$/Si/GaAs (for as-deposited samples) and La$_2$O$_3$/GaAs gate stacks, respectively. C-V characteristics of Al/La$_2$O$_3$/Si/p-GaAs MOS structures for different PDA temperatures of 400 °C, 500 °C, and 600 °C, show that small change in accumulation capacitance ($C_{ox}$), which is associated with the EOT, depends on the PDA temperature. With the increased annealing temperature, the EOT values decreased to 3.7 nm (for 400 °C) and 3.4 nm (for 500 °C annealing), respectively, but EOT slightly increased to 3.6 nm for sample annealed at 600 °C. This may be due to degradation of the interface at higher annealing temperature and resulted in decreased accumulation capacitance (i.e, increase in EOT) [30]. For directly deposited La$_2$O$_3$ on p-GaAs the stretch-out ($\Delta C/\Delta V$) behavior of the C-V curves along the voltage axis indicates higher interface trap density ($D_{it}$). It is observed
that the Si passivation reduced the $D_{it}$ and samples annealed at 500 °C exhibit minimum stretch-out effect. There is slight increased in stretch-out effect and decreased in accumulation capacitance of C-V characteristics as observed for the sample annealed at 600 °C. This is most likely due to the oxidation of Ga at higher annealing temperature [31]. Significant reduction in flatband voltage ($V_{fb}$~0.5 V) was found for Si passivated samples under 500 °C PDA condition.

Figure 5.10(b) shows the frequency dispersions, evaluated as $\Delta C_{ox}$ and $\Delta V_{fb}$ (flatband voltage differences between 1 MHz and 50 kHz) for 500 °C PDA La$_2$O$_3$/Si gate stacks. Frequency dispersion characteristics for devices with and without Si IPL as a function of PDA temperature are shown in inset of Figure 5.10(b).

In contrast to the devices without IPL which exhibited frequency dispersion of higher than 25% and 800 mV, MOS capacitors with Si IPLs have shown much improved frequency dispersion (~11% and 430 mV). This indicates that GaAs
surface is effectively passivated by thin Si IPL and prevents Fermi level pinning at the interface. With higher PDA temperature, low frequency dispersion can be obtained. Samples annealed at 500 °C exhibit minimum values in both ΔC_{ox} (7.2%) and ΔmV (230 mV). This is due to complete oxidation of the Si IPL layer which reduced the charge trapping due to reduced thickness of highly trapped unoxidized Si layer [32]. The dispersion in accumulation and flat-band is comparable and/or lower than the reported values of ΔC_{ox} and ΔmV for HfO₂ and Al₂O₃ [17, 33]. It is worth to note that, generally, Hf-based dielectric on Si-passivated GaAs, the arsenic oxide remove after high temperature annealing, however, for La₂O₃/Si/p-GaAs gate stacks, there is significant amount of arsenic oxide present even after annealing at 500 °C and the frequency dispersion as well as hysteresis voltage is minimum. This is surprising as arsenic oxide generally considered one of the major elements to introduce defects traps at interface. In the present work, as we observed there is a presence of La-O-Si at interface, which possible make interface oxide layer more stable. As a result, the interfacial properties and electrical properties of the sputtered deposited La₂O₃ on Si-passivated p-GaAs show low interface state density, frequency dispersion and hysteresis voltage. The amount of out-diffused elemental As and Ga reduced significantly after introduction of Si passivation layer, which possible improved the electrical properties of La₂O₃ films.

Figure 5.11 shows the summary of the PDA temperature dependence of the midgap D_{it} (inset) and hysteresis voltage of different samples. Hysteresis is believed to be due to the presence of interfacial electrons and/or mobile charge in the oxide. Hysteresis widths of samples with and without IPL are approximately 0.4 V and 0.8 V, respectively. For Si passivated samples, the hysteresis voltage improved after annealing at 500 °C and exhibited a minimum value of 260 mV. The effective border trap density N_{bt} was calculated by
integrating the absolute value of the difference between the forward and reverse curves by the equation [34]:

$$\Delta N_{bt} \approx \frac{1}{qA} \int ((C_{\text{inverse}} - C_{\text{forward}})) dV \quad (5.1)$$

The change of $N_{bt}$ with different annealing temperature rather than only the hysteresis plot was shown in Figure 8. The decrease of hysteresis voltage is consistent with border trap density ($N_{bt}$). The calculated value of $N_{bt}$ from hysteresis width for the directly deposited La$_2$O$_3$ on p-GaAs is $1.8 \times 10^{11}$ cm$^{-2}$; however, the value decreased to $7.32 \times 10^{10}$ cm$^{-2}$ for samples annealed at 500 °C.

![Graph showing variation of hysteresis voltage and border traps density with different PDA temperatures and interface trap density (Dit) variation throughout the trap energy level to valance band of GaAs for various PDA temperature.](image)

Figure 5.11: Variation of hysteresis voltage and border traps density with different PDA temperatures and (inset) interface trap density (Dit) variation throughout the trap energy level to valance band of GaAs for various PDA temperature.

The hysteresis voltage improved after annealing at 500 °C and exhibits a minimum value of 260 mV. This result reflects the smaller density of slow border traps that reside close to the dielectric interface after N$_2$ annealing. The decrease of hysteresis voltage is consistent with border trap density ($N_{bt}$). The value of $N_{bt}$ for the directly deposited La$_2$O$_3$ on p-GaAs is $1.8 \times 10^{11}$ cm$^{-2}$; however, the value decreased to $7.32 \times 10^{10}$ cm$^{-2}$ for samples annealed at 500 °C.
The interface trap density \( D_{it} \) reduction was evaluated by using the technique proposed by Terman [35]. The interface trap densities close to the mid-gap are approximately \( 1 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2} \) and \( 1.2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2} \) for \( \text{La}_2\text{O}_3 \) directly deposited on GaAs and Si passivated-GaAs, respectively. A thin layer of Si suppresses the amounts of unstable As-As and As-O species, which are believed to be a source of high-density interfacial traps. Moreover, presence of La-O-Si at the interface makes interfacial native oxide more stable, as confirmed by the XPS analysis in the previous section. Subsequent increase in \( D_{it} \) after PDA at 600 °C implies that the degradation of the interface quality is probably due to the out-diffusion of elemental Ga and As into the \( \text{La}_2\text{O}_3 \) films from GaAs substrates [36].

To extract the extremely slow traps near the midgap which have very low characteristic trapping frequencies for both electrons and holes is very difficult for higher bandgap materials like GaAs. As a consequence, these states cannot be probed within the usual frequency range of 100 Hz - 1 MHz. An alternative method to evaluate the density of midgap states in GaAs is to thermally activate them at elevated temperature. Heated semiconductor will strongly increase the characteristic emission frequencies. In elevated temperature, it has been shown the possibility to access interface defects over an increased portion of the semiconductor energy gap and assesses their effect on the C-V characteristics [37]. The average percentage capacitance dispersions per 25 °C step of the temperature at \( V_{\text{gate}}=4 \text{ V} \) is 16.5%.

The high temperature C-V characteristics in Figure 5.12 indicate the appearance of large bumps in depletion at the elevated temperature, which are created by interface states near the midgap. The positive flatband shift, also representing the generation of large amount of negative traps, may be attributed to dangling bond sites in interface. For non-passivated samples, the flatband voltage shift is very high and after 150 °C, the C-V nature is lost. This is due to the
large amount of trap generation in the interfacial layer containing As-O and Ga-O related oxides. The thermionic emission of trapped charges during measurements above the room temperature is therefore expected to produce C-V characteristics shifts towards the positive voltage. Inversion generation can also be recognized, especially at higher temperature, where the tendency of rise in inversion capacitance due to minority carrier generation.

Figure 5.12: 100 kHz C-V response with varying temperature (RT to 200 °C) of La$_2$O$_3$/Si gate stacks under PDA at 500 °C. The average percentage capacitance dispersions per 25 °C step of the temperature at V$_{gate}$= 4 V is 16.5%.

Figure 5.13 (a) compares the current density-voltage (J-V) characteristics of La$_2$O$_3$/p-GaAs MOS capacitors with and without Si IPL vs. PDA temperature. High gate leakage current density of the order of $4.3\times10^{-3}$ A cm$^{-2}$ is observed at $V_{fb}$-1 V for the sample without passivation; likely due to interface trap assisted tunneling or interfacial oxides induced lowering of conduction band offset between high-k dielectric and GaAs [38]. However, for the La$_2$O$_3$/Si gate stack, the current density is $1.2\times10^{-5}$ A cm$^{-2}$ at a gate voltage of $V_{fb}$-1 V. These results show two orders of lower leakage current compared to directly deposited La$_2$O$_3$ on p-GaAs substrates. However, the current density increases after annealing at
600 °C as well as decrease of the accumulation capacitance at higher negative bias, as shown in Figure 5.10.

Figure 5.13: (a) Leakage current density vs. voltage characteristics of La$_2$O$_3$ and La$_2$O$_3$/Si gate stacks on p-GaAs as a function of various PDA temperatures (b) current density at $V_{fb}$-1 V vs. EOT. For comparison, reported data on high-k/Si and SiO$_2$/Si are also plotted together.

This can be attributed to the growth of Ga$_2$O$_3$ as evident from the XPS analyses shown in Figure 5.3 and 5.4. It is worthy to note that as the tunneling current is determined by the physical thickness of the dielectric and the change of the physical thickness is also reflected in the change of EOT, the results in Figure 5.13(b) confirms that an interfacial layer grows during the PDA and the interfacial layer thickness is strongly dependent on the PDA temperature. Increase of PDA temperature also increases EOT. Figure 5.13(b) shows the gate leakage current density at $V_{fb}$-1 V against EOT. The result shows that even though high-k on GaAs is leakier than high-k on Si, it can achieve a comparable or lower leakage current than SiO$_2$ on Si. Our results are similar to previously reported results [36, 39]. Among all the samples, 500 °C annealed samples exhibit
the lowest leakage current for the same EOT. Therefore, for the scaled devices which require a lower EOT, the PDA temperature must be kept as low as possible.

### 5.4.2 Charge trapping analysis

Leakage current and capacitance-voltage characteristics were monitored to study the stress induced charge trapping/generation in the La$_2$O$_3$/Si gate dielectric stack, after every 100s constant voltage stressing (CVS) at ±4 V. Figure 5.14(a) shows the charge trapping induced flatband voltage shift after positive gate bias stressing (4 V) as a function of stress time. According to the same dc positive effective electric field stress on Al/La$_2$O$_3$/Si/p-GaAs the devices with different PDA temperature. It is clear that the flatband voltage increases in the positive direction after positive gate bias stress due to the trapping of negative charges (electrons) at the interfaces and bulk of La$_2$O$_3$ layers. The samples that underwent subsequent N$_2$ annealing possess superior dielectric reliability, relative to that of as-deposited samples, with small increase in flatband shift with the increase in PDA temperature. It should be noted that, the differences in $V_{fb}$ originate from the trapping at the interfaces since the samples have the same thickness of La$_2$O$_3$/Si gate stack, producing different types of interfaces with different annealing temperature. With the increase in PDA temperature, significant reduction in trapping was observed up to annealing in 500 °C. However, the interface degraded for annealing at 600 °C due to the generation of surface pits or holes within the GaAs substrate thus increasing the surface roughness [40].
Figure 5.14: The charge trapping induced flatband voltage ($\Delta V_{fb}$) shift of different annealed sample as a function of stress time under CVS at ±4 V.

Figure 5.14(b) illustrates that the flatband voltage shift toward negative gate voltage with stress time after negative gate bias stressing (-4 V), indicating positive charge generation. Compared to positive bias stress, the trend is similar except that the shift is not as large, indicating less trapping of positive charges or less detrapping of pre-existing negative charges. Irrespective of the dielectric stress method employed (substrate hole or electron injection); it was found that the PDA improves the dielectric reliability. These findings indicate that the annealing environment is a crucial factor in determining the electrical performance of high-k/GaAs MOS capacitor structures.
5.5 Summary

In summary, interfacial and electrical characteristics of Al/La$_2$O$_3$/Si/p-GaAs MOS capacitors under various PDA conditions have been presented. The XPS and ToF-SIMS results imply the growth of thermally stable interfacial layer of Ga- and As-oxides for the La$_2$O$_3$/Si/p-GaAs gate stacks. The effective band gap for La$_2$O$_3$/Si/p-GaAs (5.5-5.9 eV) gate stack was higher than La$_2$O$_3$/p-GaAs (5.6±0.05 eV) gate stack. Using optimal PDA conditions of 500 °C with Si IPL for La$_2$O$_3$/p-GaAs gate stack, excellent electrical characteristics such as low frequency dispersion (<8% and 230 mV) with higher oxide capacitances, decreased hysteresis widths, reasonable interfacial state density ($D_{it}$) value (~1.2×10$^{12}$ eV$^{-1}$ cm$^{-2}$) and lower gate leakages ($I_g$), makes La$_2$O$_3$/Si gate stacks a potential candidate for GaAs based MOSFET applications.
Reference:


5. L. Börnstein, “Phase Equilibria, Crystallographic and Thermodynamic data of Binary Alloys”, Group IV - Volume 5.


145

