CHAPTER-1

Introduction & Organization of the Thesis

1.1 Introduction

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Reference
1.1 INTRODUCTION

Technological developments in almost all the fields of Engineering and Science, all over the world, have paved the way for extraordinary growth of low-dimensional devices, called Nanodevices [1.1 - 1.10], which are developed using crystal growth technology resulting in fabrication of thin layer structures, applying various algorithmic based techniques using various required and desired materials, resulting in low dimensional, low power consumption and high speed/high frequency devices [1.11 - 1.13]. Nanodevices reign the world and change the day-to-day life-style of the people in the coming decades.

The growth in activity surrounding nano materials continues unabated as more R&D funds are poured into nano technology. Advances in existing production techniques are improving the quality and yields, providing a clear prospect of commercially viable volume production. There is still a wide range of processes being used, and it is clear that some of them will be commercially successful and will be those for which the materials have been developed at the same time as the application. Recent reports from a number of working groups have highlighted the need for increased examination of the health, environmental, and ethical aspects of nano technology, and this is an area that the industry will need to understand more fully and take appropriate action if the benefits of nanomaterials are to be realized.
The fact that materials can be divided into very small particles does not immediately mean that they have any practical use. However, the fact that these materials can be made at this scale gives them the potential to have some very interesting properties. Materials at the nanoscale between 1nm and 250nm lie between the quantum effects of atoms and molecules and the bulk properties of materials[1.14 - 1.20]. It is in this ‘no-man’s-land’ where many physical properties of materials are controlled by phenomena that have their critical dimensions at the nanoscale. By being able to fabricate and control the structure of nanoparticles, the scientist and engineer can influence the resulting properties and, ultimately, design materials to give desired properties. The electronic properties that can be controlled at this scale are of great interest. The ranges of application where the physical size of the particle can provide enhanced properties that are of benefit are extremely wide. Advances in nanotechnology may lead to the development of new biomaterials and implants; improve drug delivery; endow therapeutics with improved solubility and more precise targeting of diseased tissue; make diagnostics less invasive, more rapid, and more informative; and enable more complex biomedical research.

As per semiconductors technologists the end of CMOS scaling will occur around 2016. Technologies such as spintronics, nano devices etc have spurred interest in emerging alternative technologies, particularly nanotechnologies that
promise to extend Moore’s Law beyond 2016. The semiconductor industry has already entered the nanotechnology world: In 2000, it introduced the 130 nm node with a 70 nm gate-length feature size, followed in 2002 by the 90 nm node featuring a critical dimension of 25 nm. [1.21 - 1.30]. Industry leaders see new scalable technologies emerging from the novel alternative architectures and devices being proposed today that will take us through multiple processor generations for another 30 years or so. Reviewing the lessons learned in the semiconductor industry over the past few decades helps us to understand the emerging technologies and suggests some criteria for bringing current research efforts into the realm of high-volume manufacturing. We are equally confident that from the novel alternative architectures and devices being proposed today, new scalable technologies – hopefully not too many, will emerge- that will take us through multiple processor generations for another 30 years or so.

An analysis based on fundamental quantum mechanical principles reveals that heat dissipation will ultimately limit any logic device using an electronic charge. This analysis of an arbitrary switching device made up of a single electron in a dual quantum well separated by a barrier and operating at room temperature shows that the amount of power pulled off the material surface ultimately limits device density and operation frequency [1.31 - 1.36]. That limit is about 100 watts per square centimeter for passive cooling techniques with no active or electro thermal elements. This calculation demonstrates that even
though nanotubes and nanodots may allow the fabrication of smaller and faster
devices, power dissipation requires spreading them out and slowing them down to
keep from vaporizing the chip.  Semiconductor Research Corporation task force
working on Emerging Research Devices determined that taxonomy was needed to
give some organization to this grown field of research in which the problem
domains have not yet been well differentiated.  A basic CMOS device such as an
FET uses Boolean logic gates (AND/OR gates, XNOR gates, and so forth) in a
Boolean architecture, and the state variable is associated with the presence or
absence of electric charge differentiating the 1 and 0 state in a binary digital data
representation.  Categorizing the devices, architectures, variables, and data
representations that populate this space of emerging alternative technologies is
even more challenging.  Although it is likely to undergo numerous revisions, this
taxonomy provides a starting point for developing an organizational structure to
frame future discussions.

To form carbon nanotubes, an atomic planar sheet of carbon atoms is
bonded together into an array of hexagons and rolled up to form molecular tubes
or cylinders with 1 to 20 nm diameters and ranging from 100 nm to several
microns in length [1.37-1.40].  The details of fabrication determine a nanotube’s
electronic properties – that is, whether it is a semiconductor or a metal.
Researchers at several institutions have fabricated CNT-FET device structures
with the standard source, drain, and gate, but with a CNT replacing the silicon
channel [1.41-1.45]. Recent studies show that it is possible to form a low-leakage gate dielectric by atomic layer deposition of a zirconium dioxide thin-film (8 nm) high-gate material on top of an array of CNT-FETs. The zirconium dioxide gate insulation provides high capacitance, allowing efficient charge injection and reducing current leakage. Performance characteristics for this prototype device have shown good switching characteristics as measured by the sub threshold slope. All the known processes for producing CNT materials produce CNTs of all types and sizes mixed together. To make devices, the nanotubes must be separated into groups of similar size. Currently, a laborious manual process using a scanning tunneling microscope is the only way to separate the tubes.

NEC has introduced a room temperature single electron transistor (SET) that implements an “island” surrounded by TiOx barriers a quantum dot – where the presence or absence of a single electron controls the current flow from source to drain via the Coulomb blockade effect [1.46 - 1.56]. Connected through tunneling barriers, the conductance of the dot exhibits strong oscillations as the voltage of a gate electrode is varied. Each successive conductance maximum corresponds to the discrete addition of a single electron to the dot. This prototype device currently has problems associated with stray charges in the substrates, but there may be ways to handle that. In addition, several concepts of single electron memory have been experimentally demonstrated, including a SET/FET hybrid [1.57 - 1.61].
Another novel device is a molecular switch constructed by Mark Reed’s group at Yale. Molecular memory is a broad term combining different proposals for using individual molecules as building blocks of memory cells in which one bit of information can be stored in the space of an atom, molecule, or cell. Placing 100 or so molecules between the source and drain actually changes their molecular state and thus their I-V characteristics. This molecular memory stores data by applying external voltage that causes the transition of the molecule into one of two possible conduction states. The molecular memory reads the data by measuring resistance changes in the molecular cell. This operational characteristic is frequently represented as a hysteresis plot with voltage on the horizontal axis and resistance on the vertical axis. All of these devices use electrons as their state variables, but it is possible to envision devices that manipulate other state variables.

The integration of semiconductor devices in 3D arrays is being driven from two distinct directions. The first is associated with the need to integrate dissimilar technologies on a common platform to deliver an optimum information processing solution. It is clear that emerging technologies beyond scaled CMOS offer the potential for greatly improved performance by mixing and matching technologies for particular applications. The combination of technologies requires the 3D integration of functionally dissimilar technologies beginning with microprocessors, ASICs, and DRAMs and extending to RF, analog, optical and
MEMS [1.62 - 1.70]. These dissimilar technologies may later include 3D integration of molecular, plastic, rapid single-flux quantum superconductors and other emerging technologies directly on to silicon platforms.

Basically all specific IC manufacturers strive hard to provide high speed and high frequency devices. These are the major factors in deciding the device performance. Transistors are the basic components in VLSI circuits. Hence to make the transistor used in VLSI circuits, to operate at high frequency, we are to reduce the base transit time of a transistor. Base transit time is an important parameter in determining the high frequency response of the devices. It is a fact that incorporation of carbon into the base of a transistor can change the base transit time ($\tau_b$), thereby changing the switching speed of the device. But improper amount of carbon content can create several problems. We can use artificial neural network (ANN) to predict optimum doping concentration thereby determining the least base transit time [1.71 - 1.80]. However sufficient attention should be focused on the fact that the doping of carbon for reducing the base transit time will not disturb the normal activities of the HBT.

Technological developments of the crystal growth techniques resulted in the fabrication of thin layer structures. A layer of indium antimonite [1.81 - 1.82] sandwiched between layers of aluminum indium antimonite can act as a quantum well. This approach is used for constructing very fast transistors. Bipolar transistors operating at frequencies up to 85 GHz were constructed from indium
antimonite in the late 1990s. Field effect transistors operating at over 200 GHz have been reported more recently (Intel/QinetiQ). Some models suggest terahertz frequencies are achievable with this material. Different scattering mechanisms are very important for the high speed and high frequency InSb based Quantum well like other quantum wells. The electron motions in quantum well are decelerated by the different scattering mechanism. Scattering due to ionized impurity plays an important role here. The effect of ionized impurity can be reduced by modulation doping, providing high electron mobility at low temperatures where phonon scattering is suppressed. The small effective mass and consequent high mobility of the carriers have been utilized in the fabrication of high frequency and high-speed circuit devices, and magnetic field sensors.

As ever increasing power of computer chips brings us closer and closer to the limits of silicon technology, the future will belong to “spintronics”: a nanoscale technology in which information is carried not by the electronic charge. Yet even Moore’s law will run out of momentum one day as the size of features on an IC chip approaches the dimensions of atoms- this has been called the end of the silicon road map. For this reason and also to enhance the multifunctionality of devices (for example, carrying out processing and data storage on the same chips), investigators have been eager to exploit another property of the electron-a characteristic known as ‘spin’. Spin is purely quantum phenomenon roughly akin to the spinning of a child’s top or the directional behavior of a compass needle. A
top can spin in a clockwise or counter clock direction; electrons have spin of a sort in which the compass needles can point either “up” or “down” in relation to a magnetic field. Spin therefore lends itself elegantly to a new kind of binary logic of ones and zeros. The movement of spin, like the flow of charge, can also carry information among devices.

In recent years the emerging research field spin-electronics or spintronics has received a great deal of attention [1.81, 1.82]. Conventional electronics are based on the charge of the electron. Attempts to use electron’s other fundamental property, viz., ‘spin’, gave rise to a new, rapidly evolving field, known as spintronics. This opens the new routes for design of novel devices that are extremely faster, nonvolatile, and therefore have no boot up time, and have low power consumption. In fact first generation spintronics devices are already in existence and are currently used or under development, in the magnetic recording industry. Example includes spin-valve and current perpendicular to the plane giant magneto resistance (GMR) read heads [1.81-1.85] and non-volatile magnetic random access memory (MRAM), [1.81, 1.82, 1.87] based on tunneling magneto resistance (TMR) [1.81, 1.82, 1.88]. Future generation of spintronics device promise to combine technologically important nonmagnetic semiconductors with magnetism, either by synthesizing dilute magnetic semiconductors [1.86,1.89] or by fabricating hetero-structures with conventional ferromagnetic metals [1.90,1.91].
Most integrated circuits (ICs) of sufficient complexity utilize a clock signal in order to synchronize different parts of the circuit and to account for propagation delay. As ICs become more complex, the problem of supplying accurate and synchronized clocks to all the circuits becomes increasingly difficult. The pre-eminent example of such complex chips is the microprocessor, the central component of modern computers, which relies on a clock from a crystal oscillator. The ordinary Multivibrator circuits (555 timers) that are used for clock generation have on delay and off delay time. This is due to the internal and external device capacitances and finite transport time of the carriers. So a perfect pulse is hardly achievable and hence perfect synchronization is very difficult to be realized. Moreover, the speed of response is limited to a certain maximum value of the order of 10-100 GHz. However, in the era of Global communication the speed has to be increased several times to cope with the ever increasing demand of ultra fast processors.

A spintronic device based Digital Signal Generator can be integrated with digital communication systems and microprocessors to achieve versatile functionalities and high response speed along with perfect synchronization. Since the spintronics based devices operate with the principle of Quantum spin flip that occurs instantaneously in a quantum dot, the delay concept vanishes and we can get into the era of complete synchronization and ultra high speed with ultra low power dissipation and ultra high integration [1.92 – 1.95].
1.2 ORGANIZATION OF THE THESIS

This thesis embodies some studies on the characteristics of low-dimensional, low power consumption and high frequency devices and some of their applications which are very important from the technological point of view. An introduction and basic organization of the thesis is presented in this chapter. The remaining part of the thesis is organized as follows: Chapter 2 deals with High frequency response characteristics of InSb Quantum Well. Artificial Neural network based Base Transit Time Prediction for better HBT is detailed in chapter 3. Chapter 4 deals with a spintronic device based RFID system. Nanocrystalline ZnO-Si Heterojunction Methane Sensor is fabricated and its performance is studied in chapter 5.

The thin layers made by InSb and InSb-based alloys have found considerable interest due to their potential applications in groups III–V semiconductor-based infrared optoelectronic devices. The small electronic effective mass and consequent high mobility of the carriers of InSb have been utilized in the fabrication of high frequency and high-speed circuit devices. From a technology point of view heteroepitaxy of InSb on GaAs substrates is advantageous for monolithic integration of InSb devices on GaAs substrates in microelectronics and infrared detector array fabrication. To understand the basic carrier kinetics, the study of high frequency transport of two dimensional (2D) hot electrons in InSb needs a careful investigation.
Basically all specific IC manufacturers strive hard to provide high speed and high frequency devices. These are the major factors in deciding the device performance. Transistors are the basic components in VLSI circuits. Hence to make the transistor used in VLSI circuits, to operate at high frequency, we are to reduce the base transit time of a transistor. Base transit time is an important parameter in determining the high frequency response of the devices. It is a fact that incorporation of carbon into the base of a transistor can change the base transit time ($\tau_b$), thereby changing the switching speed of the device. But improper amount of carbon content can create several problems. We can use artificial neural network (ANN) to predict optimum doping concentration thereby determining the least base transit time. However sufficient attention should be focused on the fact that the doping of carbon for reducing the base transit time will not disturb the normal activities of the HBT.

The Spintronics logic has been proposed for the first time in 1994 as a classical paradigm where binary bits 0 and 1 are encoded in the bistable spin polarization of single electrons confined in quantum dots and binary bits 1 and 0 are encoded into anti parallel spin polarization of single electron confined in the quantum dot placed in magnetic field. The split metal gates, called wrap-around split Schottky gates, delineate quantum dot electro statically in a penta-layered structure consisting of a Ferro-magnet-insulator semiconductor-insulator- Ferro-magnet combination. The “writing” and “flipping” operations are performed by
using these gates. We have to reverse the spin polarization (or rotate it by 180 degree) to flip a bit. It appears that realization of a system based on the present scheme can provide simultaneously higher processing speed and high density of component integration at reasonably reduced cost. The candidate plans to have application of spin based logic circuits here. In this present work the candidate has designed a RFID system using single spin logic for anti-collision Binary-tree scheme. It is sure that present circuit is much faster than the conventional logic circuits and supports very high-density of integration. Spin based logic circuits are of course at the top of the hierarchy.

The theoretical values are substantiated by software based simulation to show the possible spin orientations. Further he has calculated the power dissipation as well as speed of response of spintronics devices and compare them with those of other types of devices like MOSFET and SET devices. The power dissipation of the spintronics devices is extremely small about tens of nano Watt per bit switching and the power delay product is $\sim 10^{-20}$ J which is comparable to that of quantum interference devices. The Spintronics devices can operate at extremely high speed and flip time is of the order of 1ps because there is no movement of charge during the operation of these devices and is not limited to transit time or resistance capacitance (RC) time constant. Hence such a high switching speed can never be achieved by conventional CMOS devices or quantum interference devices.
ZnO based gas sensors are widely used for environmental monitoring and industrial applications due to their advantages like small dimensions, low cost and convenient operation. On interaction with reducing gases, adsorbed oxygen concentration results in change of conductivity. The change in conductivity defines a measure of gas concentration. As the gas sensing mechanism is a surface reaction, use of nanostructured material improves gas sensing characteristics. Thus ZnO is greatly recognized for different commercial applications. In the present work a sol–gel derived Si-ZnO heterojunction with Au and Al gate pad is fabricated for the purpose of methane sensing. The characteristics of the device are studied by varying the temperature from 50°C to 250°C. The optimum temperature and voltage are calculated through the V-I characteristics with the presence of the reducing gas. The response magnitude of the device is found as ~52%.

The outcome and the conclusions of the present study summarized and provides the directions of future work in Chapter-6.
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