CHAPTER IV

MICROPROCESSOR BASED PHASE AND FAULT IDENTIFIER
CHAPTER - IV

MICROPROCESSOR BASED PHASE AND FAULT IDENTIFIER

4-1. INTRODUCTION:

For many industrial applications, an accurate and reliable identification of phase sequences and single phase condition of supply are essential as well as desirable. Also for rectification of faults identification of the nature of faults is essential and is extremely helpful to restore the healthy condition of the supply.

In this investigation, a microprocessor based scheme has been developed for on-line identification of phase sequence, single phasing together with system faults such as phase to phase, phase to earth and double phase to earth faults. Unlike conventional arrangements, the proposed scheme indicates the nature of the fault, indicates the particular phase or phases under fault well before the conventional protection system operates. The proposed scheme may meet the present needs of complex power networks.

4-2. SYSTEM HARDWARE:

The schematic block diagram of the system hardware is shown in fig. 4-1 whereas the sensor circuit with input terminals R-Y-B and load resistances $R_0$ and $R'_0$ are shown
FIG 41: SCHEMATIC BLOCK DIAGRAM OF THE SYSTEM HARD WARE
Fig. 4-2: Sensor circuit.
FIG. 4-3: EQUIVALENT SENSOR CIRCUIT.
in fig. 4-2. Required reference signal for the microcomputer (INCONIX - IMS 5808) is generated across the resistance $R_0$ for both R-Y-B and R-B-Y phase sequences, single phase condition of supply and also for various fault conditions.

The analysis of the sensor circuit has been shown in previous chapter (2-2.2). The voltage $V_0$ developed across $R_0$ (under healthy condition) from equation (2-9) in chapter 2, is given by,

$$V_0 = f_{Rg} \frac{[2r (V_1-V_8)-(r-\frac{j}{\omega C}) (V_2-V_8)] R_0}{2r (5r-3j/\omega C)} \quad \text{(4-1)}$$

The same voltage under single phasing condition (when B-phase is open) is obtained by assuming $R^\infty$ infinitely large as shown in chapter-2, equation (2-10), as

$$[V_0]_{\phi} = \frac{2r-(V_1-V_8)}{(3r-\frac{j}{\omega C})^2 + (r-\frac{j}{\omega C})2r} \quad \text{(4-2)}$$

Where, $V_1$, $V_8$, and $V_2$ are voltages in R,Y, and B phases of supply respectively. The expression for the voltage appearing across $R_0$ when R and Y-phase is open can simultaneously be obtained.
The Voltages generated under various Conditions of fault may also be calculated from (4-1) considering different conditions of the system.

**LL - Fault:**

\[
\begin{align*}
V_1 &= V_8 = \frac{-\left( r - \frac{1}{Wc} \right) \left( V_2 - V_8 \right)}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.4) \\
V_2 &= V_1 = \frac{\left[ V_1 - V_8 \right] (r + \frac{1}{Wc})}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.5) \\
V_2 &= V_8 = \frac{2r (V_1 - V_8)}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.6)
\end{align*}
\]

**L - G Fault:** (Single phase to earth)

\[
\begin{align*}
V_1 &= 0 = \frac{-2r V_3 - (r - \frac{1}{Wc}) \left( V_2 - V_8 \right)}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.7) \\
V_8 &= 0 = \frac{2r (V_1 - V_8)}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.8) \\
V_2 &= 0 = \frac{2r (V_1 - V_8) + (r - \frac{1}{Wc}) V_8}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.9)
\end{align*}
\]

**L - L - G Fault:**

\[
\begin{align*}
V_1 &= 0 = \frac{-\left( r - \frac{1}{Wc} \right) \left( V_2 \right)}{2r (5r - \frac{3j}{Wc})} R_o \quad \ldots \ldots (4.10) \\
V_8 &= 0 = \frac{-R_o \left( r + \frac{1}{Wc} \right) V_8}{2r (5r - \frac{3j}{Wc})} \quad \ldots \ldots (4.11) \\
V_2 &= 0 = \frac{2r R_o \ V_1}{2r (5r - \frac{3j}{Wc})} \quad \ldots \ldots (4.12)
\end{align*}
\]
Table - 4.1 represents voltages developed across $R_q$ in mV under different sequential mode, single phasing condition of supply and under different fault conditions of the system using $r = 120K = R_g$ and $C = 0.01 \mu F$ magnitude of three phase line voltages being $400 \pm 12.5\%$.

**TABLE - 4.1**

<table>
<thead>
<tr>
<th>Mode of supply/ fault</th>
<th>Voltage across $R_q$ = 500 ohms with input voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(400 + 12.5%) V</td>
</tr>
<tr>
<td></td>
<td>Analog Voltage in mV</td>
</tr>
<tr>
<td>R-Y-B (Normal phase)</td>
<td>92</td>
</tr>
<tr>
<td>Single phasing with:</td>
<td>R-Phase open</td>
</tr>
<tr>
<td></td>
<td>Y-Phase open</td>
</tr>
<tr>
<td></td>
<td>B-Phase open</td>
</tr>
<tr>
<td>Reversed Phase (R-B-Y)</td>
<td>448</td>
</tr>
<tr>
<td>Phase to L-G Fault:</td>
<td>R-G</td>
</tr>
<tr>
<td></td>
<td>B-G</td>
</tr>
<tr>
<td></td>
<td>Y-G</td>
</tr>
<tr>
<td>Phase short circuit</td>
<td>R-Y</td>
</tr>
<tr>
<td></td>
<td>Y-B</td>
</tr>
<tr>
<td></td>
<td>B-R</td>
</tr>
<tr>
<td>Double phase to L-L-G Fault:</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R-YG</td>
</tr>
<tr>
<td></td>
<td>Y-BG</td>
</tr>
<tr>
<td></td>
<td>B-RG</td>
</tr>
</tbody>
</table>
4-3. **SYSTEM SOFTWARE**

The signal developed across $R_0$ being rectified and filtered and is received by the microcomputer input port instantaneously through ADC, (having 12 bit resolution, conversion rate being 7.5 samples per second) converting the analog voltage to digital form and stored in a particular RAM location. Digital values of signals corresponding to the upper and lower limit of the reference voltages (viz. $400 \, V \pm 12.5\%$) developed across $R_0$ for R-Y-B, R-B-Y, mode of supply, single phasing (when B-Phase is open and also when R-or Y-Phase is open) are stored in eight successive RAM locations starting from memory location $(A_4, A_3, A_2, A_1)$. The upper and lower limits of the digital signals corresponding to the voltages developed across $R_0$ under different faults (viz. YBG, YG, RYG/RBG, BG, RG, RX/BR, YB fault conditions) are stored in fourteen consecutive RAM locations starting from $(B_4, B_3, B_2, B_1)$ to $(B_4, B_3, B_2, B_1 + D)$. The complete software of the system has been developed to execute the system under two different modes vis. 00 mode for identifying RYB, single phasing and RBY phase sequences and 01 mode for identification of different fault conditions. In the absence of supply, the accumulator receives no signal and keeps the display screen blank following a proper software.

The first task of the microcomputer is to identify the mode of execution comparing the corresponding data (00H or 01H) transferred to accumulator from a particular RAM location.
with $00\ H$ stored in register B. The first mode being identified, the next task of the ALU is to compare the instantaneous input digital reference signal received from $R_0$ first with the content of memory locations $(A_4', A_3', A_2', A_1)$ and $(A_4', A_3', A_2', A_1 + 1)$ and displays R-Y-B in the address field of the display screen if the instantaneous value is within the limiting zone of the particular phase sequence. If the instantaneous signal exceeds the upper limit, the ALU is allowed to compare the same with the upper and lower limiting signals stored in memory locations $(A_4', A_3', A_2', A_1 + 2)$ and $(A_4', A_3', A_2', A_1 + 3)$ respectively corresponding to the single phasing condition with B-phase open circuited and displays 'SPBO' provided the instantaneous signal is within the limiting zone of single phase condition. The upper limiting value of signal being crossed, the task of ALU is to compare the same within the upper and lower limiting signals stored in memory locations $(A_4', A_3', A_2', A_1 + 4)$ and $(A_4', A_3', A_2', A_1 + 5)$ respectively corresponding to the single phase condition when either R or Y phase is open and displays 'SPRO' and 'SPYO' alternately on the display screen if the instantaneous signal is within the limiting zone. The upper limiting value being crossed, the task of the ALU is to compare the same with the upper and lower limiting signals stored in memory locations $(A_4', A_3', A_2', A_1 + 6)$ and $(A_4', A_3', A_2', A_1 + 7)$ respectively corresponding to the R-Y-B mode of supply and displays R-Y-B if the instantaneous signal is within the limiting zone of R-Y-B mode of supply.
In the second mode (i.e. 01H mode) of operation, the microprocessor through its software acknowledges the upper and lower limiting signals stored in memory locations \((B_4, B_3, B_2, B_1)\) and \((B_4, B_3, B_2, B_1 + 1)\) corresponding to YBG (yellow phase to blue phase to ground) fault condition and compares the same with the instantaneous value being received in the accumulator. It displays 'YBGF' on the displays screen provided \((B_4, B_3, B_2, B_1) > (\text{Acc}) > (B_4, B_3, B_2, B_1 + 1)\) is satisfied. Otherwise if upper limit be crossed, the task of the microprocessor is to satisfy itself with the inequality \((B_4, B_3, B_2, B_1 + 2) > (\text{Acc}) > (B_4, B_3, B_2, B_1 + 3)\) for the YG (yellow phase to earth) fault in order to display YGF on the display screen. In the same manner, it displays RBGF/RYGF (alternately), BGF, RGF, YGF, and RYF/BRF (alternately) for \(m=2,3,4,5\) and 6 respectively provided the condition \((B_4, B_2, B_2, B_1 + 2m) > (\text{Acc}) > \left[(B_4, B_3, B_2, B_1) + (2m + 1)\right]\) is satisfied. Otherwise, it stops execution. The flow-chart corresponding to the software is shown in fig. 4-3. The program listing has been presented in Appendix - 4.

4-4 CONCLUSION:

With the growing complexity of modern power networks fast, accurate and reliable phase and fault identification schemes are becoming necessary. Proposed microprocessor based scheme can fulfil these requirements at a competitive price. The scheme offers attractive compactness and
and flexibility and reduces the number and types of identification units.

In the present investigation, a unique microprocessor based static system has been developed for the identification of different phase sequences and single phasing condition together with the identification of different faults of the system. The system is unique in the sense that it can identify the phase sequences and the single phase condition of the supply clearly identifying the particular phase which is open. The same system is also capable of identifying various fault conditions of the supply indicating phase-earth, phase-phase, short circuit and double phase to earth faults clearly stating the particular phase or phases under fault. Thus it avoids confusion in detecting different conditions of supply and faults displaying appropriate symbols on the display screen.

Though the system has been designed for a three phase, 400V supply system with a tolerance of \( \pm 12.5\% \), it can be used for any three phase input voltage with a minor modification in the arrangement. The magnitude of input signal to the microprocessor through ADC from \( R_0 \) can be changed simply by changing the value of \( R_0 \).

It is interesting to mention that the proposed system indicates the nature of faults so quickly compared to
conventional protective system that it detects the faults before the protective system starts to operate. Since there is no moving parts associated in this system, it is free from maintenance and reliable in operation. The proposed scheme is simple in construction, fast and accurate in action, versatile in nature and it is expected to be widely used in industry to meet the present needs of complex power networks.

4-5. REFERENCES:

BOOKS: 1, 3, 4, 5, 8, 11, 12, 13, 14-41.

JOURNALS: 12, 20, 25, 35, 37, 40, 46, 52, 71, 80, 81-91, 94.