STARTING, CONTROL AND SPEED REGULATION OF DC MOTOR USING PULSED SUPPLY METHOD

5.1 INTRODUCTION

During last few years, pulsed-supply method of speed control [31, 57, 158] of low power (FHP) motors gained considerable attention. In this method, the motor operating parameters are controlled in such a way and with such a frequency that, the motor acquires a definite average speed over a full cycle of change of the operating parameters. The value of the average speed may be controlled by setting up a certain ratio between the durations of the motor acceleration and deceleration periods. If cycles are repeated continuously at a definite frequency and the elements of the cycle (i.e. ON and OFF periods) are maintained in fixed relationship with respect to each other, the motor will run at a definite constant average speed, although its instantaneous speed remains variable.

5.2 OBJECTIVE

In this investigation, an attempt has been made to convert the so-called constant speed DC shunt motor into a variable speed motor and to overcome the fluctuation of speed due to load or supply voltage variation by adjusting armature supply voltage by controlling duty factor using "Bang Bang" (BB) control methodology. In controlling duty
factor, for intelligent control and to eliminate conventional complex hardware circuitries, an 8085A CPU based microprocessor utilised.

5.3 THEORY

With the motor load torque constant, the average speed will change with relative duration of ON and OFF periods of the armature voltage. If 'T(ON)' and 'T(OFF)' be the duration of ON period and that of OFF period respectively, the relative duration of supply pulse can be expressed as the ratio (Duty Factor):

$$\frac{T(ON)}{T(ON) + T(OFF)}$$

and the average voltage 'V(AV)' impressed on the load becomes,

$$V(AV) = \frac{T(ON) \times V}{T(ON) + T(OFF)}$$

where V is the supply voltage.

It is evident that, an increase in the value of ( with the motor operating at constant load will result in a rise in motor speed. It is well known that, the motor speed varies with the change in load for constant ( i.e. for a given value of the supply-pulse duration factor, any drop in load will lead to a rise in speed and vice versa. On the other hand for a constant duty factor, during fluctuation of supply voltage, motor speed fluctuates accordingly.

5.4 SYSTEM HARDWARE

The simplified circuit diagram of the proposed scheme has been presented in fig. 5.1. In this control scheme, the average armature voltage is controlled by controlling the pulse width of the supply voltage. The controller used here is the microprocessor which generates the pulse with controlled width. The pulse is applied to the base of the
FIG. 5.1 SIMPLIFIED CIRCUIT DIAGRAM OF THE PROPOSED SCHEME.
transistor. Due to high power handling capability, a power transistor (2N 3055SD) has been used as a switching element by means of which the average voltage is controlled.

During ON period of the pulse, the transistor conducts only, otherwise it remains in OFF state and hence the average voltage can be controlled by controlling the pulse width.

In order to isolate the logic circuit from power circuit, an opto-isolator circuit based on IC MCT-2E with an amplifier using transistor SL-100 has been used. The switching signal in this way electrically isolates the microprocessor and switches the power transistor. The detailed circuit diagram of the opto-coupler based triggering circuitry has been presented in Chapter - 2.

A tacho-generator (TG) (feedback element) connected with the motor shaft is used to convey the instantaneous analog voltage signal proportional to the speed of the motor. The analog voltage signal being an instantaneous (dynamic) feedback signal, enters into the microprocessor through port PA of 8255(2) and analog to digital converter (ADC) based on IC 0809.

5.5 OPERATIONAL STRATEGY

DC shunt motors suffer from fluctuation of speed due to the fluctuation of supply voltage and the variation of load. The proposed scheme eliminates speed fluctuation due to reasons cited above by adjusting the supply voltage by controlling duty factor.

The task of the microprocessor is to generate controlled pulse. The desired speed being attained, the microprocessor receives the signal from the tachogenerator and stores it as a set value. During running, the microprocessor always receives the instantaneous tacho signal,
compares the same with the set value and generates the controlled pulse to run the motor at a desired speed.

The control strategy is such that when the speed of the motor is reduced due to the reasons cited above, the microprocessor increases the ON period and decreases the OFF period and automatically the average impressed voltage increases enhancing the speed of the motor. Conversely, when the speed of the motor increases above desired speed, the microprocessor, increasing the OFF period and decreasing the ON period, decreases the effective average voltage to the motor reducing the speed.

In this control philosophy, to adjust duty factor, Bang-Bang control mode of operation has been provided through which, the microprocessor adjusts the duty factor in steps by gradually increasing ON period and decreasing OFF period or by decreasing ON period and increasing OFF period according to the nature of the fluctuation of speed. This has been achieved by adjusting a number may be called "DELAY NUMBER" (6) (described in Chapter - 3) in the software.

5.6 SYSTEM SOFTWARE

The detailed flowchart for system software has been presented in Flow-Diagram. The software has been developed in such a way that, the microprocessor generates the rectangular pulse through port PBO with predetermined ON and OFF periods stored in the particular RAM locations. During ON period, the pulse energises the LED of the opto-coupler circuitry and produces the output which after amplification is impressed on the base of the power transistor and the transistor conducts.

In order to stabilise the speed of the motor, sufficient number of rectangular pulses should be provided to the motor. This number of
FLOW CHART

FLOW CHART FOR CLOSED LOOP CONTROL:

1. START

   INITIALISE STACK POINTER, PORT A AS INPUT PORT AND
   PORT B AND C AS OUTPUT PORTS

   SET DELAY NUMBER 'δ(ON)' AND 'δ(OFF)' CORRESPONDING TO TIME
   DELAY 'T(ON)' AND 'T(OFF)' RESPECTIVELY FOR STARTING IN TWO
   SUCCESSIVE MEMORY LOCATIONS

   SET REG. D AS A COUNTER

   GENERATE AND OUTPUT SWITCHING SIGNAL THROUGH PORT PBO
   FOR TIME 'T(ON)' CORRESPONDING TO DELAY NUMBER 'δ(ON)'

   CALL DELAY SUBROUTINE CORRESPONDING TO DELAY NUMBER 'δ(OFF)'
   FOR TIME 'T(OFF)'

   DECREMENT (REG. D)

2. 

   IS (REG. D) = 0?

   YES

   INPUT TACHO SIGNAL THROUGH ADC AND SET IT AS SET VALUE 'E(SET)'

   SET REG. D AS A COUNTER

   GENERATE AND OUTPUT SWITCHING SIGNAL THROUGH PORT PBO
   FOR TIME 'T(ON)' CORRESPONDING TO DELAY NUMBER 'δ(ON)'

   CALL DELAY SUBROUTINE CORRESPONDING TO DELAY NUMBER 'δ(OFF)'
   FOR TIME 'T(OFF)'

   NO
A

DECREMENT (REG. D)

\[ (\text{REG. D}) = 0 \]

YES

INPUT INSTANTANEOUS TACHO SIGNAL 'E(IN)' THROUGH ADC

COMPARE 'E(IN)' FROM 'E(SET)'

\[ \text{RESULT} = 0 \]

YES

\[ \begin{align*}
\text{SET } \delta(\text{ON}) &= \delta(\text{ON}) - 01H \\
\delta(\text{OFF}) &= \delta(\text{OFF}) + 01H
\end{align*} \]

CARRY SET

NO

SET \[ \delta(\text{ON}) = \delta(\text{ON}) + 01H \]
\[ \delta(\text{OFF}) = \delta(\text{OFF}) - 01H \]

YES

\[ \begin{align*}
\text{SET } \delta(\text{ON}) &= \delta(\text{ON}) + 01H \\
\delta(\text{OFF}) &= \delta(\text{OFF}) + 01H
\end{align*} \]

NO

\[ \begin{align*}
\text{SET } \delta(\text{ON}) &= \delta(\text{ON}) - 01H \\
\delta(\text{OFF}) &= \delta(\text{OFF}) - 01H
\end{align*} \]
repetition of the generated pulse is previously stored in Reg. B. Desired speed being attained, the microprocessor receives the instantaneous digitised tacho signal from ADC through port PA of 8255(2), recognises it as the set value 'E(SET)' and stores it in a particular RAM location.

The next task of the microprocessor is to receive the instantaneous tacho signal 'E(IN)' through ADC corresponding to the motor speed and compares the same with the permissible set value stored previously. The results being equal, the microprocessor generates the pulse keeping the same ON and OFF periods through preassigned number of times and again accepts the instantaneous value of the sensor signal in order to decide its future activity.

If the former comparison results in an inequality, the microprocessor examines whether the instantaneous signal is greater than the set value or less. If less, microprocessor adjusts the duty factor by increasing ON period and decreasing OFF period by one unit; otherwise it decreases the ON period and increases the OFF period to improve the motor speed and the same cyclic operation is repeated for a few cycles to stabilise the motor with new speed. Then again accepting the new tacho signal, it repeats the cyclic operation until the motor attains its desired speed.

5.7 EXPERIMENT

The developed scheme has been implemented in the laboratory to control the speed of a 40 V, 0.2 KW, 1500 RPM DC shunt motor. The experimental arrangement has been shown in fig. 5.1. In open loop control, the element of duty factor (i.e. Delay Number) has been changed and the speed (in RPM) and generated tacho voltage (in hex) have been
recorded and plotted. The switching signal for the power transistor at
different duty factor has been shown in fig. 5.2. The speed response of
the motor under experiment versus Delay Number for ON period and OFF
period relationship and the tacho voltage versus duty factor curve have
been shown in fig. 5.3 and fig. 5.4 respectively. The motor can be run
at any desired speed by storing the Delay Number corresponding to ON and
OFF period following calibration curve shown in fig. 5.3.

In closed loop control, the Delay Number has been stored in the
particular RAM location for 1000 RPM running of the motor which is
considered as set speed. To create sudden load fluctuation, magnetic
load has been used. Speed response oscillograms for 10%, 50%, 100% and
125% load fluctuation (i.e. No load to load and Load to no load) and 25%
supply voltage variation have been recorded and presented in fig. 5.5.
In these speed response curves, the points 'A' and 'B' represent speed
fluctuation and speed recovery instant respectively.

5.8 SOFTWARE LISTING

MAIN PROGRAM FOR OPEN LOOP CONTROL :

<table>
<thead>
<tr>
<th>MEM. LABEL</th>
<th>MNEMONICS</th>
<th>OPCODE</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOC.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4200</td>
<td>START:</td>
<td>31</td>
<td>DEFINE STACK POINTER AT MEM. LOC. 47FFH</td>
</tr>
<tr>
<td>4203</td>
<td>LXI SP</td>
<td>21</td>
<td>MSP 31 FF 47</td>
</tr>
<tr>
<td>4206</td>
<td>MVI T(ON)</td>
<td>36</td>
<td>20 STORE DATA 20H FOR ON PERIOD</td>
</tr>
<tr>
<td>4208</td>
<td>INX H</td>
<td>23</td>
<td>INITIALISE NEXT MEM. LOC.</td>
</tr>
<tr>
<td>4209</td>
<td>MVI T(OFF)D0</td>
<td>36 3E</td>
<td>STORE DATA FOR OFF PERIOD</td>
</tr>
<tr>
<td>420B</td>
<td>MVI A 80</td>
<td>3E 80</td>
<td>INITIALISE ALL PORTS AS OUTPUT PORTS</td>
</tr>
<tr>
<td>420D</td>
<td>OUT 0B</td>
<td>D3 08</td>
<td>SELECT I/O CHIP (CWR 0B)</td>
</tr>
<tr>
<td>420F LOOP:</td>
<td>MVI A 01</td>
<td>3E 01</td>
<td>ARRAY ACC. BIT PATTERN AS 01H</td>
</tr>
<tr>
<td>4211</td>
<td>OUT PB</td>
<td>D3 09</td>
<td>OUTPUT SIGNAL THROUGH PB</td>
</tr>
<tr>
<td>4213</td>
<td>LXI H</td>
<td>21 00</td>
<td>43 INITIALISE MEM. LOC. 4300H</td>
</tr>
<tr>
<td>4216</td>
<td>MOV D,M</td>
<td>56</td>
<td>MOVE MEMORY CONTENT TO REG. D</td>
</tr>
<tr>
<td>4217 LOOP1:</td>
<td>CALL DLY1</td>
<td>CD 42</td>
<td>CALL SUBROUTINE 'DLY1' FOR ON PERIOD</td>
</tr>
<tr>
<td>421A</td>
<td>DCR D</td>
<td>15</td>
<td>DECREMENT (REG.D)</td>
</tr>
<tr>
<td>421B</td>
<td>JNZ LOOP1</td>
<td>C2 17</td>
<td>JUMP ON NO ZERO TO LOOP1</td>
</tr>
<tr>
<td>421E</td>
<td>MVI A 00</td>
<td>3E 00</td>
<td>CLEAR ACC.</td>
</tr>
<tr>
<td>4220</td>
<td>OUT PB</td>
<td>D3 09</td>
<td>OUTPUT THROUGH PB</td>
</tr>
</tbody>
</table>
FIG. 5.2 NATURE OF SWITCHING SIGNAL AT DIFFERENT DUTY FACTOR ($\varepsilon$).

$\varepsilon = 0.1$  
$\varepsilon = 0.3$  
$\varepsilon = 0.6$  
$\varepsilon = 0.9$

$X$ AXIS : 2 $\mu$s / DIV  
$Y$ AXIS : 2 V / DIV
Supply voltage: 40 Volts.

\[ T(ON) + T(OFF) = 0FH \]

Fig. 5.3 Delay Number corresponding to ON-period vs. Speed in rpm.
Fig. 5.4  Duty factor vs. Tacho voltage
SPEED RECOVERY TIME

NO-LOAD TO 10% LOAD

NO-LOAD TO 50% LOAD

NO-LOAD TO 100% LOAD

NO-LOAD TO 125% LOAD

10% LOAD TO NO-LOAD

50% LOAD TO NO-LOAD

100% LOAD TO NO-LOAD

125% LOAD TO NO-LOAD

X AXIS: 1 S / DIV
Y AXIS: 500 mV / DIV

(a) SPEED RESPONSE OSCILLOGRAM DURING LOAD VARIATION.

FIG. 5.5 (a) SPEED RESPONSE OSCILLOGRAM DURING LOAD VARIATION.

138
FIG. 5.5 (b) SPEED RESPONSE OSCILLOGRAM DURING SUPPLY VOLTAGE FLUCTUATION.

X AXIS : 1 S / DIV
Y AXIS : 500 mV / DIV
Note: The speed of the machine is controlled by controlling input data 'T(ON)' and 'T(OFF)'. In this investigation T(ON) + T(OFF) = FOH, i.e. T(OFF) = FOH - T(ON) has been assumed. The speed will be increased with the increment of T(ON) and decrement of T(OFF).

MAIN PROGRAM FOR CLOSED LOOP CONTROL:

MEM. LABEL MNEMONICS OPCODE COMMENTS 
LOC. 

4230 START: LXI SP MSP 31 FF 47 ;DEFINE STACK POINTER AT MEM. LOC. 47FFH 
4233 LXI H M 21 00 43 ;INITIALISE MEM. LOC. 4300H 
4236 MVI M T(ON) 36 40 ;STORE 40H FOR ON PERIOD IN THE MEMORY 
4238 INX H 23 ;INITIALISE NEXT MEM. LOC. 
4239 MVI M T(OFF)36 CO ;STORE COH FOR OFF PERIOD THERE 
423B MVI E LC 1E 16 ;STORE DATA 16H FOR NUMBER OF CYCLIC OPERATION IN REG. E 
423D MVI A 90 3E 90 ;INITIALISE PA AS INPUT AND PB AND PC AS OUTPUT PORTS 
423F OUT OB D3 OB ;SELECT I/O CHIP (CWR OBH) 
4241 GO: MVI A 01 3E 01 ;ARRANGE ACC. BIT PATTERN AS 01H 
4243 OUT PB D3 09 ;OUTPUT SIGNAL THROUGH PB 
4245 LXI H M 21 00 43 ;INITIALISE MEM. LOC. 4300H 
4248 MOV D,M 56 ;MOVE MEMORY CONTENT TO REG. D 
424B LOOP1: CALL DLY1 CD CO 42 ;CALL SUBROUTINE DLY1 
424C DCR D 15 ;DECREMENT (REG. D) 
424D JNZ LOOP1 C2 49 42 ;IF RESULT IS NOT ZERO, JUMP TO LOOP1 
4250 MVI A 00 3E 00 ;OTHERWISE, CLEAR ACC. 
4252 OUT PB D3 09 ;OUTPUT THROUGH PB 
4254 LXI H (M+1) 21 01 43 ;INITIALISE MEM. LOC. 4301H 
4257 MOV D,M 56 ;MOVE MEMORY CONTENT TO REG. D 
4258 LOOP2: CALL DLY1 CD CO 42 ;CALL SUBROUTINE DLY1 
425B DCR D 15 ;DECREMENT (REG. D) 
425C JNZ LOOP2 C2 58 42 ;IF RESULT IS NOT ZERO, JUMP TO LOOP2 
425F DCR E 1D ;OTHERWISE, DECREMENT (REG. E) 
4260 JNZ GO C2 41 42 ;JUMP ON NO ZERO TO NEXT 
4263 CALL ADC CD 80 47 ;CALL SUBROUTINE ADC (ANNEXUER-2) 
4266 LXI H M3 21 02 43 ;INITIALISE MEM. LOC. 4302H 
4269 MOV M,A 77 ;MOVE (ACC.) TO THE MEMORY 
426A LOOP: MVI E NLC 1E 0A ;STORE DATA OAH IN REG. E FOR NUMBER OF CYCLIC OPERATION 
426C NEXT1: MVI A 01 3E 01 ;ARRANGE ACC. BIT PATTERN AS 01H
<table>
<thead>
<tr>
<th>MEM. LABEL</th>
<th>MNEMONICS</th>
<th>OPCODE</th>
<th>COMMENTS</th>
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<tr>
<td>LOC.</td>
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<tr>
<td>426E</td>
<td>OUT PB</td>
<td>D3 09</td>
<td>OUTPUT SIGNAL THROUGH PB</td>
</tr>
<tr>
<td>4270</td>
<td>LXI H M</td>
<td>21 00 43</td>
<td>INITIALISE MEM. LOC. 4300H</td>
</tr>
<tr>
<td>4273</td>
<td>MOV D,M</td>
<td>56</td>
<td>MOVE MEMORY CONTENT TO REG. D</td>
</tr>
<tr>
<td>4274</td>
<td>LOOP3: CALL DLY1</td>
<td>CD CO 42</td>
<td>CALL SUBROUTINE DLY1</td>
</tr>
<tr>
<td>4277</td>
<td>DCR D</td>
<td>15</td>
<td>DECREMENT (REG. D)</td>
</tr>
<tr>
<td>4278</td>
<td>JNZ LOOP3</td>
<td>C2 74 42</td>
<td>IF RESULT IS NOT ZERO, JUMP TO LOOP3</td>
</tr>
<tr>
<td>427B</td>
<td>MVI A 00</td>
<td>3E 00</td>
<td>OTHERWISE, CLEAR ACC.</td>
</tr>
<tr>
<td>427D</td>
<td>OUT PB</td>
<td>D3 09</td>
<td>OUTPUT SIGNAL THROUGH PB</td>
</tr>
<tr>
<td>427F</td>
<td>LXI H (M+1)</td>
<td>21 01 43</td>
<td>INITIALISE MEM. LOC. 4301H</td>
</tr>
<tr>
<td>4282</td>
<td>MOV D,M</td>
<td>56</td>
<td>MOVE MEMORY CONTENT TO REG. D</td>
</tr>
<tr>
<td>4283</td>
<td>LOOP4: CALL DLY1</td>
<td>CD CO 42</td>
<td>CALL SUBROUTINE DLY1</td>
</tr>
<tr>
<td>4286</td>
<td>DCR D</td>
<td>15</td>
<td>DECREMENT (REG. D)</td>
</tr>
<tr>
<td>4287</td>
<td>JNZ LOOP4</td>
<td>C2 83 42</td>
<td>IF RESULT IS NOT ZERO, JUMP TO LOOP4</td>
</tr>
<tr>
<td>428A</td>
<td>DCR E</td>
<td>1D</td>
<td>OTHERWISE, DECREMENT (REG. E)</td>
</tr>
<tr>
<td>428B</td>
<td>JNZ G01</td>
<td>C2 6C 42</td>
<td>JUMP ON NO ZERO TO G01</td>
</tr>
<tr>
<td>428E</td>
<td>CALL ADC</td>
<td>CD 80 47</td>
<td>CALL SUBROUTINE ADC (ANNEXUER-2)</td>
</tr>
<tr>
<td>4291</td>
<td>MOV C,A</td>
<td>4F</td>
<td>MOVE DATA FROM ACC. TO REG. C</td>
</tr>
<tr>
<td>4292</td>
<td>LXI H (M+2)</td>
<td>21 02 43</td>
<td>INITIALISE MEM. LOC. 4302H</td>
</tr>
<tr>
<td>4295</td>
<td>MOV A, M</td>
<td>7E</td>
<td>MOVE MEMORY CONTENT TO ACC.</td>
</tr>
<tr>
<td>4296</td>
<td>CMP C</td>
<td>B9</td>
<td>COMPARE (REG.C) WITH (ACC.)</td>
</tr>
<tr>
<td>4297</td>
<td>JZ LOOP</td>
<td>CA 6A 42</td>
<td>JUMP ON ZERO TO LOOP2</td>
</tr>
<tr>
<td>429A</td>
<td>JNC NEXT</td>
<td>D2 A8 42</td>
<td>IF CARRY BE SET, JUMP TO NEXT</td>
</tr>
<tr>
<td>429D</td>
<td>STC</td>
<td>37</td>
<td>OTHERWISE, SET CARRY</td>
</tr>
<tr>
<td>429E</td>
<td>CMC</td>
<td>3F</td>
<td>COMPLEMENT CARRY</td>
</tr>
<tr>
<td>429F</td>
<td>LXI H M</td>
<td>21 00 43</td>
<td>INITIALISE MEM. LOC. 4300H</td>
</tr>
<tr>
<td>42A2</td>
<td>DCR M</td>
<td>35</td>
<td>DECREMENT MEMORY CONTENT</td>
</tr>
<tr>
<td>42A3</td>
<td>INX H</td>
<td>23</td>
<td>INITIALISE MEM. LOC. 4301H</td>
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<tr>
<td>42A4</td>
<td>INR M</td>
<td>34</td>
<td>INCREMENT MEMORY CONTENT</td>
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<td>42A5</td>
<td>JMP LOOP</td>
<td>C3 6A 42</td>
<td>JUMP TO LOOP2</td>
</tr>
<tr>
<td>42A8 NEXT:</td>
<td>LXI H M</td>
<td>21 00 43</td>
<td>INITIALISE MEM. LOC. 4300H</td>
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<tr>
<td>42AB</td>
<td>INR M</td>
<td>34</td>
<td>INCREMENT MEMORY CONTENT</td>
</tr>
<tr>
<td>42AC</td>
<td>INX H</td>
<td>23</td>
<td>INITIALISE MEM. LOC. 4301H</td>
</tr>
<tr>
<td>42AD</td>
<td>DCR M</td>
<td>35</td>
<td>DECREMENT MEMORY CONTENT</td>
</tr>
<tr>
<td>42AE</td>
<td>JMP LOOP</td>
<td>C3 6A 42</td>
<td>JUMP TO LOOP</td>
</tr>
</tbody>
</table>

SUBROUTINE: 'DLY1'

<table>
<thead>
<tr>
<th>MEM. LABEL</th>
<th>MNEMONICS</th>
<th>OPCODE</th>
<th>COMMENTS</th>
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</thead>
<tbody>
<tr>
<td>LOC.</td>
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<td></td>
</tr>
<tr>
<td>42C0</td>
<td>DLY1: PUSH B</td>
<td>C5</td>
<td>PRESERVE DATA OF (BC) IN STACK</td>
</tr>
<tr>
<td>42C1</td>
<td>MVI B NNH</td>
<td>06 20</td>
<td>LOAD DATA 20H IN REG. B</td>
</tr>
<tr>
<td>42C3</td>
<td>DLY: NOP</td>
<td>00</td>
<td>NO OPERATION</td>
</tr>
<tr>
<td>42C4</td>
<td>NOP</td>
<td>00</td>
<td>NO OPERATION</td>
</tr>
<tr>
<td>42C5</td>
<td>DCR B</td>
<td>05</td>
<td>DECREMENT (REG. D)</td>
</tr>
<tr>
<td>42C6</td>
<td>JNZ DLY</td>
<td>C2 C3 42</td>
<td>JUMP ON NO ZERO TO NEXT</td>
</tr>
<tr>
<td>42C9</td>
<td>POP B</td>
<td>C1</td>
<td>RETRIEVE DATA OF (BC) FROM STACK</td>
</tr>
<tr>
<td>42CA</td>
<td>RET</td>
<td>C9</td>
<td>RETURN</td>
</tr>
</tbody>
</table>

141
5.9 CONCLUSION

This investigation evolves a new control technique to maintain constancy of speed of a DC shunt motor under load and/or supply voltage variation by controlling the applied voltage. The same control scheme may be utilised in controlling DC Series motor and may also be extended for an industrial sized motor with reduced voltage starting. The applied voltage has been controlled by controlling only the duty factor of the supply pulse by developing software based controller using intelligence of microprocessor. In traditional methods, the thyristors are used to amplify the pulses where firing of thyristors are generally controlled electronically. For forced commutation, additional circuitry is required which results in increasing the complexity of logical and hardware portion [39, 145, 146, 151]. To avoid these complexities, power transistor has been used for better switching and to overcome commutation problem. The software based controller (microprocessor) enhances the simplicity, reliability and adds maintenance free operation of the system within a reasonable cost.

During experiment, it has been found that, the microprocessor based controller efficiently regulates the speed of the motor for values of \( \varepsilon \) ranging from 0.2 to unity. With the change of size of the motor the lower limiting value of \( \varepsilon \) may change, which can be investigated from the experimental facts. It may be noted that, the motor is switched ON and OFF using the power transistor without creating any discontinuity in electrical conduction due to the presence of armature inductance.

This developed scheme has been used to regulate the speed of an experimental motor where the free wheeling diode has been avoided. For better performance during violent load variation in high powered motor, a free wheeling diode may be provided. The developed scheme is applied
to an experimental motor and can be applied to an industrial motor only replacing power transistor by a MOSFET due to its better power handling capability, heavy duty operation and low power loss in comparison to power transistor.