Chapter 1
Introduction

Aluminium served the integrated circuit (IC) fabrication industry as preferred material for interconnections for more than 30 years. Further development in scaling needed a breakthrough in the interconnection materials and deposition techniques. Speed and size requirements were such that copper emerged to be the right choice for interconnection material. There were several issues and advantages associated with copper that will be discussed in this chapter which lead it to be at the top of chart. Yet there were few drawbacks also that formed the basis of research for the diffusion barrier needed in case of copper metallization. This chapter will also introduce the mechanism of diffusion and criteria to select a material for barrier application. Many research groups have worked on the diffusion barriers using different materials and deposition techniques. Earlier work carried out by the researchers is summarized here. An overview of reasons for using copper and problems associated with it are presented.

1.1 Interconnection Issues in Integrated Circuits
Interconnections are the metal strips used to make connections among different transistors and circuits in an IC. Speed of an IC depends upon how fast these interconnections can convey the information from one point to another. In 1965 Intel’s co-founder, Gordon Moore, figured out the legendary Moore’s Law in Electronics magazine [1]. This law depicted that the number of transistors in a square inch of silicon doubles every 24 months. Later on this prediction was found correct although a slight deceleration down to 18 months occurred. After the first microprocessor that contained about 2,200 transistors, the progress has been tremendous. For example, Intel’s 8080 processor in 1974 contained 6,000 transistors, the first Pentium processor in 1993 contained 3,100,000 transistors and Pentium 4 in 2004 contained 125,000,000 transistors on the chip when the chip size was only 112 mm², which equals the size of a finger tip. As the industry moved towards 45 nm process technology node, CoreTM² quad-core processor comprises more than 500 million transistors. Such a transistor can be switched on and off approximately 300 billion times a second. Since the magnitude of these numbers is often very difficult to visualize, some simplifications are needed. For example:
- One could fit more than 2000 transistors (45 nm) across the width of a human hair
- 300 billion times a second means that one switch equals the time a beam of light travels a couple of centimetres.

Moore’s law was one of the major factors leading to the reducing costs in the IC manufacturing. The cost driven factors are also dominating when new process technologies are chosen for the IC manufacturing. Moore’s Law has led to increasing function density in the chip, defining the number of interconnected devices per chip area. As the minimum feature size of an IC decreases, the active device density increases. The device integration became more demanding because the area occupied by the interconnection lines on the chip surface extended more rapidly than the area needed to accommodate the active devices. Eventually, minimum chip area became interconnect-limited. At this point, continued shrinking of complementary metal-oxide semiconductor (CMOS) transistors produced less circuit-performance benefits. This dilemma was solved by a multilevel interconnection system in which the area needed by the interconnect lines is shared among two or more levels (figure 1.1).

![Figure 1.1 Cross-section of hierarchical scaling of MPU device [2]](image_url)

In 2010, the functional density of active devices in microprocessor unit (MPU) was so high that the number of metal levels was expected to be 12 [2]. Furthermore, because there were
more gates, a larger number of connections between gates must be made and the average length of the interconnection lines will increase. Total length of interconnects in MPU is expected be over 2 km/cm² when global wires are excluded. As in all process steps, the cost impact of the multilevel metallization scheme had to be carefully considered. Although it made possible to manufacture more dies per wafer and reducing the cost per chip in that manner, it brought additional cost factors for the development, manufacturing and the device reliability. For example:

- New materials had to be used comprising significant R&D work
- Process challenges meant some negative impact to the manufacturing yield
- New failure modes such as electromigration, corrosion and hillock formation was expected to influence the circuit reliability

The question was whether the chip-size reduction and enhanced chip value will produce a margin of profit that is greater than the amount lost due to additional incurred process costs and yield and reliability loss. Evidently, the multilevel metallization scheme became cost-effective and successful.

It was found obvious that the increasing length of interconnects was leading to the increase in the resistance times capacitance (RC) time delay of interconnects and in sub-quarter-micron device nodes the propagation delay passed the intrinsic delay that comprises the MOS transistor delay. Figure 1.2 gives the glimpse of this scenario. As shown in figure, with the decreasing feature size the gate delay also decreases while interconnection delay increase and became the dominating one in total delay. Cu + low κ system follows the same trend but magnitude is quite lesser than Al + SiO₂ system. Response of the devices is set to a limit by the RC delay occurring due to the resistance and capacitances associated with these interconnections.

Any metal strip has resistance defined by the relations:

$$ R = \rho L/A \quad (1.1) $$

This relations shows that a decrease in the cross sectional area and an increase in the length of a metal strip eventually increases its resistance. Resistance also depends upon the resistivity of the material being used for interconnections.
Capacitance comes into action as these metal strips run over dielectric materials such as SiO$_2$, forming a capacitor like circuit. This capacitance is given by:

$$C = \kappa A/t$$  \hspace{1cm} (1.2)

So capacitance value depends upon the dielectric material and its thickness. To stay tuned with Moor’s law it was desirable to decrease the device size so that number of transistors in the same area could be doubled after each 18 months. There were two ways to tackle this situation. First to reduce resistance of interconnects and second to decrease the capacitance. As there must be continuous reduction in metal strip cross sectional area and increment in its length so the only way to achieve less resistance was to select low resistivity interconnection material. Capacitance could be decreased by using low $\kappa$ dielectric materials. The overall situation was demanding a change in both interconnection and dielectric materials. So the search for the alternate options was started.

### 1.2 Copper Interconnects

The multilevel metallization was facing new challenges that required major changes in materials and the process flow. Minimization of the RC delay forced a transition from aluminium-copper (Al-Cu), tungsten (W) and silicon dioxide (SiO$_2$) based interconnects to the Cu metal and the low-dielectric constant ($\kappa$) insulator metallization scheme. In addition to the RC delay, conventional aluminium metallization was facing overwhelming challenges.
because aluminium is sensitive for electromigration [3], also known as “electron wind effect”. When the current density increases, aluminium atoms can move in the lattice and cause severe device failures such as voids and hillocks [4]. In the worst case, the wire will be open or shorting with other wire. Alternative metals such as tungsten, silver and gold were considered since they have better electromigration properties. However, tungsten has about twice as high electrical resistivity than pure aluminium and gold and silver have high cost. Copper metal was found to be an attractive option because of its high electromigration resistance and low bulk resistivity (1.7 μΩcm versus 2.7 μΩcm for aluminium). Surely it was one of the main requirements and copper fulfilled it. After all, one of the most important reasons for a successful breakthrough of the copper metallization was the great progress achieved in the process development of robust and cost effective copper deposition and patterning. When the hunt for a suitable material begun, copper emerges out to be the best one replacing aluminum. Other properties are compared in the table 1.1 with other candidates.

Table 1.1: Comparison of properties of low resistivity materials [5]

<table>
<thead>
<tr>
<th>Metal</th>
<th>At. Wt.</th>
<th>Density (20°C) (g/cm³)</th>
<th>Melt. Point (°C)</th>
<th>Heat capacity (25°C) J/(kg.K)</th>
<th>Thermal exp. coef. (20° C) (10⁻⁶ K⁻¹)</th>
<th>Electrical Resistivity (20°C) (10⁻⁶ W.cm)</th>
<th>Thermal Conductivity (W/(m.K))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminium</td>
<td>26.98</td>
<td>2.702</td>
<td>660.46</td>
<td>902.1</td>
<td>23.03</td>
<td>2.62</td>
<td>238</td>
</tr>
<tr>
<td>Copper</td>
<td>63.54</td>
<td>8.92</td>
<td>1084.9</td>
<td>385.2</td>
<td>16.6</td>
<td>1.69</td>
<td>416</td>
</tr>
<tr>
<td>Gold</td>
<td>196.97</td>
<td>19.3</td>
<td>1064.4</td>
<td>127.5</td>
<td>14.2</td>
<td>2.4</td>
<td>311</td>
</tr>
<tr>
<td>Silver</td>
<td>107.87</td>
<td>10.5</td>
<td>961.93</td>
<td>236.3</td>
<td>18.9</td>
<td>1.62</td>
<td>417</td>
</tr>
<tr>
<td>Tungsten</td>
<td>183.86</td>
<td>19.25</td>
<td>3422</td>
<td>132</td>
<td>4.5</td>
<td>5.65</td>
<td>174</td>
</tr>
</tbody>
</table>

Thus it’s obvious from the table that aluminium was the best until resistivity issues comes in. Besides having low resistivity copper has high melting point, less TEC and more thermal conductivity too. All these factors made it easy to trade off copper into the fabrication line. Though it seems that copper would have solved all the interconnection problems but it was not so simple to use it. There are shortcomings while using copper as interconnection material. These are listed below:
- Copper is prone to be oxidized due to the unavailability of passivation layer like in case of aluminium
- It diffuses into SiO₂ and low κ dielectrics at higher temperature and under bias too
- Copper reacts with silicon and forms copper silicide after annealing at 200 °C
- It has poor adhesion with dielectrics
- Difficulty in dry etching

Copper is difficult to pattern/etch using dry etching. This disadvantage could change the game and copper might not have been used for metallization despite of its several advantages as this fact could make it hard for existing fabrication process to adopt copper. But fortunately damascene process opened the new doors for patterning the copper. The *American Heritage Illustrated Encyclopedic Dictionary* defines *damascene* as a native inhabitant of Damascus (*Damaskus*), which is a major city in the north-west of Syria. The word *Damask* means patterned silk fabrics woven in Damascus, a city notable for manufacturing and shipment of damascened steel sword blades, which were exceptionally hard and resilient. In French, damascene is *damas quiner* means to decorate in the manner of Damascus blades or steel from Damasquine of Damascus. Thus the word *damascene* can be taken literally as the process of decorating a metal with wavy patterns of gold or silver. However, in ICs the *damascene process* means an elegant technique of inlaying metal (copper) for interconnect which avoids the complicated process of metal etching [6]. Figure 1.3 shows the cross-section of an interconnect structure created by: (a) the subtractive conventional process and (b) Cu-damascene process.

Steps involved in a simple Cu damascene process are as follow:

- First of all the dielectric is deposited
- The dielectric is etched according to the defined photoresist pattern and then barrier layer is deposited
- Next, copper is deposited using any suitable deposition technique like electroplating etc. (Optimum way of copper deposition is Copper electrodeposition which is a two step process. In the first step seed layer is deposited on the wafer using physical vapour deposition (PVD) and then copper is electroplated. That is why seed layer is shown in the figures.)
- Finally, the surface is planarized using chemical mechanical polishing (CMP)
RC delay could be reduced by using low resistivity material for interconnection and low k dielectric materials. Copper could be a material of choice because of low resistivity but at the same time it has several issues with SiO₂ and low κ dielectrics. The drawbacks of copper initiated new area of research that explored various techniques and material to make copper the metal of choice for interconnections in ICs.

### 1.3 Diffusion Barriers

Since copper is a fast diffuser in silicon and low k dielectrics hence a barrier is needed in between copper and silicon or between copper and dielectric that can prevent interaction between copper and silicon or dielectric. This barrier is known as “Diffusion Barrier”. It would be better if same barrier will promote the adhesion too. The concept of the use of barrier layers in metallization systems is simple: two materials that have unfavourable chemical interaction are kept separate by an intermediate layer. Such a barrier should posses several features, which include [7, 8]:

1. If the barrier layer X separates materials A and B, the barrier should be thermodynamically stable when in contact with both A and B.
2. X should prevent harmful interdiffusion between A and B. Thus, diffusivity of both materials A and B in barrier layer should be as low as possible.
3. The barrier layer should form low resistance contacts with both materials A and B and be at least a reasonable thermal conductor. The resistivity of the barrier layer itself is usually not
too significant up to a certain point [9] because of its small thickness compared to that of the materials A and B. 

(4) X should adhere well to all materials used in the metallization scheme. 

(5) The material X should not have an electrochemical potential very different from that of A and B in order to avoid the formation of galvanic corrosion cells with the metallization layers. 

(6) Stresses of around GPa are expected to exert significant effects upon thin-film diffusion processes [10]. Therefore, stresses in the barrier material should not be too high. 

As can be seen from the list of requirements, compromises are often needed and some contradictions cannot be avoided. In addition to the physicochemical demands, also process conditions related to step coverage, capability of selective patterning, reasonable rate and ease of deposition and so on, must be fulfilled in order to have a satisfactory diffusion barrier. 

Practical diffusion barriers are generally divided into (i) sacrificial barriers, (ii) stuffed barriers and (iii) amorphous diffusion barriers [8] as shown in figure 1.4. 

Figure 1.4 Types of barriers 

The idea of sacrificial barrier is that the intermediate layer X reacts either with one or both of the materials A and B in a laterally uniform manner with characterized reaction rates. The effectiveness of the barrier is determined by the reaction rate. As long as the intermediate layer is not completely consumed in the reactions, the separation between the materials A and B is still effective. Therefore, reaction rate between X and A or/and B should not be too high in order to have effective barrier layer. This definite lifetime is also the major limitation of
sacrificial barriers. For a more permanent protection the barrier layer X should be thermodynamically stable against A and B. This means that there are no driving forces for reactions at the interfaces A/X and X/B. This is necessary but not sufficient condition for a stable diffusion barrier. It is also necessary to stop or reduce diffusion of A and B across X via short-circuit paths, since there is still a driving force for A to diffuse into B and vice versa. This can be achieved either by eliminating the short-circuit paths or filling the easy paths with appropriate atoms/molecules and thereby prevent the short circuit diffusion of A and B [8]. The second approach leads to the concept of stuffed barrier. When atoms of A and B cannot use the short-circuit paths (they are now occupied by the atoms or molecules introduced there on purpose) diffusion is slowed down generally by several orders of magnitude. The elimination of short-circuit paths can also be achieved by removing the easy paths (i.e. grain boundaries) by making the structure of the barrier amorphous. It is emphasized that amorphous layers are metastable and will eventually crystallize. When crystallization takes place, grain boundaries are again present in the barrier. Thus, crystallization temperature of amorphous layer is of critical importance. The barrier should meet certain requirements to be suitable for use. Few are listed below:

- It should be as thin as possible
- Should not react with copper
- Should not produce any strain in the metallization
- Easy to be deposited
- Should be compatible with existing fabrication process
- Cost effective

Various transition metals, their binary and ternary compounds have been suggested for the copper barrier application. The compounds of W, Ta and Ti are the most studied comprising desirable physical, chemical and electrical properties.

1.4 **Diffusion through thin films**

In order to develop diffusion barrier, it is necessary to understand the diffusion mechanism of copper in thin films. It is known that atomic migration takes place to establish equilibrium when different atoms are placed together. It is typically due to concentration differences, existence of a negative free energy, applied electric field, thermal energy and generation of a strain gradient or any combination of these factors [11]. Atomic migration results in a
diffusion flux, with the net flow of atoms being characterized by a diffusion coefficient $D$. The latter is described by Fick’s law:

$$J = -D \frac{dC}{dx} \quad (1.3)$$

Where

$C$: atomic concentration
$J$: the atomic flux per unit area per second
$x$: distance

The diffusion coefficient $D$ is temperature dependent and can be described using an Arrhenius relationship:

$$D = D_0 \exp\left(-\frac{Q}{K T}\right) \quad (1.4)$$

Where

$D_0$ is a constant,
$Q$: the activation energy for diffusion
$K$: Boltzmann’s constant
$T$: temperature in degrees Kelvin

Hence defects in the barrier layers can be quantified for diffusion using parameters $D_0$ and $Q$. Dominating mechanisms of diffusion barrier failure are as follows:

- Diffusion of copper or substrate/base atoms in barrier layer
- Diffusion of copper along grain boundaries
- Failure due to chemical reaction of barrier material with copper or substrate

Vacancies and dislocations are two types of bulk defects that contribute to diffusion. Rate of diffusion is different through vacancies, defects and grain boundaries. It was experimentally observed that lattice diffusion rates are proportional to the absolute melting temperature $T_m$ of the host material, with the corresponding behaviour being given by the following relationship [12]:

$$D \sim A T_m \quad (1.5)$$

where $A$ is proportionality constant that depends on a variety of factors, including lattice structure and type of material.

Diffusion due to atom-vacancy exchange is the slowest diffusion while diffusion through dislocations exhibit intermediate rates. When there is mismatch between adjoining grains, it
results in high-angle grain boundaries which have the highest diffusion rates. This discussion clearly highlights the critical role that microstructure plays in the resulting diffusion barrier performance of the barrier material. Film microstructure can be categorized as single crystal, polycrystalline, nano-crystalline (i.e. polycrystalline with grain size below 5 nm) and amorphous as shown schematically in figure 1.5.

![Figure 1.5 Different structures of barrier film](image)

There are more chances of grain mismatch in case of polycrystalline barrier films. Polycrystalline barriers tend to yield the poorest barrier performance and are thus the least desirable for diffusion barrier applications. This assessment is especially true for barriers with grain sizes on the order of film thickness or films with columnar structure. The latter exhibit grain boundaries that extend throughout the entire film thickness and are mostly normal to the substrate surface, as shown in figure 1.5 c, thus providing an effective pathway for copper diffusion. Though single crystal barriers are ideal yet the cost factor and the complications in deposition techniques make it hard to use [13]. Hence the choice is left as nano-crystalline or
amorphous barrier layer as small and complex structure at grain boundaries can result in better barrier performance due to less space available at boundaries for diffusion to occur.

Barrier failure is most affected by the following properties of barrier:

- Chemical reaction of barrier material with copper or substrate material
- Density
- Crystalline structure of barrier layer

Barrier material must not react with copper or the underlying substrate under any type of stress i.e. thermal, mechanical, electrical or any combination of these. Such stress conditions are normally encountered by the ICs while processing and/or operation. Packing of deposited barrier layer should be as close as possible to achieve higher density to prevent void formation, defects and loosely packed grain boundaries. In this way due to the non availability of diffusion paths, diffusion will be eliminated. Smaller is the molecular size of barrier layer lesser will be the grain boundary diffusion paths.

From the above discussion it can be concluded that barrier material must satisfy the following specifications before it can be used:

- High thermal and structural stabilities
- Adequate adhesion to adjacent layers
- Excellent surface coverage and packing density
- Should provide smooth surface for subsequent Cu conductor layer deposition
- Resistant to thermal, mechanical and electrical stresses
- Fair thermal and electrical conductivities
- Low contact resistance
- Compatibility with integrated circuit fabrication flows
- Deposition within the thermal limitations of microelectronics processing
- Non-reactive and zero cross contamination with existing materials in process flow

1.5 History of Barriers

It is evident from the discussion till now that in order to use copper as interconnect material there is an unavoidable need of diffusion barrier. Plenty of research has been conducted on different materials and deposition techniques in the past. Generally metals or compounds with high melting point are suitable for barrier application because of less chance of having grain
boundaries, which are the fastest diffusion pathways. Hence refractory materials seem to be the best choice due to their high melting temperature and suitable resistivity. Various refractory metals and their binary and ternary compounds have been investigated for such applications [14].

Initially Ti, Ta and W were tried as diffusion barrier as these were being used for aluminum already. Later on due to the different nature of Cu from Al and demand of thinner layers raised the need of new materials to be explored. Table 1.2 summarize the earlier studies on with Si/Barrier/Cu structure along with the failure temperatures and probable mechanism of failure. This table is mainly extracted from the work of Shi-Qing Wang et al. in 1993 [15] and some other surveys.

<table>
<thead>
<tr>
<th>Sample structure (nm)</th>
<th>Annealing ambient</th>
<th>Failure Duration (min) /temperature (°C)</th>
<th>Mechanism</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Ti&lt;sub&gt;55&lt;/sub&gt;N&lt;sub&gt;45&lt;/sub&gt;(95)/Cu(175)</td>
<td>N&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.5/700</td>
<td>Cu&lt;sub&gt;2&lt;/sub&gt;Si formation</td>
<td>16</td>
</tr>
<tr>
<td>Si/Ti&lt;sub&gt;45&lt;/sub&gt;N&lt;sub&gt;55&lt;/sub&gt;(120)/Cu(175)</td>
<td>N&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.5/900</td>
<td>Cu&lt;sub&gt;2&lt;/sub&gt;Si formation</td>
<td>16</td>
</tr>
<tr>
<td>Si/TiN&lt;sub&gt;0.95&lt;/sub&gt;(50)/Cu(65-200)</td>
<td>Vacuum</td>
<td>60/600</td>
<td>degradation at higher temperature, earlier for Si/TiN/Cu than for Si/TiN(O)/Cu</td>
<td>17</td>
</tr>
<tr>
<td>Si/TiN&lt;sub&gt;1.3&lt;/sub&gt;O&lt;sub&gt;0.75&lt;/sub&gt;(50)/Cu(65-200)</td>
<td>Vacuum</td>
<td>60/600</td>
<td></td>
<td>17</td>
</tr>
<tr>
<td>Si/Ti&lt;sub&gt;52&lt;/sub&gt;N&lt;sub&gt;48&lt;/sub&gt;(55, Sputtered)/vent/Cu(250)</td>
<td>Vacuum</td>
<td>30/700</td>
<td>Small Cu-Si nodules formation</td>
<td>18</td>
</tr>
<tr>
<td>Si/TiN(60, CVD)/Cu(250)</td>
<td>Vacuum</td>
<td>30/550</td>
<td>Small Cu-Si nodules formation</td>
<td>18</td>
</tr>
<tr>
<td>Si/TiN(40-60, CVD)/Cu(250)</td>
<td>Vacuum</td>
<td>30/ &lt;500</td>
<td>Cu-Si compounds formation</td>
<td>18</td>
</tr>
<tr>
<td>Si/W&lt;sub&gt;76&lt;/sub&gt;N&lt;sub&gt;24&lt;/sub&gt; (120, amorphous)/Cu(620)</td>
<td>Vacuum</td>
<td>30/750</td>
<td>W&lt;sub&gt;5&lt;/sub&gt;Si&lt;sub&gt;3&lt;/sub&gt; formation</td>
<td>19</td>
</tr>
<tr>
<td>Configuration</td>
<td>Process</td>
<td>Temperature</td>
<td>Time</td>
<td>Notes</td>
</tr>
<tr>
<td>-------------------------------------</td>
<td>---------</td>
<td>-------------</td>
<td>------</td>
<td>-------</td>
</tr>
<tr>
<td>Si/W_{46}N_{54}(120, polycrystalline/Cu(620))</td>
<td>Vacuum</td>
<td>30/750</td>
<td></td>
<td>W_{3}Si_{3} formation</td>
</tr>
<tr>
<td>Si/Ti/Cu</td>
<td>Vacuum</td>
<td>…</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/Ti(220)/TiN(100)/Cu(160)</td>
<td>Vacuum</td>
<td>30/700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/TiN(100)/Cu(160)</td>
<td>Vacuum</td>
<td>30/700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/W_{2}N(150)/Cu(50-100)</td>
<td>He</td>
<td>30/500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/Ta(50)/Cu(100)</td>
<td>He</td>
<td>3 °C/min to 660</td>
<td></td>
<td>Ta out-diffuses to Cu surface before any interaction</td>
</tr>
<tr>
<td>Si/Ta(20)/Cu(150)</td>
<td>Ti purified</td>
<td>320</td>
<td></td>
<td>diffusion of Cu through Ta</td>
</tr>
<tr>
<td>Si/Pd(100)/Cu(200)</td>
<td>N₂:H₂ = 9:1</td>
<td>30/200</td>
<td></td>
<td>Reaction at 300</td>
</tr>
<tr>
<td>Si/W(100)/Cu(200)</td>
<td>Vacuum</td>
<td>…</td>
<td></td>
<td>Cu diffuses through W</td>
</tr>
<tr>
<td>Si/Cr(20)/Cu(200)</td>
<td>Vacuum</td>
<td>…</td>
<td></td>
<td>Limited Cu diffusion in Si</td>
</tr>
<tr>
<td>Si/W(500)/Ta(80)/Cu(200)</td>
<td>Vacuum</td>
<td>30/450</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/W(50)/Cu</td>
<td>…</td>
<td>…/500</td>
<td></td>
<td>Reaction at 600</td>
</tr>
<tr>
<td>Si/Ta(180)/Cu(260)</td>
<td>Vacuum</td>
<td>30/600</td>
<td></td>
<td>TaSi₂ and Cu₃Si formation</td>
</tr>
<tr>
<td>Si/α-Ta₇₄Si₂₆(100)/Cu(360)</td>
<td>Vacuum</td>
<td>30/600</td>
<td></td>
<td>Cu induced crystallization of Ta₇₄Si₂₆ film</td>
</tr>
<tr>
<td>Si/α-Ta_{36}Si_{14}N_{50}(120)/Cu(280)</td>
<td>Vacuum</td>
<td>30/900</td>
<td></td>
<td>Ta_{36}Si_{14}N_{50} crystallizes</td>
</tr>
<tr>
<td>Si(shallow junction)/Ta_{36}Si_{14}N_{50}(120)/Cu(500)/Ta_{36}Si_{14}N_{50}(20)</td>
<td>Ar</td>
<td>1000 H/350</td>
<td></td>
<td>Barrier fails after 650 H at 450 °C</td>
</tr>
<tr>
<td>System</td>
<td>Process</td>
<td>Temperature</td>
<td>Result</td>
<td>Notes</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>---------</td>
<td>-------------</td>
<td>---------------------------------------------</td>
<td>------------------------</td>
</tr>
<tr>
<td>Si/α-TiP_{2}(80)/Cu(250)</td>
<td>Vacuum</td>
<td>30/600</td>
<td>Failed structurally and electrically at</td>
<td></td>
</tr>
<tr>
<td>Si/TiSi_{2}(40)/α-TiP_{2}(80)/Cu(250)</td>
<td>Vacuum</td>
<td>30/700</td>
<td>Failed both structurally and electrically</td>
<td></td>
</tr>
<tr>
<td>Si/α-W_{72}Si_{18}(2000)/Cu(105)</td>
<td>Vacuum</td>
<td>60/750</td>
<td>Crystallizes at</td>
<td></td>
</tr>
<tr>
<td>Si/α-Ni_{60}Nb_{40}(500)/Cu(100)</td>
<td>Vacuum</td>
<td>60/600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/α-W_{85}Si_{15}/Cu</td>
<td>…</td>
<td>60/600</td>
<td>Barrier crystallizes at</td>
<td></td>
</tr>
<tr>
<td>Si/Ni_{57}Nb_{42}/Cu</td>
<td>…</td>
<td>…</td>
<td>Cu diffuses in NiNb, replacing Nb at</td>
<td></td>
</tr>
<tr>
<td>Si/W_{85}Si_{15}/Cu</td>
<td>…</td>
<td>60/600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si/Ni_{60}Mo_{40}/Cu</td>
<td>…</td>
<td>…</td>
<td>60/500</td>
<td></td>
</tr>
<tr>
<td>Si/α-Ir_{45}Ta_{55}(30)/Cu(50)/α-Ir_{45}Ta_{55}(30)</td>
<td>Vacuum</td>
<td>30/700</td>
<td>Cu diffuses in Si at 30/800</td>
<td></td>
</tr>
<tr>
<td>Si/PtSi/Ta(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/200</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/Ta(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/300</td>
<td>Reaction at 30/400</td>
<td></td>
</tr>
<tr>
<td>Si/PtSi/Cr(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/200</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/PtSi/Ti(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/200</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/PtSi/W(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/200</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/PtSi/α-C(100)/Cu(200)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>30/200</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/TiSi_{2}/Ta(20)/Cu(200)/Ta(30)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>…</td>
<td>Reaction at 30/400</td>
<td></td>
</tr>
<tr>
<td>Si/TiSi_{2}/W(200)/Cu/Ta(30)</td>
<td>N_{2}:H_{2} = 9:1</td>
<td>…</td>
<td>Reaction at 30/300</td>
<td></td>
</tr>
<tr>
<td>Si/\text{TiSi}_2/\text{Ti}(25)/\text{TiN}(25)/\text{Cu}/Ta(30)</td>
<td>N_2:H_2 = 9:1</td>
<td>30/400</td>
<td>Reaction at 30/400</td>
<td>43</td>
</tr>
<tr>
<td>Si/\text{TiSi}_2/\text{Ti}/\text{TiN}/W/Ta/Cu/Ta</td>
<td>N_2:H_2 = 9:1</td>
<td>30/600</td>
<td>Reaction at 30/600</td>
<td>43</td>
</tr>
<tr>
<td>Si/\text{CoSi}_2/\text{TiN}_x(50)/\text{Cu}</td>
<td>Vacuum</td>
<td>30/600</td>
<td></td>
<td>44</td>
</tr>
<tr>
<td>Si/\text{CrSi}_2/\text{TiN}_x(50)/\text{Cu}</td>
<td>Vacuum</td>
<td>30/600</td>
<td></td>
<td>44</td>
</tr>
<tr>
<td>Si/\text{TiSi}_2/\text{TiN}_x(50)/\text{Cu}(50)</td>
<td>Vacuum</td>
<td>30/600</td>
<td></td>
<td>44</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{33}\text{C}</em>{47}(25)/\text{Cu}(100) A</td>
<td>5%\text{H}_2/\text{N}_2</td>
<td>30/750</td>
<td>TaSi_{2} and copper silicide formation</td>
<td>45</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{33}\text{C}</em>{47}(5)/\text{Cu}(100)</td>
<td>5%\text{H}_2/\text{N}_2</td>
<td>30/600</td>
<td></td>
<td>45</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{40}\text{C}</em>{60}(25)/\text{Cu}(100)</td>
<td>5%\text{H}_2/\text{N}_2</td>
<td>30/700</td>
<td>TaSi_{2} and Cu_{3}Si formation</td>
<td>45</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{20}\text{C}</em>{80}(25)/\text{Cu}(100)</td>
<td>5%\text{H}_2/\text{N}_2</td>
<td>30/500</td>
<td>Cu_{3}Si formation</td>
<td>45</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{34}\text{N}</em>{46}(25)/\text{Cu}(100)</td>
<td>5%\text{H}_2/\text{N}_2</td>
<td>30/800</td>
<td></td>
<td>46</td>
</tr>
<tr>
<td>Si/\text{Ta}(12,5)/\text{Zr}(5)/\text{Ta}(12,5)/Cu(100)</td>
<td>Vacuum</td>
<td>30/775</td>
<td>Cu_{3}Si formation</td>
<td>47</td>
</tr>
<tr>
<td>Si/\text{Ta}<em>{43}\text{Si}</em>{4}\text{N}_{53}(30)/\text{Cu}(100)</td>
<td>Ar-H_2 (10%)</td>
<td>60/800</td>
<td>TaSi_{2} and Cu_{3}Si formation</td>
<td>48</td>
</tr>
</tbody>
</table>

From the data provided in the table it can be concluded that refractory metals, such as Ti, Ta and W as well as their binary nitrides and carbides and ternary SiN are the most studied materials. Also TaN and compound of TaNSi are the most viable diffusion barriers because of comparative stability at higher temperatures. TaN and TaNSi are stable up to 700-800 °C whereas other material survive up to 500-600 °C only. That is why Ta and TaN based diffusion barriers became the first choice of the industry. Tantalum has several advantages from the diffusion barrier point of view. It has a high melting point (3020 °C) and therefore expected to have high activation energy for both lattice and grain boundary diffusion. It does not form inter-metallic compounds with copper and thus provides a stable interface between copper and tantalum. The reaction between silicon and tantalum is also known to require quite high temperatures (650 °C) [49], in this way providing a reasonably stable Si/Ta interface.
Apart from the literature listed in the table 1.2, the work carried out by other researchers is discussed here. Chen and Liu [50] tried Mo and Zr as barrier material. ZrC is an advanced ceramic due to superior covalent properties such as excellent mechanical stability, high melting point, lower work function, great hardness and metallic behavior electrically and optically. The study showed that reactively sputtered ZrC results in a nanocrystalline ZrC. Although amorphous barrier is much preferred due to the lack of grain boundaries, nanocrystalline ZrC showed performance comparable to TaN. Cu diffusion into Si substrate along the localized defects in the barrier film caused the barrier failure of 150-200 nm thick ZrC at 800 °C forming ZrSi$_2$. 100 nm thick TaN was reported to fail at 700 °C [51]. Zr ternary compounds are of interest as the reaction temperature of Zr with Si (700 °C) is higher than that of Ta with Si (650 °C). Song et al. [52] showed that 100 nm of ZrSiN was stable even at 850 °C from the diffusion of copper and other elements. However, this study was done on material thickness significantly higher than the Ta ternary compound, thus inhibits comparison with TaSiN. Although amorphous ternary barriers discussed above exhibit superior performance as diffusion barriers, they possess significantly high resistivity, which is highly undesirable. The need for high conductivity and thermal stability prompted studies of amorphous alloy diffusion barrier. Fang et al. investigated sputtered binary alloy to form amorphous thin film with crystallization resistant and conductive diffusion barrier. Amorphous (20 and 50 nm) TaNi film with resistivity of 169.7 μΩcm prepared by DC magnetron sputtering was able to prevent the formation of intermetallic compounds up to 700 °C. It was found that higher Ta content in TaNi films increases barrier effectiveness as they exhibit superior glassy behavior [53]. Similar works involving TaCo and TaFe have shown potential promise. TaCo and TaFe exhibit similar results with resistivities of 146.82 and 247.01 μΩcm, respectively. Stacked Si/Ta$_{0.5}$Fe$_{0.5}$/Cu and Si/Ta$_{0.5}$Co$_{0.5}$/Cu failed at temperatures of 650 and 700 °C, respectively [54]. Failure of the amorphous alloys was triggered by its dissociation and reaction with underlying silicon substrate.

All the barrier materials discussed so far made the use of conventional deposition techniques like sputtering, PVD, CVD etc. But with the further decrease in device dimensions need of continuous exploration of new materials and techniques is required. Many groups have done experiments with new deposition technique, Self Assembly. This technique is simple and uses no special equipment. Caro et al. [55] studied self assembled barrier of APTMS and found it stable up to 500 °C with the advantage of monolayer thickness. A. Krishnamoorthy and co-workers [56] also tried self assembled monlayers of different precursors and characterize the
barrier thermally and electrically. The results showed that the monolayers are capable of good coverage with monolayer thickness. Another technique explored by the researchers is electroless deposition. Yoshino et al. [57] reported that thin film of NiB, deposited using electroless deposition technique, could prevent copper diffusion into SiO$_2$/Si substrate up to 400 °C. Choi et al. [58] found NiP layer as a better option than NiB. Electroless deposited CoWP films have been found to be effective diffusion barriers even after annealing at 500 °C [59]. Nakano et al. [60] showed the usefulness of CoWB as barrier at 400 °C. CoWP was demonstrated as barrier up to 450 °C by Khon et al. [61]. NiCoP showed the stability as barrier up to 500 °C [62]. All these unconventional deposition materials and techniques have the potential to replace the existing barrier technology.

A detailed review of different materials with their deposition techniques is provided in the next chapter.

1.6 Motivation behind present work

From the previous section it can be found that though Ta and TaN based barriers are most suitable still there is demand of new materials and deposition techniques. According to international roadmap for semiconductors (ITRS) 2012, the barrier layer should be 1-2 nm thick by 2016 [63]. To take full advantage of the copper metallization, barriers with molecular thickness are required. Molecular thickness brings the challenge of proper coverage of substrate by barrier film along with sufficient density to prevent the diffusion through it. The barrier thickness must not be compromised with cost and effectiveness. Also the compatibility with existing IC technology is a must to reduce the overall cost and investment. Hence there are several unavoidable challenges associated with new barrier materials and techniques. Taking these facts into account our group started working on the thin diffusion barriers. Early members of the group studied electroless diffusion barriers, plasma enhanced barriers and sputtered deposited barriers of different materials [62, 64-66]. Present work is solely dedicated to ultrathin barriers with monolayer thickness. Self assembly technique is characterized first. In the second phase Langmuir-Blodgett technique is explored to deposit diffusion barriers. Barriers deposited over both SiO$_2$/Si and Si substrates were studied. Standard structural and electrical characterizations are done to evaluate the present work to meet the present demand.
1.7 Outline of the present work

Importance of diffusion barrier has been discussed previously. The aim of present work is to study monolayer thickness barriers for copper metallization. Two approaches for monolayer deposition were studied:

- Self assembly technique
- Langmuir-Blodgett (LB) technique

Diffusion barrier of 3 aminopropyletrimethoxysilane (3-APTMS) was deposited using self assembly and Co, NiO and CoNiO monolayers were deposited using LB technique. LB technique deposited monolayers were studied as diffusion barrier over both Si and SiO₂/Si substrates. Characterization was carried out using XPS, EDS, SEM, AFM, CV analyzer, IV plots, XRD and Four probe resistivity technique.

1.8 Chapter wise layout of the thesis

Chapter 1 Introduction

This chapter provides the information related to interconnects and issues associated with them that lead to the need of the diffusion barrier. Benefits of copper over other candidates are discussed. Some desirable characteristics of diffusion barrier are mentioned. Diffusion mechanism of copper is discussed. Historical development of different barrier materials developed by various research groups is also described. In the end, motivation behind current research is discussed with the help of future roadmap. Outline of the research work carried out is provided at the end of the chapter.

Chapter 2 Literature Survey: Evolution of Diffusion Barriers

In this chapter, historical development of different barrier materials and deposition techniques developed by various research groups is described. Chapter is organized according to the barrier materials. Attention is paid to include all the materials and techniques available in the literature.

Chapter 3 Deposition and Characterization Techniques

Various experimental setups and techniques used to deposit monolayers and characterize their structural and electrical properties as diffusion barriers are described here. The experimental setups are explained. The chapter describes the techniques to check the presence of a barrier and evaluate its capability using different tools available.
Chapter 4  SAM Diffusion Barrier on SiO$_2$/Si substrate

In this chapter self assembly approach is described to deposit 3-APTMS barrier along with experimental procedure included. The results obtained from different characterization techniques are discussed in detail.

Chapter 5  LB Diffusion Barriers on SiO$_2$/Si substrate

LB technique is described to deposit Co, NiO and CoNiO monolayers for barrier application in this chapter. Experimental procedure and setup requirements are mentioned. Experimental procedure and results of LB technique deposited barriers over SiO$_2$/Si surface are discussed.

Chapter 6  LB Diffusion Barriers on SiO$_2$/Si substrate

In this chapter also, LB technique is described to deposit Co, NiO and CoNiO monolayers for barrier application, but on Si substrate only. Experimental procedure and setup requirements are presented along with the results.

Chapter 7  Conclusion and Future Scope

All the experimental results are concluded here in nut shell to present the main findings of the research work. The future scope of this work in the same research area as well as in different areas are provided in this chapter.
References

[62] Anuj Kumar, Mukesh Kumar and Dinesh Kumar, Microelectronic Engineering, 87 (2010) 387