ABSTRACT

Wide spread of handy electronic devices and the advances in VLSI technology have enabled the implementation of complex digital circuits in a single chip. Digital circuits consist of a number of interconnected logic gates which together perform logical operations with many input signals. In recent years, in deep submicron and low power VLSI design, power dissipation and area have become a critical parameter.

The main cause of power dissipation is due to charging and discharging of internal node capacitance during transition activity. Power dissipation is the most critical parameter in hand held and mobile devices. It is classified into two types namely static or leakage power dissipation and active or dynamic power dissipation. Static power dissipation is caused by leakage current and other static components. Dynamic power dissipation is caused by charging and discharging of inter node capacitance.

In a typical chip 10% of power is consumed by static power dissipation and 90% of power is consumed by dynamic power dissipation. As static power dissipated is in nanowatts, only dynamic power dissipation is considered here. The research work analyze an efficient method to transmit huge number of data through interconnect with reduced transition activity, area and power dissipation.

To reduce coding complexity and effective data transmission, the input data are initially compressed to the required bit level. Then the compressed data are analyzed whether the transition (Switching activity) is in an acceptable level or not and if the transition is in an acceptable level then

the information is transmitted to the output bus. Else the data are coded using multi coding technique.

Hamming distance estimator is used to estimate number of transition that occurs in each coding method during data transmission, within and between the buses. Comparator then compares and selects the coding method that has the least transition activity among all and that selected coding method is transmitted via buses for further process.

Data compression is an efficient technique to represent information in a compact form. In multimedia applications such as text or message transmission the number of bytes required to represent the data can be very large. The speed of transmission also depends on the number of bits transmitted. Data compression is classified into lossy and lossless. Lossy compression cannot reconstruct the original data effectively. But in text data reconstruction the originality is very important. To overcome the effects of lossy compression this research work implements a simple byte lossless text compression technique. The results are analyzed and compared with different lossless compression methods.

To reduce the transition activity compressed data can be coded using multi coding technique. Eight different coding techniques are applied to the same set of data. Each coding techniques are identified by 3 bit control word and appended in suffix to the input data.

Hamming distance estimator is used to estimate transition activity within and between the buses. Logic full adders are used to implement the Hamming distance estimator, which estimates the transition activity. The circuit is designed using verilog HDL and the results are analyzed using Xilinx and Modelsim Tools and power is calculated using Xpower Tool.

The Logic full adder used in Hamming distance estimator occupies more number of logic gates to perform arithmetic operations while handling large number of data as input. This will increase the circuit complexity, area and power dissipation. So to reduce the area and power dissipation, Complementary pass transistor logic full adder (CPL) is implemented in the Hamming distance estimator to calculate the transition activity.

The design is implemented using Tanner EDA and the result is analyzed and compare with other existing CMOS logic full adder. The CPL full adder gives less area, delay and power dissipation than other methods. By using compression, multi coding and CPL logic the overall power dissipation and area has been reduced to the acceptable level.