CHAPTER 7

CONCLUSION

7.1 CONCLUSION

This research has analyzed a better method to transmit the data through the buses. To achieve this, the data was initially compressed using simple byte compression technique to reduce to the required bit level. To reduce the transition activity compressed data is coded into eight different way using multi coding technique. Then to estimate the transition activity the coded data is analyzed using Hamming distance estimator. Logic full adder and CPL full adders are implemented in the Hamming distance estimator to perform arithmetic operations. The results are analyzed for each logic design and the corresponding results are recorded.

To reduce the data rate and circuit complexity the information must be compressed. Text data compression is an important area because the reconstructed data should be identical to original input data. Even small differences will make very big issue in important applications. In this work lossless text compression technique namely a Simple byte compression (SBC) has been implemented. The results are analyzed and compared with existing lossless compression techniques. The average bits per character for SBC are 5.011which are less compared to other lossless compression techniques. The compression ratio is in the range of 1.57 to 1.68 and the compression factor is from 0.56 to 0.63. The saving percentage ranges from 36.38 to 43.91.

Considering above performance characteristics simple byte compression is the very best method among all. The output values of this algorithm are in an acceptable range and shows better results for text files.

During data transmission through buses the output nodes will charge and discharge through logic devices which causes data transition (switching activity) within and between the buses. To reduce the transition activity the data must be coded by proper coding method before transmitting data. Hence multi coding technique was implemented and the data are coded in 8 different ways. The transition effectiveness could be understood by the comparison of parameters like transition count and energy saving percentage. The coding methods are designed using verilog HDL, simulated and synthesized using modelsim and Xilinx. The results were analyzed and compared with the existing coding techniques. By using multi coding technique, 66.66% energy could be saved.

For effective data transmission and low power consumption it is necessary to know the number of transitions that occur in each coding method. Hamming distance estimator is used to estimate transition activity. Logic full adder used in the Hamming distance estimator to perform arithmetic functions occupies more area and power consumption. It produces a power dissipation of 33.25mW, delay of 23.755ns and area occupied 159 $\mu m^{2.}$

Complementary pass transistor logic (CPL) full adder was implemented in the Hamming distance estimator, the results were analyzed and compared with existing CMOS logic full adders, in terms of power dissipation, delay, area and transistor count. CPL logic full adder occupies less area 110 $\mu m^{2.}$, a delay of 13.04ns and power dissipation of 28.972mW.

7.2 FUTURE SCOPE

Future enhancements can be developed by partitioning of bus lines with larger bit width so that power could be saved efficiently and would be better than the coding techniques directly applied to the entire bus width. Crosstalk is another major problem that creates errors and delay on the buses. So implementing, partitioning with encoding technique in deep submicron designs will reduce crosstalk, delay and power dissipation.