CHAPTER 6

HAMMING DISTANCE ESTIMATOR USING PASS TRANSISTOR LOGIC

6.1 INTRODUCTION

Due to wide usage of portable electronic devices and the evaluation of microelectronic technology, power dissipation and area have become a critical parameter in Low power VLSI design in recent years. The reduction of the power consumption, area and increasing of the speed require optimizations at all levels of the design procedures. Complementary pass transistor logic circuits are used to design the Hamming distance estimator. Complementary pass transistor logic (CPL) is becoming increasingly important in the design of specific class of digital integrated circuits. Also CPL is much more power-efficient than conventional CMOS. In all type of digital circuits, designing of chips for low power technology is one of the most important challenges faced by the VLSI designers. Complementary pass transistor logic is intrinsically a lower power technology that has been established as the basic technology for the fabrication of integrated circuit mainly because it needs smallest area and fewer interconnections to design the circuits than other logic styles. The design styles which use CPL logic are the best in terms of low power dissipation and area because of its lower parasitic capacitance as well as node capacitance.

6.2 PASS TRANSISTOR LOGIC

A popular and widely used alternative to complementary CMOS is pass transistor logic. Pass transistor logic offers advantages of all the three metrics of VLSI like size, area, speed and power consumption .In electronics, pass transistor logic (PTL) describes several logic families used in the design of IC's. It reduces the transistor count used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of switches connected directly to supply voltages. This reduces the number of active devices.

If several devices are chained in series in a logical path, conventional gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic always switches transistors to the power supply rails, so that logic voltage levels do not decrease. As isolation is less between input and outputs signals, the output of one gate can only drive a finite number of inputs to other gates, a number called the 'fan out limit'. Also, there is always a delay called the 'propagation delay'. When gates are cascaded, the total propagation delay is approximately the sum of the individual delays, which can become a problem in high-speed circuits. Delay can be also caused when a large number of inputs are connected to an output, due to the distributed capacitance of all the inputs. The concept of pass transistor logic is used here is shown in Figure 6.1 to implement the full adders to achieve speed and low power consumption.

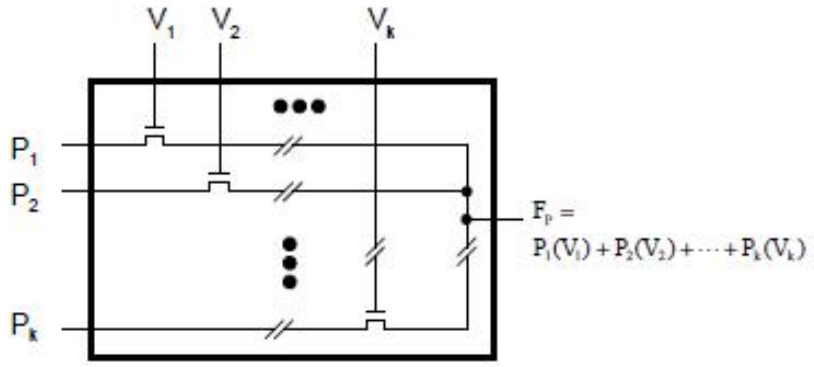

Figure 6.1 Pass transistor logic

6.2.1 NMOS Pass Transistor

Consider the single NMOS pass transistor shown in Figure 6.2. Assume that the voltage across the capacitor is initially 5V. When the gate of the NMOS transistor is taken to V_{DD}, the NMOS turns on. In this situation, assume that the drain of the NMOS is taken to V_{DD}, also connected to the load capacitance and that the source is connected to the ground , keeping in mind that the drain and source are interchangeable. The delay-time of the capacitor discharging is simply. Now consider Figure 6.3 where the capacitor is initially at 0V. In this case, the drain is connected to V_{DD} and the load is connected to the load capacitance. Since the substrate, assume at V_{SS} = ground, is not at the same potential as the source and have body effect present the threshold voltage to increase. When the gate of this NMOS is raised V_{DD}, the load capacitor changes into V_{DD}-V_{THN} where V_{THN}, is in the neighborhood of 1.5 V.

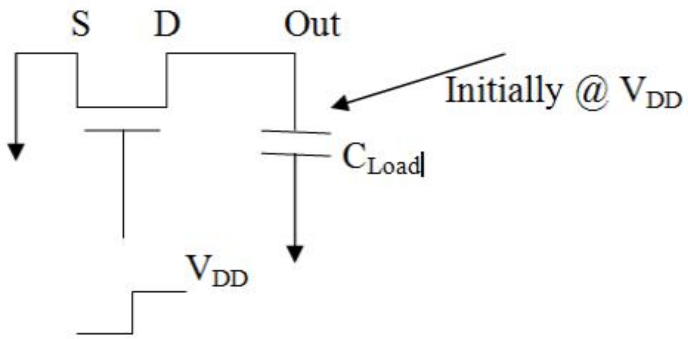

Figure 6.2 NMOS Pass transistor showing transmission of 0V

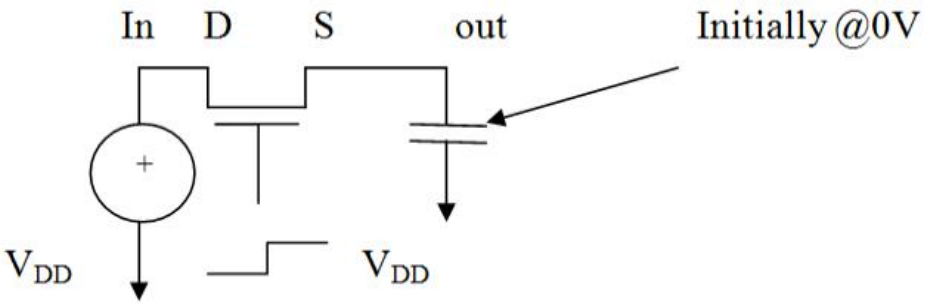

Figure 6.3 NMOS Pass transistor showing transmission of V_{DD}

6.2.2 PMOS Pass Transistor

Analyzing the operation of a PMOS pass transistor is shown in Figure 6.4. With S = 0, $V_{in} = V_{DD}$ and $V_{out} = V_{ss}$, the load capacitor C_{Load} remains unchanged. When S = 1, current begins to flow and charges the load capacitance toward $V_{DD.}$ However, When $V_{in} = V_{ss}$ and $V_{out} = V_{DD}$ the load capacitor discharges through P device until $V_{out} = V_{THP}$, at which point the transistor ceases conducting. Thus transmission of logic zero is somewhat degraded through the P device. Since the NMOS Pass transistor passes logic '0' well and the PMOS Pass transistor passes logic '1' well.

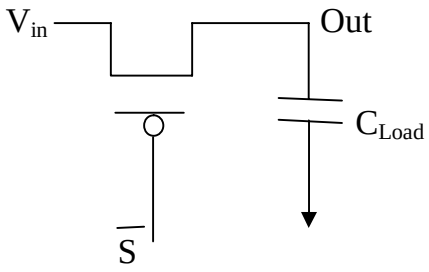

Figure 6.4 PMOS Pass transistor

6.3 ARITHMETIC ADDER

In order to achieve reduction of transition activity, it is used to estimate number of transition occurs between previous data and present data on the bus as well as transition in adjacent buses during data transmission using HD estimator. Here Figure 6.5 shows arithmetic adder implemented in HD estimator. Adders are key components in VLSI design for performing arithmetic operations. The reduction of transition improves the performance in terms of power dissipation, switching activity and delay in on chips. While handling large number of data these logic full adders implemented in arithmetic adder are not suitable for low power applications because it occupies more area and power consumption. So to improve the speed, reduce the power consumption and area different logic style full adders are implemented in the HD estimator to achieve best performance.

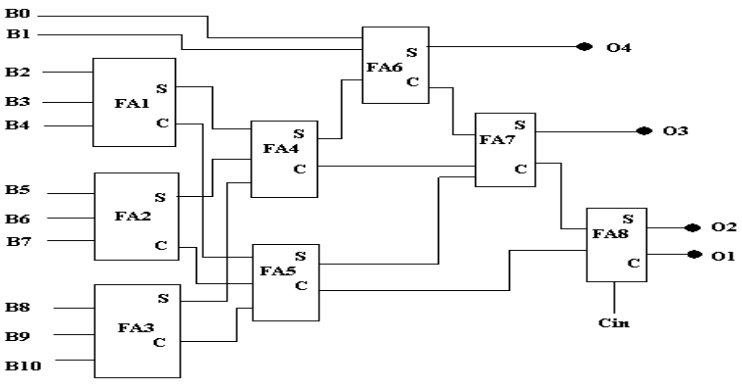

Figure 6.5 Arithmetic adder used in HD estimator

6.4 DIFFERENT LOGIC DESIGN ADDER

For compact arithmetic application various CMOS Logic full adder design styles are implemented here to achieve best performance like low power, small area and delay.

6.4.1 Conventional Static CMOS Logic Full adder

The recent VLSI arithmetic applications (Anu Gupta and Labros Bisdounis) use conventional static CMOS logic. The schematic diagram of a conventional static CMOS full adder cell is illustrated in Figure 6.6. The signals noted with '-' are the complementary signals. The P-MOS network of each stage is the dual network of the N- MOS. Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and arbitrary transistor sizes. In order to obtain a reasonable conducting current to drive capacitive loads the width of the transistors must be increased. This results in increased input capacitance and therefore high power dissipation and propagation delay.

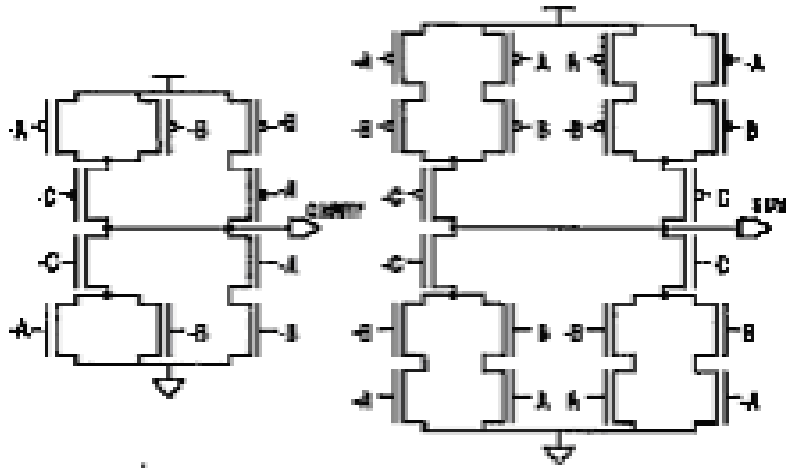

Figure 6.6 Conventional Static Full adder

6.4.2 Static Differential Cascode Voltage Switch Logic Full adder

Static DCVSL is a differential style of logic (Heller et al 1984) requiring both true and complementary signals to be routed to gates. Figure 6.7 shows the circuit diagram of static DCVSL full adder. Two complementary NMOS switching trees are constructed to a pair of cross coupled PMOS Transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding NMOS network. The differential output is then latched by the cross coupled PMOS transistors. The input drives only the NMOS transistors of switching trees and so input capacitance is typically two or three times smaller than that of conventional static CMOS logic.

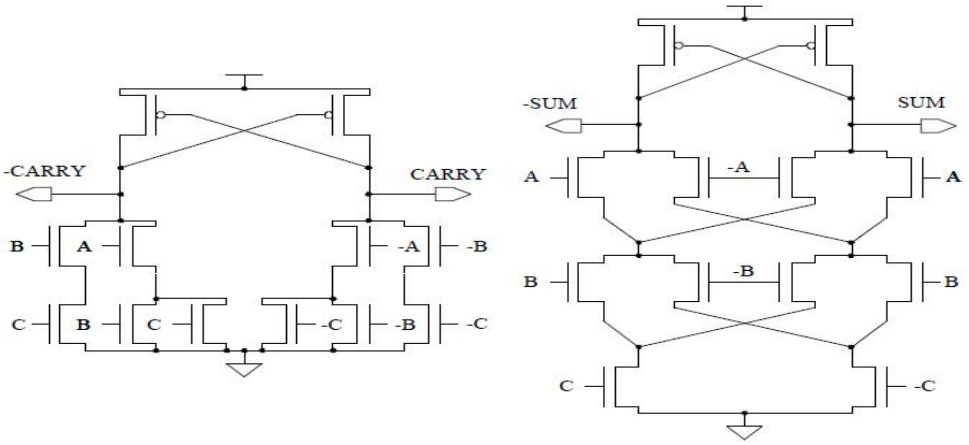

Figure 6.7 Static Differential Cascode Voltage Switch Full adder

6.4.3 Dual Rail Domino Logic Full Adder

It is a precharged circuit technique which is used to improve the speed of CMOS circuits (Krambeck et al 1982) and (Oklobdzija & Montoye 1986). Figure 6.8 shows a dual rail domino full adder circuit. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer. The dynamic circuit consists of a PMOS precharge transistor and NMOS evaluation transistor with the clock signals applied to their nodes and

NMOS also implements the required logic function. During the precharge phase clk = 0 the output node of a dynamic circuit charged through the precharged PMOS transistor to the supply voltage level. The static buffer output is discharged to ground. During the evaluation phase clk = 1 the evaluation NMOS transistor is ON, the output of the dynamic circuit is either discharged or it will stay precharged. One major advantage of the dynamic precharged design style over the static style is that they eliminate the spurious transitions and the corresponding power dissipation. Dynamic logic does not suffer from short circuit currents which flow in static circuits. But in dynamic circuits additional power is dissipated by the distribution network and the drivers of the clock signal.

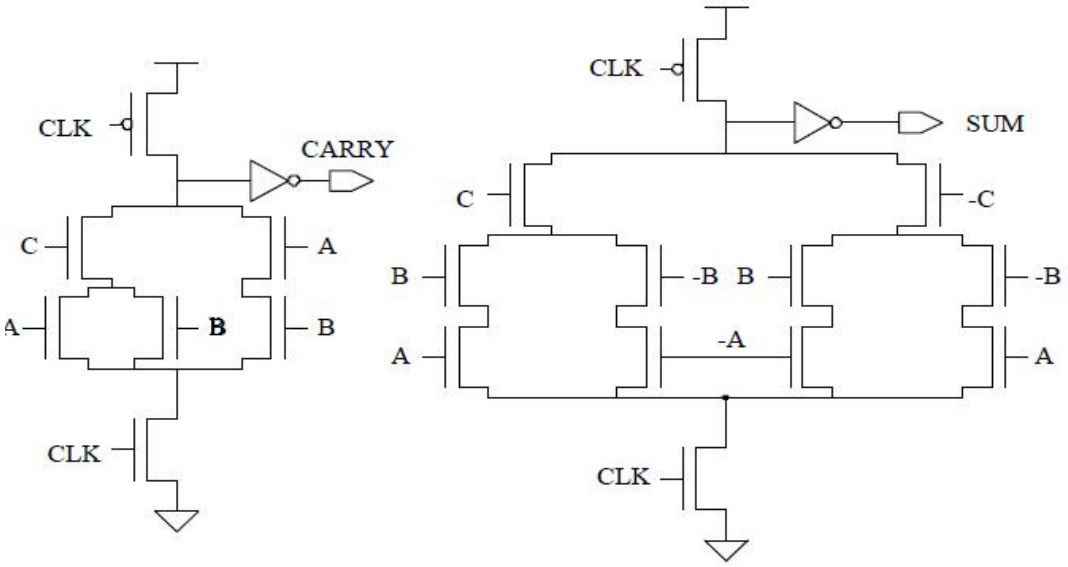

Figure 6.8 Dual Rail Domino Logic Full adder

6.4.4 Double Pass Transistor Logic Full adder

DPL is a modified logic of CPL. The DPL full adder is given in Figure 6.9 (Lu 1988) and (Bisdounis et al 1996). In DPL circuit full-swing operation is achieved by simply adding PMOS transistors in parallel with the NMOS transistors. Here the problems of noise margin and speed degradation

at reduced supply voltages, created in CPL circuits due to the reduced high voltage level, are avoided in Double pass transistor (DPL) logic Full adder The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines (Oklobdzija & Montoye 1986). The advantage is that one pass-transistor network is sufficient to perform the logic operation, which results in a smaller number of transistors and input loads, when NMOS networks are used. But, the threshold voltage drop through the NMOS transistors while passing logic "1" makes swing (or level) restoration at the gate outputs necessary in order to avoid static currents at the subsequent output inverters or logic gates. However, the addition of PMOS results in increased input capacitances which causes power dissipation.

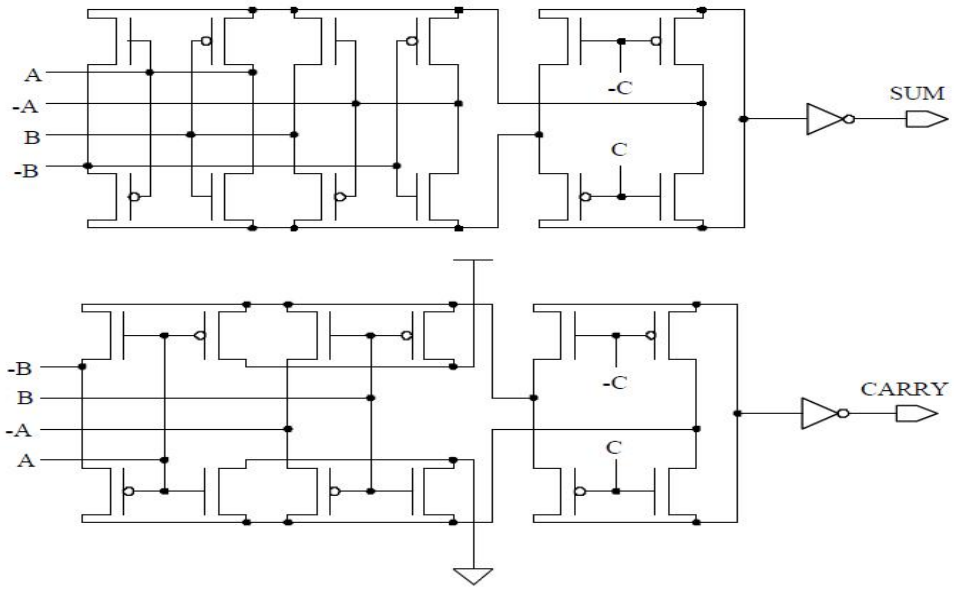

Figure 6.9 Double Pass Transistor Logic Full adder

6.4.5 Static Differential Split Level Logic (SDSL) Full adder

The variation of the differential logic style is described in the static DSL is shown in Figure 6.10 (Fennings et al 1985). Two NMOS transistors with their gates connected to a reference voltage are added to reduce the logic

swing at the nodes. The output nodes are clamped at the half of the supply voltage level. Thus, the circuit operation becomes faster than standard DCVL circuits. However, due to the incomplete turn off of the cross coupled PMOS transistors; SDSL circuits dissipate high static power dissipation. Also, the addition of two extra NMOS transistors per gate results in area overhead.

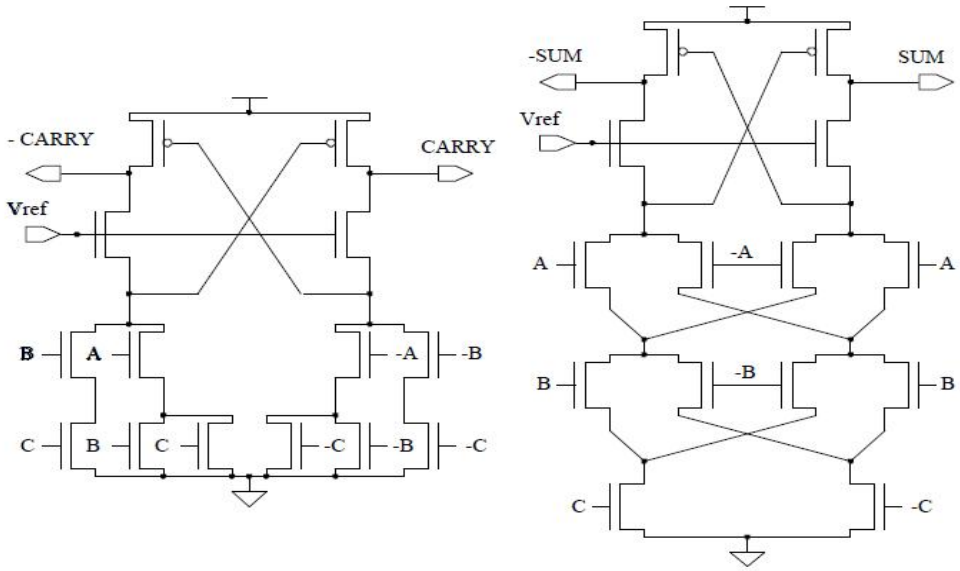

Figure 6.10 Static Differential Split Level Logic Full adder

6.4.6 Dynamic Differential Cascode Voltage Switch Logic (DDCVSL) Full adder

Dynamic DCVSL is a combination between the domino logic and the static DCVSL and a full adder circuit diagram is shown in Figure 6.11 (Chu & Pulfrey 1986). The advantage of this style logic can only generate noninverted forms of logic. For example, in the design of ripple carry adder, two cells must be designed for the carry propagation, one of the true carry signal and another for the complementary one. Using DCVSL to design dynamic circuits will eliminate PMOS logic gates because of the inherent availability of complementary signals. The P logic gates usually cause long delay times and consume large areas.

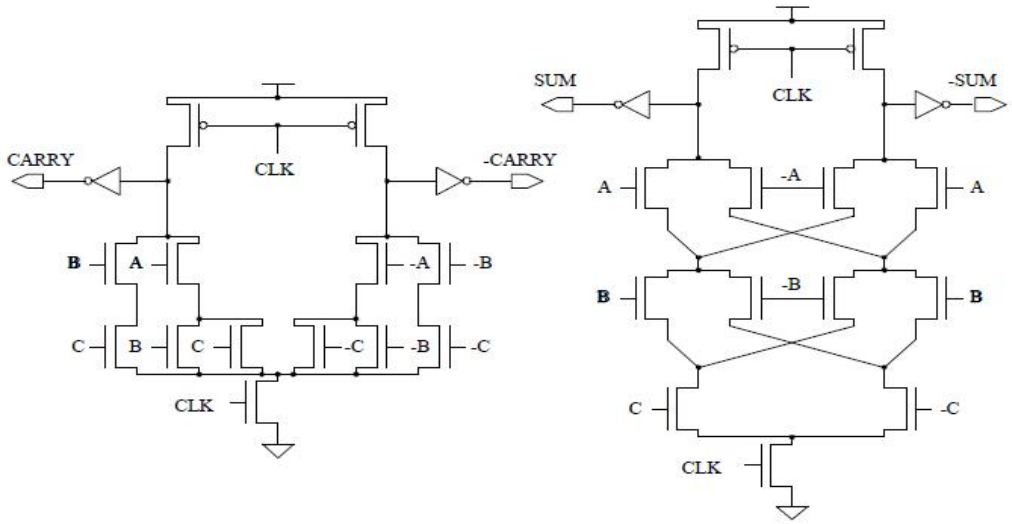

Figure 6.11 Dynamic Differential Cascode Voltage Switch Logic Full adder

6.4.7 Complementary Pass Transistor Logic Full adder (CPL)

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power rails. One pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in smaller number of transistors and input loads, especially when NMOS are used (Zimmermann & Fichtner 1997). The concept of pass transistor logic is used here to implement the full adders to achieve speed and low power consumption is retrieved. Thus the reduction of self and coupling transitions will reduce the power dissipation during the transmission of data through the bus. The main concept behind CPL is the use of only an NMOS network for the implementation of logic functions which results in low input capacitance & high speed operation.

The schematic diagram of the CPL full adder is as shown in the Figure 6.12 (Yano et al 1990). Because the high voltage level of the pass transistor outputs is lower than the supply voltage and is depended on the threshold voltage of the pass transistors and so the signals have to be

amplified by using CMOS inverters at the outputs. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistors outputs is smaller than the supply voltage level. In the case of conventional static CMOS circuits the voltage swing at the output nodes is equal to the supply voltage, resulting in power dissipation. To minimize the static current due to in-complete turn off of the PMOS device in the output inverters, a weak PMOS feedback device can be added in the CPL circuits in order to pull the pass-transistors output to full supply voltage level.

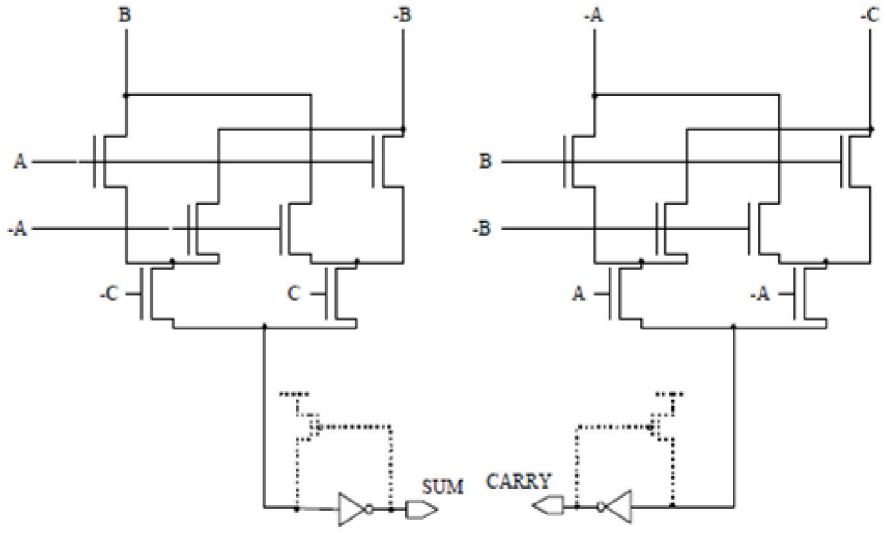

Figure 6.12 Complementary Pass Transistor Logic Full adder

6.5 RESULTS AND DISCUSSIONS

Complementary pass transistor logic (CPL) is implemented in full adder circuit which is used in the transition estimator of low power encoder to achieve a reduced power dissipation, delay and area. Several existing CMOS Logic design techniques are analyzed and their characteristics are evaluated in terms of power dissipation, delay, area and transistor count with CPL design. Among them CPL gives better power, delay and area efficiency were listed from Table 6.1 and Figure 6.13 to 6.18.

6.5.1 Comparison of Different CMOS Logic Design

To evaluate the effectiveness of full adder used in transition estimator different CMOS logic design styles like Conventional static CMOS (CSL), Double pass transistor (DPL), Static differential cascode voltage switch logic (SDCVSL), Dual rail domino logic (DRDL), Static differential split level logic (SDSL), Dynamic differential cascode voltage switch logic (DDCVSL), Complementary pass transistor logic (CPL) characteristics are compared and their results were shown from Table 6.1 and Figure 6.13 to 6.17. From this analysis Propagation delay and power dissipation for CPL is the best logic compare with other logic designs.

Table 6.1 Parameters comparison for different CMOS logic design

Sl.No	Design Method	Number of Transistors Used	Power Dissipation (mw)	Propagation delay (ns)	Area (μm^2)
1	CSL	288	32. 261	23.058	180
2	DPL	272	31.028	14.186	170
3	SDCVSL	232	30.872	15.501	145
4	DRDL	296	43.481	18.734	185
5	SDSL	256	35.283	14.092	160
6	DDCVSL	312	52.074	23.926	195
7	CPL	176	28.972	13. 04	110

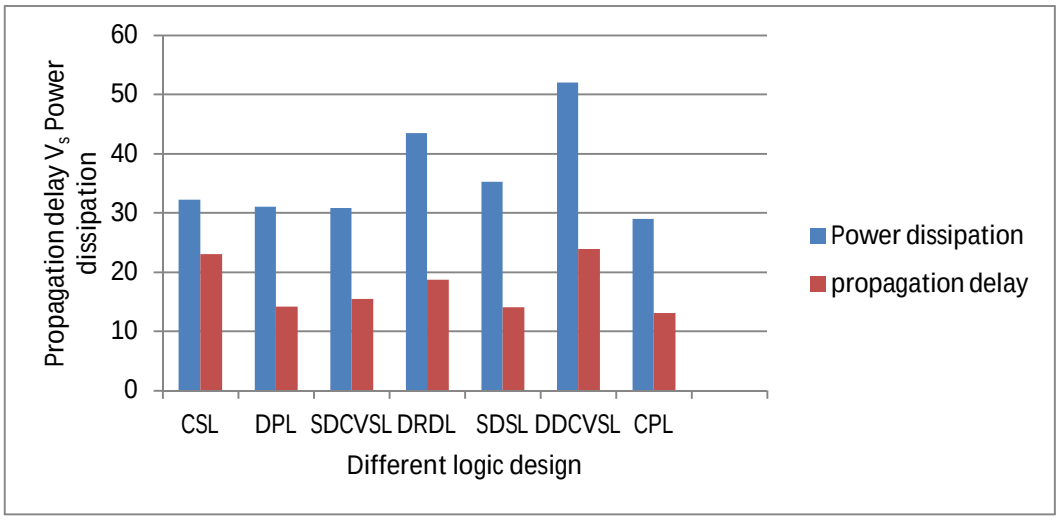

Figure 6.13 Propagation delay V_s power dissipation of different CMOS logic design

6.5.2 Transistor Count

In CMOS logic design Power dissipation mainly depends on the number transistors used per unit area. Table 6.2 and Figure 6.13 shows comparison of different CMOS full adder logic based on number transistors used for the design. From this analysis CPL design gives least transistor count than other CMOS logic styles.

Table 6.2 Transistor count in different CMOS logic design

Sl. No	Design Method	Number of Transistors Used
1	CSL	288
2	DPL	272
3	SDCVSL	232
4	DRDL	296
5	SDSL	256
6	DDCVSL	312
7	CPL	176

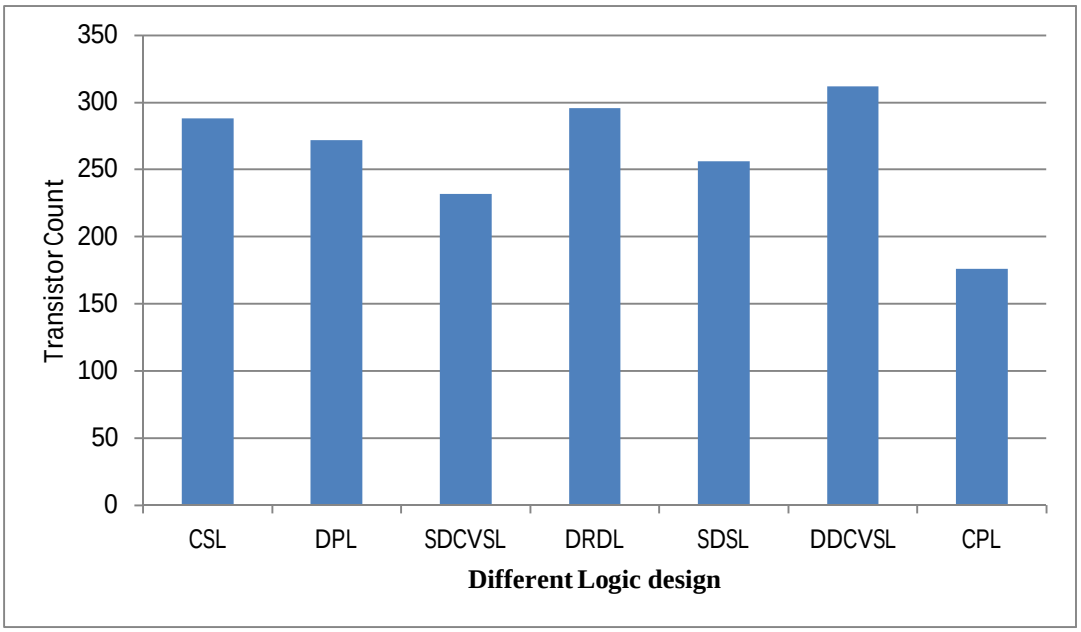

Figure 6.14 Transistor count for different CMOS logic design

6.5.3 Power Dissipation

Reduction in power dissipation is an essential design issue in VLSI circuit. The design parameters have conflicting to affect on overall performance of the system. Depending upon the component and function different optimization approaches can be adapted. The reduction of power dissipation requires optimizations at all levels of the circuit design. The best way of achieving low power dissipation by seven different CMOS logic full adders are designed and analyzed and the results are presented in the Table 6.3 and Figure 6.15. Among all CPL design gives lowest power consumption than other logic styles.

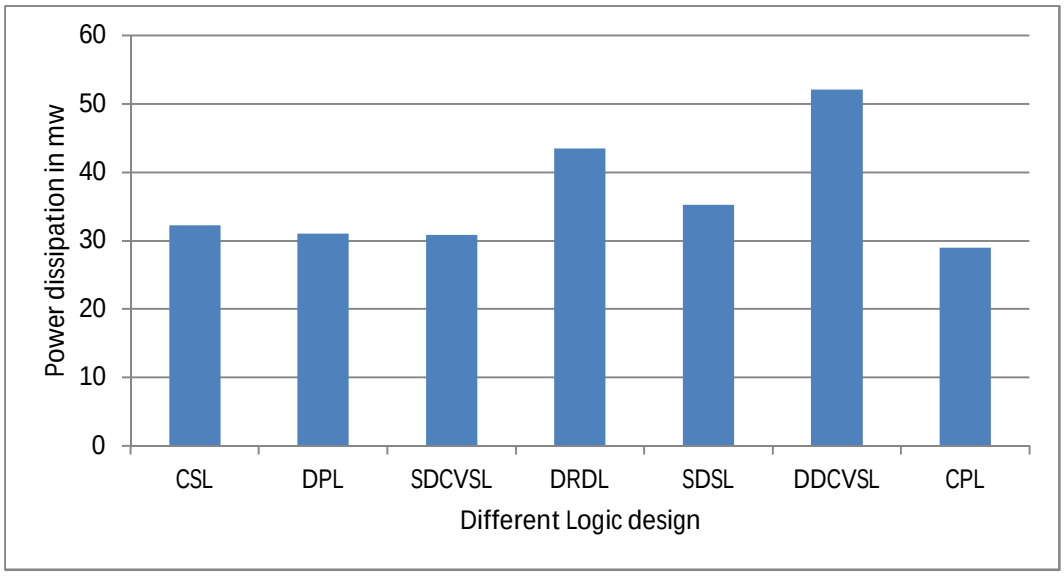

Figure 6.15 Power dissipation for different CMOS logic design

Table 6.3 Power dissipation for different CMOS logic design

Sl.No	Design Method	Power Dissipation (mw)
1	CSL	32. 261
2	DPL	31.028
3	SDCVSL	30.872
4	DRDL	43.481
5	SDSL	35.283
6	DDCVSL	52.074
7	CPL	28.972

6.5.4 Propagation Delay

In electronic digital circuits the propagation delay is the length of time which starts when the input to a logic design becomes stable and valid to change, to the time that the output of the logic design is stable and valid to change. Reducing delays in digital circuits to process data at faster rate and

improve performance. Propagation delay of the different logic designs are compared and shown in Table 6.4 and Figure 6.16, from this analysis CPL is the lowest propagation delay than other logic styles.

Table 6.4 Propagation delay for different CMOS logic design

Sl.No	Design Method	Propagation delay (ns)
1	CSL	23.058
2	DPL	14.186
3	SDCVSL	15.501
4	DRDL	18.734
5	SDSL	14.092
6	DDCVSL	23.926
7	CPL	13. 04

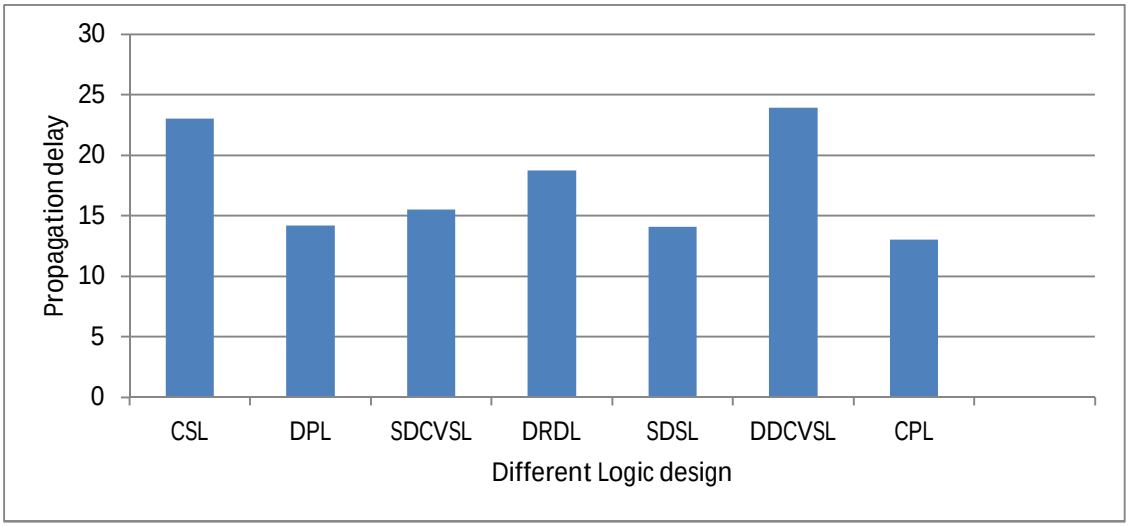

Figure 6.16 Propagation delay for different CMOS logic design

6.5.5 Area

Integrated circuits are much smaller both transistors and wires are shrunk to micrometer and centimeter scales of discrete components. The size of the circuit can be determined by using total number of required IO devices. Small size leads to high speed and low power consumption. The product of channel width and length of the transistor also determines area of design. From the Table 6.5 and Figure 6.17 CPL circuit occupied smallest area than other logic design.

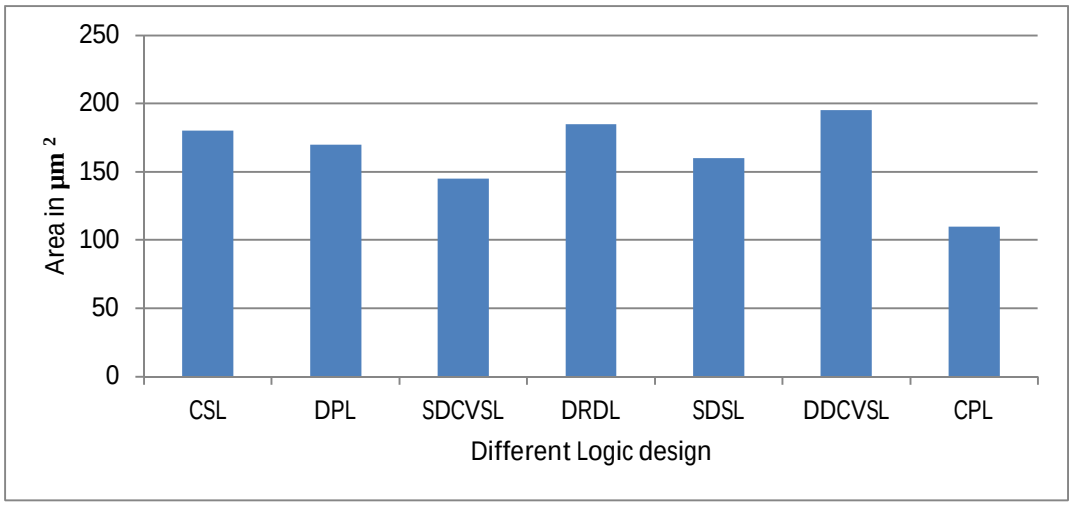

Figure 6.17 Area of different CMOS logic design

Table 6.5 Area of different CMOS logic design

Sl.No	Design Method	Area (μm^2)
1	CSL	180
2	DPL	170
3	SDCVSL	145
4	DRDL	185
5	SDSL	160
6	DDCVSL	195
7	CPL	110

6.6 SIMULATION RESULT

The proposed CPL full adder logic is designed and simulated using Tanner EDA Tool. The result is analyzed and listed in Figure 6.18.

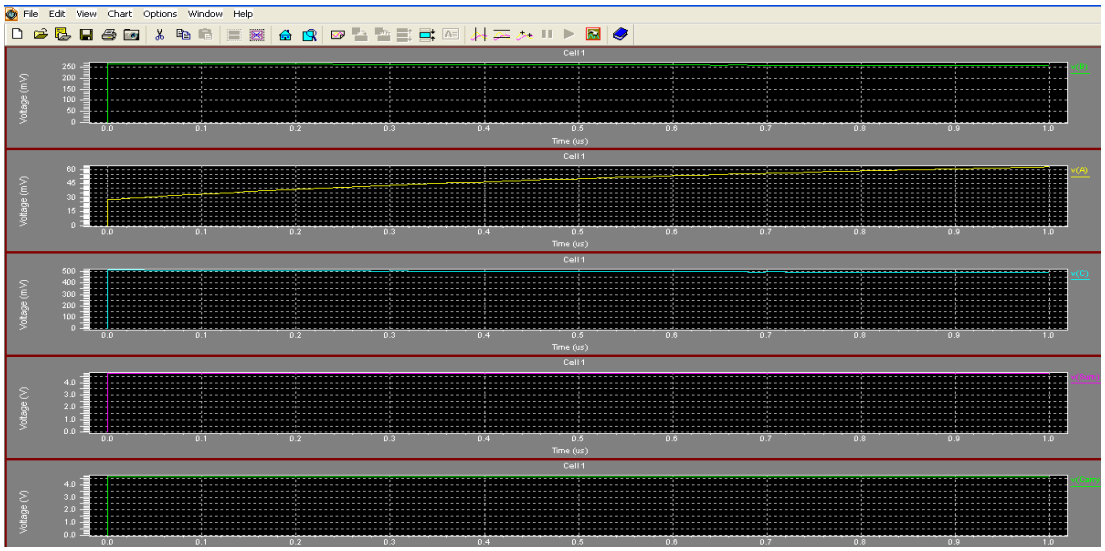

Figure 6.18 Simulation result of CPL adder

The three inputs signals V(A), V(B), V(C) are high the output signals sum and carry is also in the high state and thus the full adder logic is verified from this simulation result. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high power consumption, propagation delay and increases the speed.

6.7 CONCLUSION

The proposed CPL full adder logic has been designed and implemented in low power encoder circuit simulated using tanner EDA tool and the results are compared with existing CMOS logic full adders like CSL, SDCVSl, DRDL, DDCVSL, SDSL with respect to power, delay and area as shown in Table 6.1 to 6.6 and Figure 6.13 to 6.18.

Table 6.2 and 6.6 shows that the transistor counts, area of CPL & SDCVSL are less than other CMOS logic. The Table 6.3 and 6.4 shows propagation delay and power dissipation of CPL and DPL are less than other logic styles. Among all, CPL has less area which has fewer transistors and less interconnection. Less interconnection gives reduced delay and power dissipation. From all aspects it is concluded that CPL adder logic gives better power, delay and area efficiency than other CMOS logic designs.