CHAPTER 5

POWER MODELING AND ESTIMATION TECHNIQUES

5.1 INTRODUCTION

In emerging VLSI technology, the circuit complexity and high speed implies significant increase in the power consumption In VLSI design small area and high performance are two conflicting constraints. The integrated circuit (IC) designer's activities have been involved in trading of these constraints. There are many possible design considerations, due to which the power efficiency has become important. The most portable systems used in recent era, which are powered by batteries, are performing tasks requiring lots of computations. At the same time these systems are becoming physically smaller in size and battery weight is becoming more important factor.

5.2 NEED FOR LOW POWER DESIGN

In the early 1970's designing digital circuits for high speed and minimum area were the main design constraints. EDA tools were designed specifically to meet these criteria. Design process also included power consumption, but not very visible. In digital circuits area reduction is not as big issue today because of new IC production techniques, as millions of transistors could be fit in a single IC. In submicron technologies, there is a limitation on the proper functioning of circuits due to heat generated by power dissipation. Markets demand low power for not only better life but also

reliability, portability, performance, cost and time to market. This is very true in the field of personal devices, wireless systems and entertainment systems which are more popular now-a-days. Devices used for high-performance computing particularly needs to dissipate less power to function correctly and for a long period of time. Keeping all these in mind, low power design has become one of the most important design parameters for VLSI (Very Large Scale Integration) systems. (Goh et al 2002).

5.3 LOW POWER DESIGN METHODOLOGY

Historically, VLSI designers have used circuit speed as the performance metric. In fact, power considerations have been the ultimate design criteria in special portable applications. The objective in these applications was minimum power for maximum battery life time. Low power design not only needed for portable applications but also to reduce the power of high performance systems with large integration density and improved speed of operation.

In order to optimize the power dissipation of digital systems low power methodology should be applied through the design process from system level to process level. During optimization it is very important to know the power distribution within a process. Thus the parts or blocks consuming an important fraction of the power are properly optimized for power saving. Figure 5.1 shows the different design levels of power reduction aspects.

5.3.1 Power Reduction Through Process Technology

One way to reduce the power dissipation is to reduce the power supply voltage. However the delay increases significantly, when V_{DD}

approaches the threshold voltage. Devices should be scaled correctly to overcome this problem. The advantages of scaling are,

- Improved device characteristics for low voltage operation.
- Capacitance reduction through small geometries and junction capacitances.
- Improved interconnect technology
- Multiple and variable threshold devices available
- High density of integration, It was shown that the integration of a whole system in to a single chip.

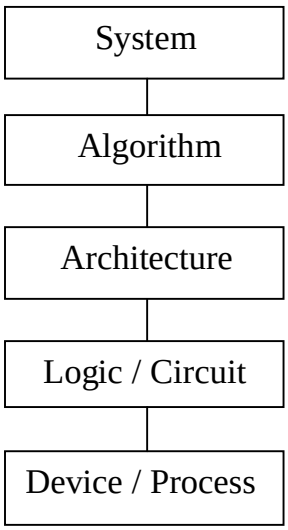

Figure 5.1 Power reduction design aspects

5.3.2 Power Reduction Through Circuit / Logic Design

To minimize the power at circuit / Logic level many techniques can be used such as

- Use of more static over dynamic
- Reduce the switching activity by logic optimization

- Optimize clock and bus loading
- Clever circuit techniques which minimizes device count and internal swing
- Custom design may improve the power
- Reduces V_{DD} in non-critical paths and proper transistor sizing
- Use of multi V_T circuits
- Re encoding of sequential circuits

5.3.3 Power Reduction Through Architectural Design

At the architectural level, several approaches can be applied to the design.

- Power management techniques where unused blocks are shut down.
- Low power architectures based on parallelism, pipelining etc,
- Memory partitioning with selectively enabled blocks
- Reduction of the numbers of global buses
- Minimization of instruction set for simple decoding and execution.

5.3.4 Power Reduction Through Algorithm

Among the techniques to minimize the power at the algorithmic level,

- Minimizing the number of operation and hence reduce the number of hardware resources.
- Data coding for minimum switching activity**.**

5.3.5 Power Reduction Through System Integration

The level of the system is also important for power optimization. Some techniques are,

- Utilize low system clocks, higher frequencies are generated with on chip phase locked loop.
- High level of integration , integrate off-chip memories

5.4 POWER MODELING

To minimize the power consumption of a circuit, various power components and their effect must be identified. There are two types of power dissipation, one is the maximum power dissipation, which is related to the peak of the instantaneous current and the other is the average power dissipation. The peak current has an effect on the supply voltage noise due to the power line resistance. It can cause heating of the device, thus resulting in performance degradation. From the battery life time point of view, the average power dissipation is more important.(Abdellatif Bellaonat & Mohamed 1996).There are three power dissipation components:

- Static power due to leakage current ILeak and other static component I_{St} due to the value of the input voltage.
- Dynamic power caused by the total output capacitance CL
- Short circuit current ISC, during the switching transient.

5.4.1 Static Power Dissipation

It is the power consumed during the standby mode of a design .CMOS gates typically have some amount of sub threshold leakage current even when gate are not turned on. The drain to source leakage current is the main component of static power consumption .The leakage power was a very small part of the overall power consumption. In a typical chip 10% of the power consumed is leakage and 90% is dynamic power. So, clearly the major concern is dynamic power dissipation. Figure 5.2 shows static power calculation model.

Instantaneous power $P(t) = i_{DD}(t)V_{DD}$ (5.1)

Energy $E = \int_0^T p(t)dt$ (5.2)

$E = \int_0^T iDD(t)VDD\ dt$ (5.3)

Static power $P_S = E/T$ (5.4)

$P_S = 1/T\int_0^T iDD(t)VDD\ dt$ (5.5)

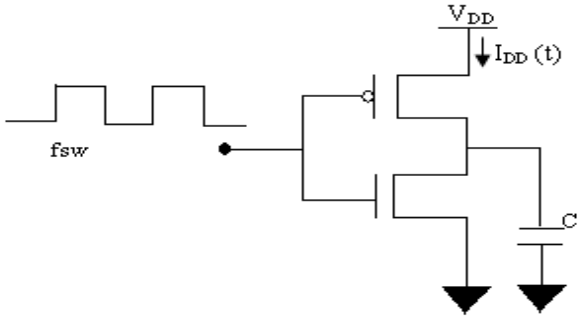

Figure 5.2 Static power calculation model

5.4.2 Dynamic Power Dissipation

A dynamic power vector describes an event in which power is dissipated due to a signal switching at the cell inputs during charging and discharging of load capacitance. Dynamic power is further divided into switching power and internal power.

5.4.2.1 Switching power

Switching power is dissipated when charging and discharging the load capacitance at the cell output. The load capacitance is composed of interconnect (net) capacitance and gate capacitances the net is connected to. The amount of switching power depends on the switching activity (is related to the operating frequency) of the cell. If there are more logic transitions on the cell output, switching power increases.

5.4.2.2 Internal power

Internal power is consumed within a cell for charging and discharging internal cell capacitances which also includes short-circuit power. During logic transitions both P and N type transistors are both on simultaneously for a short time causing direct connection from V_{dd} rail to ground rail.

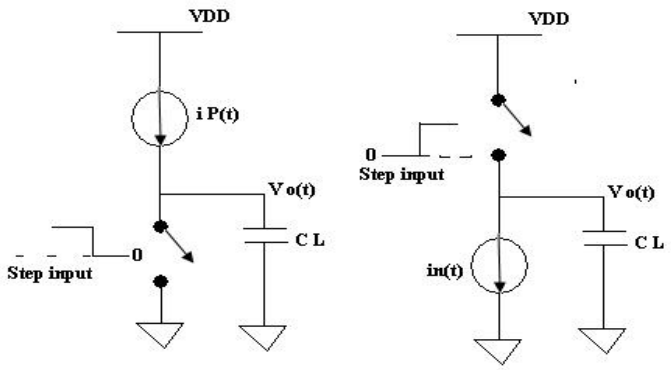

Figure 5.3 Equivalent circuit for dynamic power calculation

The power dissipation can be estimated by the load capacitance C_L. This power loss is due to the charging and discharging of Load Capacitance C_L. The average dynamic power P_D is required to charge and discharge a capacitance C_L at a switching frequency f_{sw} and equivalent dynamic power calculation model is shown in Figure 5.3.

$$P_D = f_{sw} \int_0^T io(t)Vo(t)dt \tag{5.6}$$

During charging cycle

$$i_p = C_L \cdot \frac{dVo}{dt} \tag{5.7}$$

During the discharge cycle

$$i_n = - C_L \cdot \frac{dVo(t)}{dt} \tag{5.8}$$

$$P_D = f_{sw} \left[\int_o^{VDD} C_L V_o \, dVo - \int_{VDD}^{o} C_L V_o \, dVo\right] \tag{5.9}$$

$$P_D = f_{sw} \left[C_L \left[\left[\frac{Vo^2}{2}\right]_0^{VDD} - \left[\frac{Vo^2}{2}\right]_{VDD}^{0}\right] \right] \tag{5.10}$$

$$P_D = f_{sw} \left[C_L \left[\frac{V_{DD}^2}{2} + \frac{V_{DD}^2}{2}\right] \right] \tag{5.11}$$

$$P_D = f_{sw} C_L V_{DD}^2 \tag{5.12}$$

Assuming a logic gate goes through one complete charge/discharge cycle for every clock cycle, suppose the system clock frequency is f.

Let $f_{sw} = Ef$; Where E is the energy transition activity factor

Most gates do not switch every clock cycle,

$$P_D = E\, C_L . V_{DD}^2 . f \tag{5.13}$$

A clock has E=1 because it rises and fall every cycle, but most data have a maximum Energy Transition activity factor E=0.5 because they transit only once every cycle

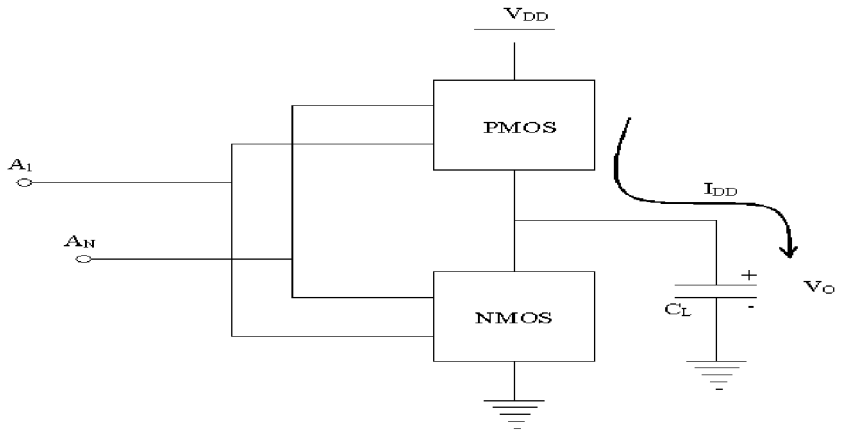

Figure 5.4 Energy per transition

The dynamic component of power consumption arises when the capacitive load C_{load} of a CMOS circuit is charged through PMOS transitions to make a voltage transition from 0 to 1, half of which is stored in the output capacitor and half is dissipated in the PMOS device. No charge is drawn from the V_{DD} during the 1 to 0 transition at the output. But the energy stored in the capacitor is dissipated in the pull down NMOS device is shown in Figure 5.4. The main cause of energy dissipation in CMOS circuits is due to charging and discharging of the node capacitances. Power analysis chart is also shown in Figure 5.5.

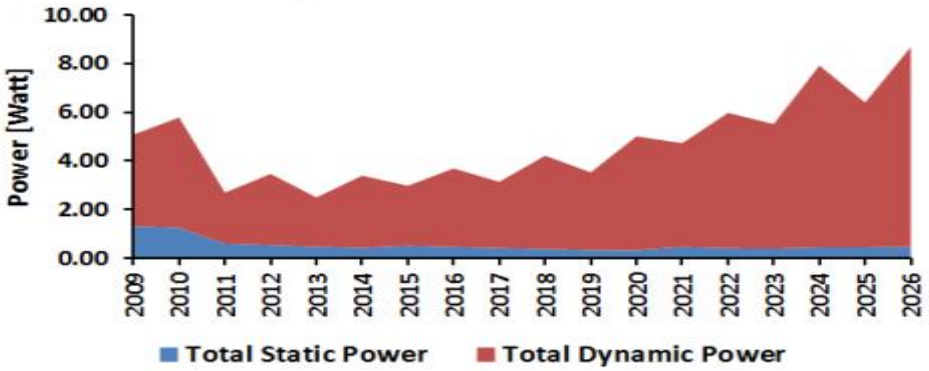

Figure 5.5 Power analysis chart, IRTS-2011

5.5 DESIGN PARAMETER

The research work focus on estimating the dynamic power dissipation. In the past, the major concern of the designer was in area, speed and cost. But secondary importance was provided for power considerations. In recent years, power has become as the primary design consideration. Several factors contribute to this trend like the growth of personal computing devices such as portable desktops, audio and video based multimedia products and wireless communication systems which demand high speed computation and complex functionality with low power consumption. So there is a strong requirement for power consumption reduction so as to reduce packaging and cooling cost and improve product reliability (Massoud pedram 2000). When the target is a low power application a power analyzer / Estimator ranks the various design aspects, thus helps in selecting the one that is potentially more effective from the power stand point

5.5.1 Two Dimension Design Flow

A top-down two dimension ordinary VLSI design approach is illustrated in Figure 5.6. The figure summarizes the flow of steps that are required to follow from a system level specification to the physical design. The approach is aimed to estimate the design parameters performance optimization and area minimization is shown in Figure 5.7.

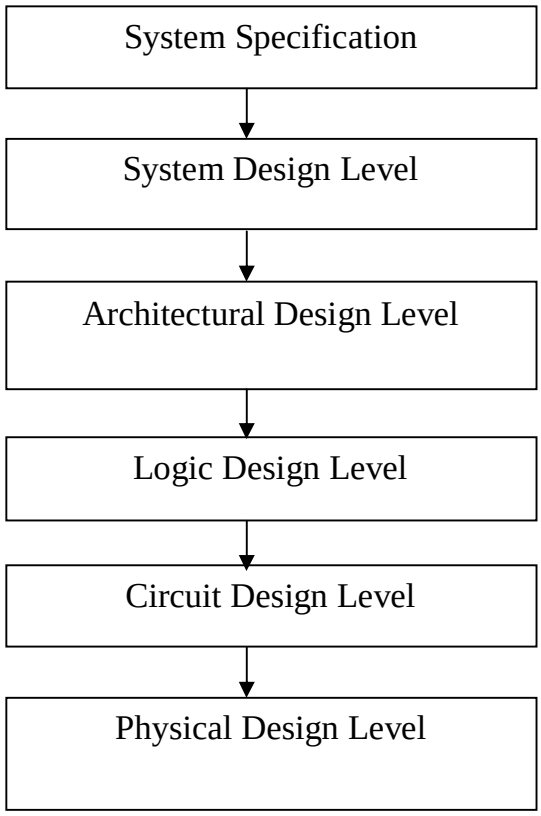

Figure 5.6 Two dimension (2D) VLSI Design Flow

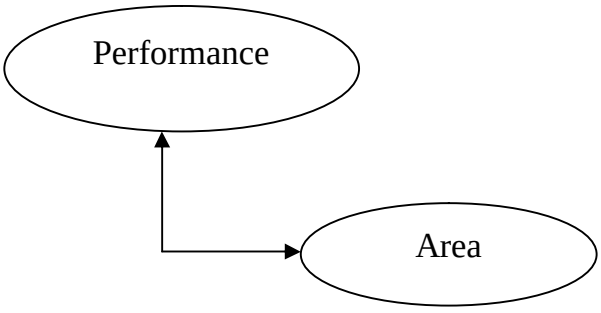

Figure 5.7 Two dimension (2D) design parameter

5.5.2 Three Dimension Design Flow

A Three dimension top-down VLSI design approach is illustrated in Figure 5.8. The figure summarizes the flow of steps that are required to follow from a system level specification to the physical design. The approach is aimed to estimate the design parameters at performance optimization, area minimization and power optimization is shown in Figure 5.9. In each of the design levels there are two important power factors, namely power optimization and power estimation. Power optimization is the process of obtaining the best design knowing the design constraints and without violating design specifications. Power estimation is defined as the process of calculating power and energy dissipated with a certain percentage of accuracy and at different phases of the design process.

Power estimation techniques evaluate the effect of various optimizations and design modifications on power at different abstraction levels are shown in Figure 5.10. Design performs power optimization step first and then power estimation step. But within a certain design level there is no specific design procedure. Each design may include a large collection of low power techniques which may result in significant reduction of power dissipation. But certain combinations of low power designs may lead to better results than another series of techniques. Generally, power is consumed when capacitors in the circuits are either charged or discharged due to Transition activities. So at higher levels of a system this power dissipation is conserved by reducing the Transition activities which is done by shutting down portions of the system when they are not needed.

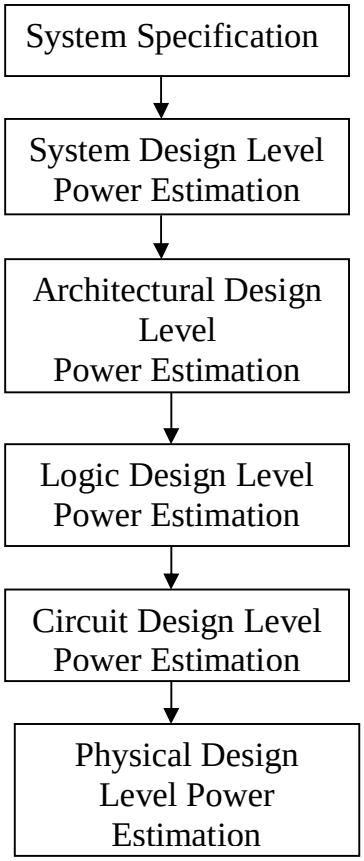

Figure 5.8 Three dimension (3D) VLSI design flow

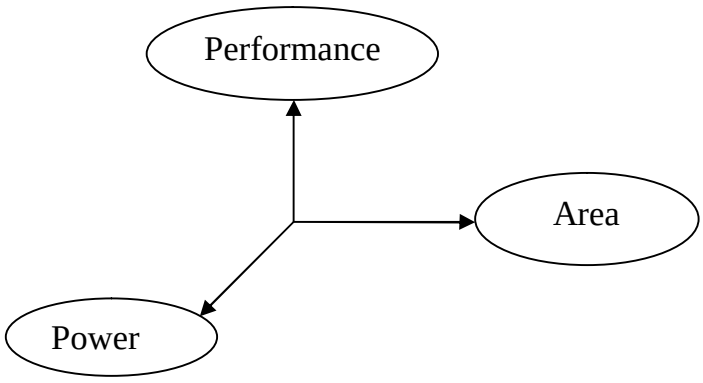

Figure 5.9 Three dimension (3D) design parameter

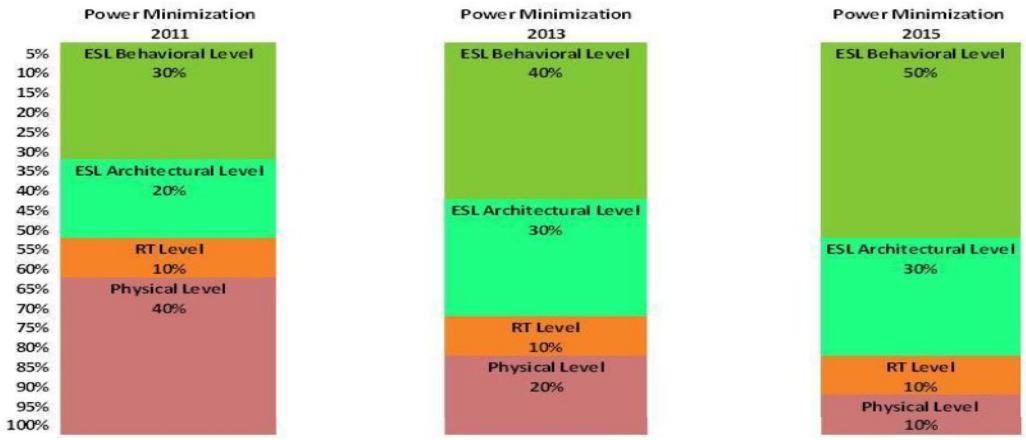

Figure 5.10 Relationship between different abstraction level & power estimation techniques

5.6 POWER ESTIMATION TOOL

In recent years, programmable design and device sizes have grown to astonishing levels of complexity. Average design sizes were approximately twelve thousand gates a few years ago. Now, they have bloomed into hundreds of thousands and even multimillion gate arrays. And, as design sizes increase, so does power consumption. Meanwhile, the demand has risen for battery- powered handheld devices that are increasingly smaller and sensitive to power usage. It’s clear that power consumption can no longer be ignored in Programmable logic design.

There has been a variety of tools available to calculate the power of a logic design. Even though, this thesis is all about power calculations of macros which are done using Power tools, there are other tools that have been used prior to the usage of power tools to give the required input to the power tools. More emphasis is provided to the tools that are mainly involved in low power estimation which has been classified as Power tools and Non-Power tools.

5.6.1 Non-Power Tool

Non-power tools include Simulation tools, Synthesis tools, Layout tools, Extraction tools and Waveform viewers.

5.6.1.1 Simulation tool

Initially, Verilog or VHDL code for a particular design is written and tested. Simulation is completed using Mentor's Modelsim for both VHDL and other Verilog simulators. ModelSim is a simulation and a debugging tool for VHDL, Verilog, and other mixed-language designs from Mentor Graphics.

5.6.1.2 Synthesis tool

Xilinx is used as core synthesis software. It synthesizes HDL designs into optimized technology-dependent, gate-level designs. It also supports a wide range of hierarchical design styles and can optimize both combinational and sequential designs for speed, area, and power. Figure 5.11 and 5.12 are synthesis output of RTL schematic encoder design.

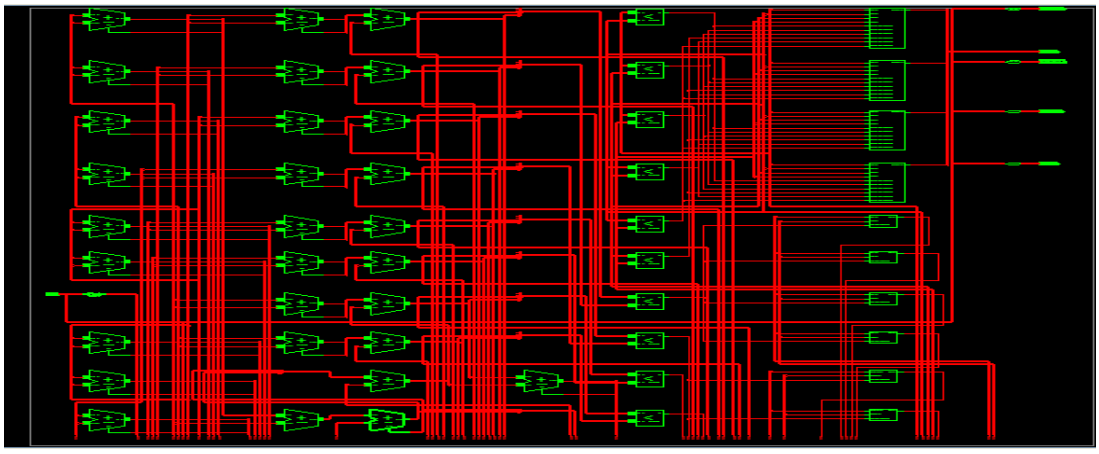

Figure 5.11 RTL Schematic overview of encoder

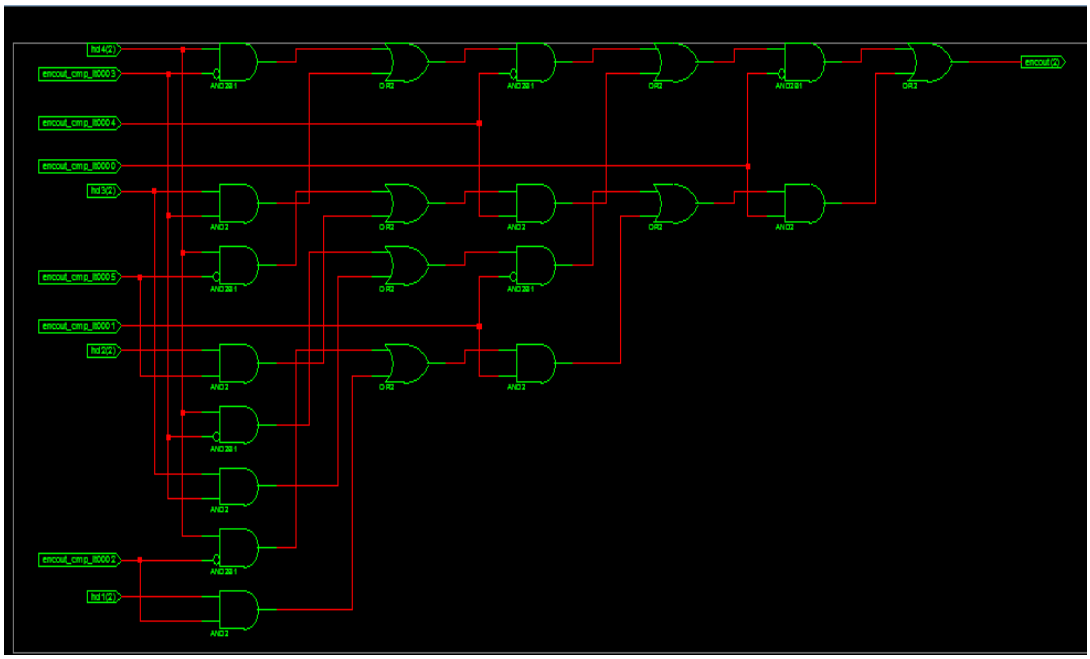

Figure 5.12 RTL Schematic of encoder output

5.6.1.3 Area output

The area of the circuit can be determined by using total number I/O devices used to design a circuit. Small size leads to high speed and low power consumption. Figure 5.13 shows the synthesis report of area requirement for encoder design.

```
Device utilization summary:
---------------------------

Selected Device : 3s500eft256-4

 Number of Slices:                      108  out of   4656     2%
 Number of 4 input LUTs:                202  out of   9312     2%
 Number of IOs:                         159
 Number of bonded IOBs:                 159  out of    190    83%
```

Figure 5.13 Synthesis report of area requirement

5.6.1.4 Delay output

With ever increasing speed of integrated circuits, violations of the performance specifications are becoming a major factor affecting the product quality level. Delay is defined as the length of time it takes for a signal to travel to its destination. As an example, in an electric signal, it is the time taken for the signal to travel through a wire. Typical propagation delays: < 100 ps. Figure 5.14 shows synthesis report of delay

```
Delay:               23.755ns (Levels of Logic = 18)
  Source:            b<2> (PAD)
  Destination:       encout<2> (PAD)

  Data Path: b<2> to encout<2>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             13   1.218   1.062  b_2_IBUF (b_2_IBUF)
     LUT2:I1->O             5   0.704   0.712  Mxor_even_Result<5>1 (even<5>)
     LUT4:I1->O             6   0.704   0.844  Madd_fa2_addsub0001_xor<0>11 (evenfa2<0>)
     LUT4:I0->O             2   0.704   0.526  Madd_fa4_addsub0001_xor<0>11 (fa4<0>)
     LUT3:I1->O             3   0.704   0.566  Madd_fa6_addsub0001_cy<0>11 (Madd_fa6_addsub0001_cy<0>)
     LUT3:I2->O             3   0.704   0.610  Madd_fa7_addsub0001_xor<0>11 (fa7<0>)
     LUT4:I1->O             2   0.704   0.526  hd1_cmp_lt0000147_SW0 (N844)
     LUT4:I1->O             1   0.704   0.000  hd1_cmp_lt00001821 (N878)
     MUXF5:I1->O            3   0.321   0.706  hd1_cmp_lt0000182_f5 (hd1_cmp_lt0000)
     LUT3:I0->O             5   0.704   0.712  hd1<1>1 (hd1_1_OBUF)
     LUT4:I1->O             1   0.704   0.455  encout_cmp_lt0001147_SW0 (N854)
     LUT3:I2->O             1   0.704   0.499  encout_cmp_lt0001147 (encout_cmp_lt00011_map17)
     LUT4:I1->O             5   0.704   0.808  encout_cmp_lt0001182 (encout_cmp_lt0001)
     LUT3:I0->O             1   0.704   0.000  encout<0>1_G (N865)
     MUXF5:I1->O            6   0.321   0.704  encout<0>1 (NO)
     LUT3:I2->O             1   0.704   0.000  encout<2>262 (N881)
     MUXF5:I0->O            1   0.321   0.420  encout<2>26_f5 (encout_2_OBUF)
     OBUF:I->O                  3.272          encout_2_OBUF (encout<2>)
    ----------------------------------------
    Total                     23.755ns (14.605ns logic, 9.150ns route)
```

Figure 5.14 Synthesis report of delay

5.6.2 Power Tool

This thesis involves the usage of Xilinx and Tanner EDA power tools. The power products are tools that comprise a complete methodology for low-power design. Xilinx power tool XPower offers power analysis and optimization throughout the design cycle (from RTL to the gate level). Analyzing power early in the design cycle can significantly affect design quality. Improvements made at RTL level can get even better results. Not only the power tools do accurate measurements but also can help in

calculating power quickly. Power consumption is calculated at three levels. The tools used in these levels are

a) RTL Level - RTL Power Estimator

b) Gate Level – Power Compiler (based on switching activity),

c) Transistor Level – Tanner EDA

Power analysis and estimation is available throughout the design process, as shown in the following Figure 5.15.

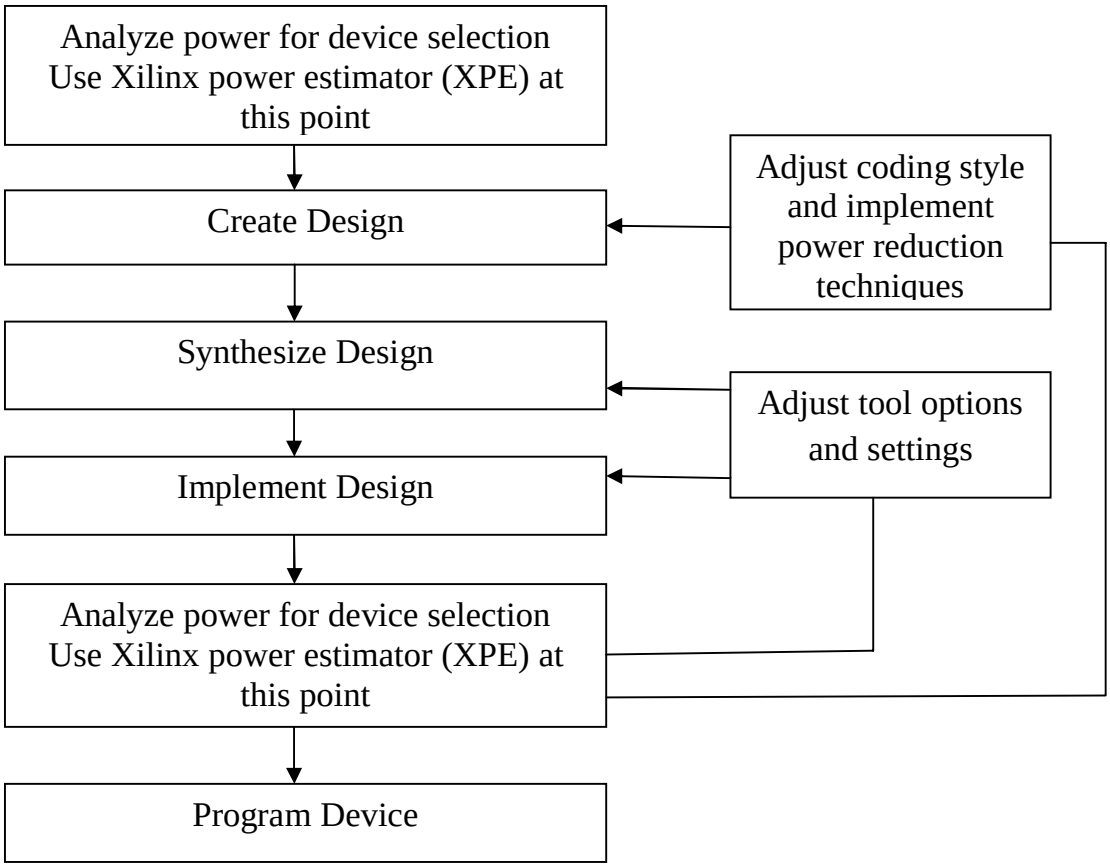

Figure 5.15 Power analysis flow chart

5.6.2.1 XPower analysis tool

XPower works on the principle of “activity rates” and are defined as the rate at which a net or logic element capacitance switches. For dynamic power calculation, activity rates are expressed as a frequency. An activity rate

may be relative to clock and in that the net or logic element switches at some percentage of the clock frequency. This is often referred to as a toggle rate. Activity rates are very useful because they enable to recalculate the power by merely changing the system clock frequency. This allows the user to use original simulation data and save time. XPower supports any number of input clocks. Expressed as a percentage, an activity rate of 100% means that a signal state change happens on average once every clock cycle with the resultant frequency being half the associated clock. For nets and logic that are not synchronized with a clock, the activity rate will be the switching rate. Figure 5.16 shows power output of encoder circuit.

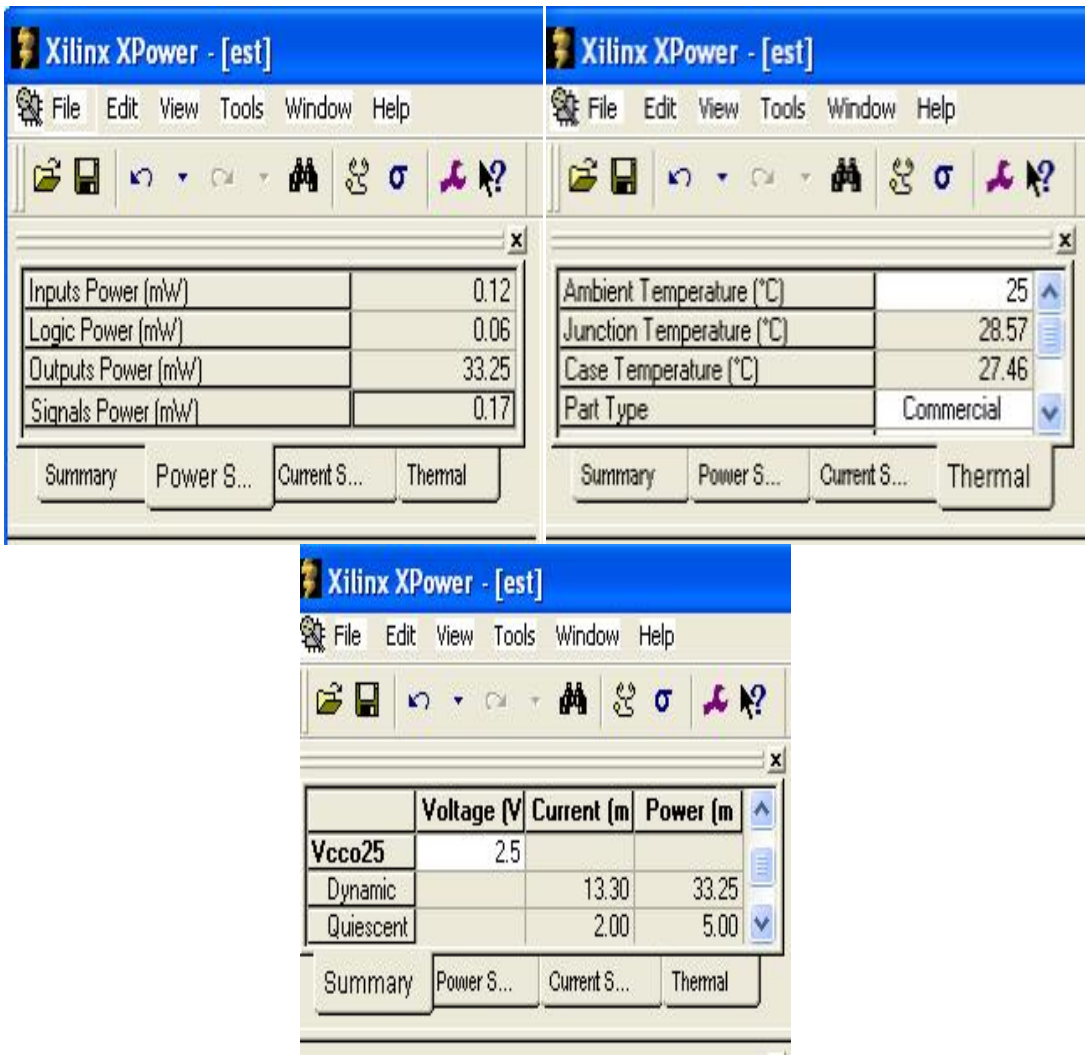

Figure 5.16 Power output using Xpower

From this analysis in multi coding techniques dynamic power dissipation up to 33.25mw which is equivalent to the output power of the encoder circuit. The ambient temperature is 28^{o}C and the junction temperature is 28.57^{o}C. Increasing of temperature will automatically affect the delay time of the design.

5.7 CONCLUSION

Estimating maximum power dissipation for a CMOS logic design is difficult because the power dissipated by the logic design is typically a strong function of the logic inputs. This implies that the number of simulations which must be performed in order to find the maximum power dissipation. It is concluded that maximum power dissipation is due to maximum gate output activity. The proposed multi coding technique reduces the transition activity. So the overall power dissipation is 33.25 mw and saved power upto 66.75 mw. In order to reduce the area and power dissipation of the circuit further, CPL full adders are implemented instead of using Logic Full adder in the Transition estimator. Now the overall power dissipation is reduced to 28.972mw and 10 % power improvement is achieved.