CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

This chapter introduces various research works done on data compression, data encoding and transition estimation. This work deals with implementation of efficient methods to transmit the data through interconnect with reduced power dissipation and the related works done on data compression, data encoding and Hamming distance estimator techniques. Also, the merits and limitations of the existing methods are analyzed with proposed method to reduce the transition activity

2.2 DATA COMPRESSION

Nowadays data compression is a very essential tool in the multimedia applications. Most of the research work deals with coding for text data compression, some of them are listed below for reference

David Huffman (1952) developed a Method for Construction of Minimum-Redundancy Codes, an optimum method of coding an ensemble of messages consisting of a finite number of members. Minimum redundancy code is constructed in such a way that the average number of coding digits per message is minimized. An optimal coding of an ensemble of messages using three or more types of digits is similar to the binary coding procedure.

Written et al (1987) introduced arithmetic Coding for Data Compression. Here, an accessible implementation of arithmetic coding and detailing of its performance characteristics are analyzed. Wolfe & Chanin (1992) have been executing compressed programs on an embedded RISC architecture in their approach; a system with code compression incorporates an instruction cache which holds uncompressed code and a main memory which holds compressed code. Huffman codes have been used to encode an instruction cache.

Howard & Vilter (1992) developed, Practical implementation of arithmetic coding showing how it provides nearly optimal data compression and how it can be matched with almost any probabilistic model. Based on reduced precision arithmetic coding, which gives only minimal loss of compression efficiency , use the concept compressed tree a new data structure for efficiently representing a multi symbol alphabet by a series of binary choices.

Jer Min & Pei (1999) have analyzed fast and efficient lossless data-compression method on online lossless data compression method using adaptive arithmetic coding. In order to achieve compression efficiency an adaptive fuzzy-tuning model that applies fuzzy inference to deal efficiently with the problem of conditional probability estimation and a novel division-free adaptive arithmetic coding method that can be easily realized with VLSI technology. With the help of fuzzy inference can achieve better compression results for various types of source data.

Lekatas et al (2000) have introduced code compression for low power embedded system design to minimize area and power (2005). Approximate arithmetic coding for bus transition reduction in low power designs was implemented to minimize bus related bit toggling.

Abul Kalam et al (2005) have developed an efficient technique for text compression for storing a word or the whole text segment, and need a huge storage space. A character usually requires one byte for storing in memory. So compression of memory is important for data management. In case of memory requirement lossless compression is needed for text data, word lookup table will make any text segment able to use lesser memory space but will not decrease its features rather will increase its usability and portability.

Mohammed & Ibrahiem (2007) developed, Comparative Study between Various Algorithms of Data Compression Techniques. The spread of computing has led to an explosion in the volume of data to be stored on hard disks and sent over the Internet. This provides a survey of data compression Techniques to reduce the amount of data storage or internet bandwidth required to handle the data. Most prominent data compression schemes are focused here by using different compression algorithm, the compression ratio and compressed file size is analyzed.

Vikas singla et al (2008) introduced data compression modeling huffman and arithmetic basic concepts of data compression and introducing the model based approach that underlies most modern techniques. Then the arithmetic coding and Huffman coding for data compression are presented, and finally the performance of arithmetic coding is analyzed. The ability of arithmetic coding to compress the text file is better than Huffman in many aspects because it accommodate adaptive models and provide separation between model and coding.

Jagadish & Lohit (2010) introduced a new lossless method of image compression and decompression using Huffman coding techniques. The raw images need large amounts of disk space seems to be a big disadvantage during transmission and storage. The Lossless method of image

compression and decompression uses a simple technique called Huffman coding which utilizes less memory. Compression and decompression techniques based on Huffman coding and decoding reduces data volume and application time.

Kodituwakku & Amarasinghe (2010) developed Comparison of Lossless Data Compression Algorithms for Text Data. Even for a single data type there are numbers of different compression algorithms using various approaches and compares their performance. Algorithms are selected, examined and implemented to evaluate performance in compression. Comparison of different lossless compression algorithms for text data has been performed and compared for their effectiveness.

Senthil & Robert (2011) introduced text compression algorithms - a comparative study provides a survey of different basic lossless data compression algorithms. Comparisons of the lossless compression algorithms using Statistical compression techniques and Dictionary based compression techniques were performed on text data. The algorithms such as Huffman coding, Shannon-Fano Coding, Run Length Encoding, Adaptive Huffman coding and Arithmetic coding are considered for statistical compression.

Xiaoke Qin et al (2011) have developed decoding-aware compression of FPGA Bit streams. Bit stream compression is important in reconfigurable system design since it reduces the bit stream size and the memory requirement. It also improves the communication bandwidth and thereby decreases the reconfiguration time. The decoding-aware compression technique tries to obtain both best possible compression and fast decompression performance. The proposed compression technique analyzes the effect of parameters on compression ratio and chooses the optimal ones automatically.

Zirrapeter & Gregory (2011) developed Radical Data Compression Algorithm Using Factorization. Proposal involves factorization techniques in conjunction with lossless data compression and decompression method for exploiting the size of memory thereby decreasing the cost of the communication. The new data compression transforms a string of characters into a new string using compression key and reverses the encoded string using decompression key. The encoded string contains the same information as the original string but whose length is small as possible.

Omar et al (2012) implemented a novel approach an convert audio compression to text coding via hybrid technique. For data transmission, compression can be performed on just the data content or on the entire transmission unit depending on a number of factors an audio compression method by using text coding where audio compression represented via convert audio file to text file for reducing the time to data transfer by communication channel. Lossy compression methods are used on sound files in order to obtain good compression ratio, it is obvious that the amount of information loss will have a minor effect on the outcome.

Nathanael et al (2012) have introduced comparative analysis of lossless text compression techniques. Data compression is an effective means for saving storage space and channel bandwidth. This paper deals with lossless compression techniques named Arithmetic, Golomb, LZ-78 and Huffman coding. Comparative analysis was performed on compression efficiency and speed. Huffman coding is optimal when the probability of each input symbol is a negative power of two. Huffman fails to compress the data in large amount when the symbols have skewed probability and long runs as compared to Arithmetic and RLE based Golomb coding respectively.

Katugampola (2012) developed A new technique for text data compression. This paper presents how ternary representation of numbers can be utilized to compress text data with fixed-symbol-length coding techniques. Using binary map for ternary digits and introduce a method to use the binary 11-pair and further use 4-Digits ternary representation of alphabet with lowercase and uppercase letters and then find a way to minimize the length of the bits, which is possible in ternary description and thus efficiently reducing the length of the code. Also some connection between this technique of coding data and Fibonacci numbers was found out.

Jinder & Monica (2013) developed A Survey on the different text data compression techniques**.** It is very useful as it helps us to reduce the resources usage, especially data storage or transmission capacity. Different basic lossless data compression methods are considered. The methods such as Shannon-Fano Coding, Huffman coding, Run Length Encoding and Arithmetic coding are considered. Lempel Ziv scheme is a dictionary based technique. In the Statistical compression method, Arithmetic coding performs with an improvement over Huffman and Shannon-Fano and over Run Length Encoding technique.

Rexline et al (2013) have developed semi-adaptive substitution coder for lossless text compression. The rapid advantage of this Substitution Coder is that it substitutes the code words by referring the reference of the word position in the dictionary to expedite the dictionary mapping and also code words are shorter requires less space. Text transformation required an external dictionary to store the frequently used words. To preserve this transformation method in a healthy way, a semi-adaptive dictionary is used and therefore which reduces the expenditure of memory overhead and speeds up the transformation because of the smaller size dictionary. This new

transformation algorithm is implemented and tested using Calgary Corpus and Large Corpus.

Pooja et al (2013) introduced data compression techniques: A comparative study. This paper discussed image compression and its need, principles and classes of compression and various algorithm of image compression. Here author's attempts to give a recipe for selecting one of the popular image compression algorithms based on Wavelet, JPEG/DCT, VQ, and Fractal approaches. The data compression algorithms require a great deal of processing power to analyze and then encode data into a smaller form. Creating a general purpose compressor that can take advantage of parallel computing should greatly reduce the amount of time it requires to compress large files.

Malathi & Ramya (2013) developed Reduction of Bus Transition for Compressed Code Systems. The main focus here is to present a method for reducing the power consumption of compressed-code systems by inverting the bits that are transmitted. Compression increases bit-toggling, as redundancies are removed from the code transmitted on the bus. Arithmetic coding is useful for compression /decompression and bit-toggling reduction is done by using shift invert coding technique. Combination of Arithmetic Coding and Shift-invert Coding for reducing bus transitions and thereby reduce the power consumed in embedded systems

Alish & Anjali (2015) have introduced a survey on data compression techniques in wireless sensor network. In this survey explain a different simple efficient data compression algorithm which suited to be used on available many commercial nodes of a wireless sensor network, where energy, memory and computational resources are limited. Some experimental results and comparisons of lossless compression algorithm formerly proposed

in the literature to be inserted in sensor nodes. Hence data compression methods are used to minimize the number of bits to be transmitted by the transmission module will significantly lessen the energy requirement and maximize the life expectancy of the sensor node. The present explanation of the study contracted with the sketching of systematic efficient data compression algorithm, particularly suited for wireless sensor network.

Pooja et al (2015) developed improving data compression ratio by the use of optimality of Lzw & adaptive Huffman algorithm**.** In this paper, a two stage data compression Algorithm that is OLZWH which uses the Optimality of Lempel- Ziv-Welch (OLZW) and Adaptive Huffman Coding has been proposed. With this proposed Algorithm, the data Compression ratios are compared with existing Compression Algorithm for different data sizes. The proposed technique has a great scope of modifications to make it suitable for large size files also by populating the dictionary with combination of character of phrase instead of the phrase itself and removing phrases not used for longest period of time if the dictionary gets filled. This method is very suitable for image compression.

2.3 DATA CODING

The importance of data coding technique is to reduce the data transition between data on parallel buses or neighboring data within the bus. Various research works carried out in reduction of power dissipation using data coding technique. Some of them are listed below.

2.3.1 Coding Scheme for Reduction of Power Dissipation

Stan & Burleson (1995) developed bus invert coding for Low power I/O. In this scheme entire buses are used for encoding purpose and

include a redundant bit along with bit line. This scheme is simple and effectively reduces the switching activity. The bus invert method was explained in the particular setting of dynamic I/O power dissipation the same method can be applied in any case where large capacitances are involved.

Yoo & Choi (1999) introduced interleaving partial bus invert coding for low power reconfiguration of FPGAs. The authors propose a bus encoding scheme which partitions the configuration of data sequence of an FPGA into sub sequences and applies partial bus invert coding to each sub sequence to reduce the number of data bus transitions while reconfiguring FPGA. The proposed method gives more reduction of bus transitions on average compared with the conventional bus invert coding, partial bus invert coding and beach coding.

Further, PBI is again extended with decomposed bus invert coding for low power I/O proposed by Hong et al (2000). This paper proposes a new bus-invert coding scheme for reducing the number of bus transitions. In this scheme, the bus lines are partitioned and each partitioned group is considered independently for bus-invert coding to maximize the effectiveness of reducing the total number of transitions. Results verify that the decomposed bus-invert coding scheme reduces the total number of bus transitions on average than those of the conventional and the partial bus-invert coding schemes respectively.

Sotiriadis & Chandrakasan (2000) developed Low power bus coding technique considering interwire capacitances. The power dissipation with driving data buses would be significant, when considering the increasing interwire capacitance. Transition reduction is not necessarily the best approach for reducing power when the effects of interwire capacitance are taken into consideration. Bus model designed for data buses with submicron

technologies is presented and a family of coding techniques is proposed that can reduce the average power consumption of the bus.

Similar to this encoding scheme, Partial bus invert coding for power optimization of application specific systems is proposed by Youngsoo Shin et al (2001). It presents two encoding scheme named as Partial Bus-Invert coding (PBI) and its extension to Multiway Partial Bus-Invert coding (MPBI). In the first scheme, only a selected subgroup of bus lines is encoded to avoid unnecessary inversion of relatively inactive and/or uncorrelated bus lines which are not included in the subgroup. In the extended scheme, partition a bus into multiple sub buses by clustering highly correlated bus lines and then encode each sub bus independently to describe a heuristic algorithm of partitioning a bus into sub buses for each encoding scheme.

Zhang et al (2002) developed odd/even bus invert with two phase transfer for buses with coupling. In this scheme the authors considered the numbered bus line and also coupling capacitances will charge and discharge by the activity of the neighbors. One line will be odd and the other neighbor line will be even. To reduce the coupling activity by independently controlling the odd and even bus lines with two separate lines, Odd Invert and Even Invert line to obtain significant reductions in power simply by comparing the coupling activity for the four possible cases of the Odd and Even Invert lines (00, 01, 10, 11), and then choosing the value with the smallest coupling activity to be transmitted on the bus. So after encoding, the transistion for a pair of bus lines is still strongly dependents on data. The toggling sequences 01→10 and 10→01 result in 4 times more coupling energy dissipation than other coupling events.

Youngsoo & Takayasu (2002) have introduced power distribution analysis of VLSI interconnects using model order reduction. The analysis and simulation effect induced by interconnects become increasingly important as

the scale of process technologies steadily shrinks. In this paper the power distribution analysis of interconnects is studied using reduced model. The difference between power consumption and the poles and residues of a transfer function is derived and a simple yet accurate deriver model is developed, allowing power consumption to be computed effectively.

The silent technique is proposed by Lee et al (2004) to reduce power dissipation in the serial bit line. In this scheme, data is coded as XOR between the continuous data words. In the receiver side, original transmitted data word can be recovered by XOR of encoded word and previously decoded words.

Lin Xie et al (2005) have developed partitioned bus coding for energy reduction. This paper proposes the bud partition scheme for the Transition pattern Coding (TPC). The genetic algorithm based approach is used. A closed form of expression is derived to calculate the energy dissipation for the partitioned bus with TPC coding. The bus lines are shuffled and portioned in order to minimize the total energy reduction. The resulted portioned bus coding reduces the encoding and decoding complexity.

Youngsoo & Junghyup (2006) have introduced power analysis of VLSI interconnect with RLC tree models and model reduction. The existence of wire resistance ignored by the lumped capacitance model, which has been estimate the charging and discharging power consumption of CMOS circuits. During this study it was revealed that about 20% of the power is consumed in the wire resistance of the buffered global interconnect, when an interconnect is modeled with RC tree networks. The power distribution analysis of interconnect with RLC tree networks based on a reduced order model. The separate evaluation of the driver and the interconnect contribution is very useful to understand the sources of energy dissipation.

Massimo et al (2006) introduced energy consumption in RC tree circuits. In this paper, resistance, capacitance tree networks are modeled in terms of their energy consumption associated with an input transition. Based on Single pole approximation, the energy consumption circuits are modeled and equivalent time constant is also analytically derived from an exact analysis for very slow and very fast I/P transitions. Then this model is extended to arbitrary values of the input rise time by exploiting some intrinsic properties of RC tree networks. This method is fully analytical and leads to closed-form results.

Transition skewing coding scheme proposed by Akl & Bayoumi (2007) reduces power dissipation and area. This scheme deals with area, noise, cross talk, peak energy and signal integrity and switching and leakage power. The authors used 90nmtechnology to simulate. The encoded bus is compared against a standard bus and a bus with shields inserted between every two wires. The encoding and decoding latencies are also analyzed. Simulations show that transition skew coding is efficient in terms of energy and area with low encoding and decoding latency overhead. This work has been further extended in 90nm encoding scheme considering 2 GHz global clock frequency (2008).

Kalyan et al (2008) have developed exploiting variable cycle Transmission for energy efficient on chip interconnect design. It propose a scheme which exploits both dynamic voltage scaling and variable cycle transmission mechanisms for minimizing on chip interconnect energy consumption. Transmit data using variable cycle transmission method, based on the delay saving achieved through variable cycle transmission method at frequent intervals. To obtain energy saving by scale the voltage and frequency.

Verma & Kaushik (2010) have introduced encoding schemes for reduction of power dissipation, crosstalk and delay in VLSI interconnects: A Review. This paper reviews different encoding schemes for reduction of delay, power dissipation and crosstalk noise. Crosstalk is aggravated by enhanced switching activity which is often main cause for the malfunctioning of VLSI chip. Therefore delay and power dissipation also increases due to intensified crosstalk. Switching activities are reduced through coupled transmission line results in enormous reduction of power dissipation. The researchers therefore often concentrate on encoding scheme that reduces the transitions of the signals.

Venkateswara & Tilak (2011) developed a bus encoding to reduce crosstalk noise effect in system on chip. This paper proposes a new bus coding scheme for reducing the crosstalk in System on chip (soc). As circuit geometries become smaller, wire interconnections closer together and longer, so the cross-coupling capacitance increased between nets. Meanwhile, parasitic capacitance to the substrate is less as interconnections become closer and circuit delays are reduced as transistors become smaller. Substrate capacitance is the dominant effect for circuit geometries at 0.25 micron and above. On the other hand with geometries at 0.18 micron and below, the coupling capacitance between nets becomes significant.

Karunamoy & Subhashis (2012) developed a novel method for analysis of power consumption in VLSI global interconnects. The analysis of effects induced by interconnects become increasingly important as the scale of process technologies shrinks. The analysis method based on a reduced order model and discrete domain Z transform. Power consumption can be computed efficiently in Z-domain using an algebraic formulation, instead of improper integration in time domain. The theoretical outcome relies on the

pole and residues of transfer function can be used in any kind of model order reduction technique.

Padmapriya (2013) introduced modified bus invert technique for low Power VLSI design in DSM technology. Here peak power for most possible power dissipation is a critical design factor as it determines the thermal and electrical restrictions of designs, system cost, size and weight, specific battery type, component and system packaging and heat sinks, and aggravates the resistive and inductive voltage drops. Hence it is necessary to have the peak power in control. The cross talk is reliant on the data transition patterns on the bus. Consequently the proposed bus invert encoding design is suitable for reducing the power dissipation and cross talk delay in VLSI circuits.

Sanjay et al (2013) developed Reduction of Sub threshold Leakage Current in MOS Transistors. Here NMOS and PMOS are simulated in different layout techniques show considerable reduction in sub threshold leakage and junction leakage currents by the use of double-finger and four-finger techniques. Junction and sub-threshold leakage reduction is observed by varying different parameters in single NMOS and PMOS transistors. So the memory is fabricated by large number of PMOS and NMOS transistors and also can be reduce leakage current in memory.

Nima et al (2014) introduced data encoding techniques for reducing energy consumption in network-on-chip. A set of data encoding schemes aimed at reducing the power dissipation in the links of a NoC. Experiments carried out on both fake and real traffic scenarios show the effectiveness of the design. This scheme used to minimize not only the switching transition, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep submicron meter technology regime

Amit & Jyoti (2014) developed an energy efficient advanced low power CMOS design to reduce power consumption in deep Submicron technologies in CMOS circuit. Here an energy efficient and ecofriendly techniques were focused for calculation of power-dissipation in various components and also the determination of different ways to reduce the total power consumption in a CMOS device. This technique has less power dissipation than the conventional CMOS design style.

Kanchan & Deshmukh (2015) proposed Power Optimization of Combinational Quaternary Logic Circuits. By the need of interconnections design of the binary logic circuits is restricted. Interconnections increase energy consumption, area and delay in digital CMOS circuits. Multiple valued logic full adder can decrease the average power needed for transitions and reduces the number of required interconnections using unique encoding technique.

Prabhakaran & Shenbagavelrajan (2015) have developed modified data encoding and decoding scheme for data transmission in network-on-chip. The dynamic power dissipation in network on chip is due to the self-switching and cross coupling capacitance. In the encoding scheme the self-switching is decreased by checking the switching transition and then the coupling technique is included with the routed network, which is encoded by the network interface before they are injected in the network and are decoded by the destination network interface. The encoding scheme on a set of data showing that it is possible to reduce the power consumption for both self and coupling switching activity in inter router links.

2.3.2 Coding Scheme for Reduction of Self and Coupling Transition

In CMOS circuits most power is dissipated as dynamic power due to switching transition during charging and discharging of load capacitance.

Transition activity is classified in to self transition and coupling transition. In this field most of the research work analyzing coupling transition, self transition and combined both self and coupling transition techniques to reduce the power dissipation.

Sumant et al (1999) introduced a coding frame work for low power address and data busses presents a source coding frame work for design of coding schemes to reduce transition activity. In this frame work a data source is first passed through a decorrelating function f_1 ,Next, a variant of entropy coding function f_2 is employed, which reduces the transition activity. In this scheme incremental xor (inc-xor) method for address bus and probabilistic based mapping xor (xor-pbm) method for data bus is used to encode the data to reduce transition activity.

Vijay & Keshab (2000) have developed reducing bus transition activity by limited weight coding with codeword slimming. Number of transitions can be reduced by introducing redundancy in data transferred through the busses. For a given repetition there exists a lower bound on the average number of switching activity. A new coding technique that leads to extremely practical techniques for bus transmission that reduce bus transitions to the lower bound depending on the redundancy employed was derived. There is also a net reduction in power dissipation over an uncoded bus transmission scheme. Applications suitable for this new technique include systems relying on bit-serial implementation and systems with bit-parallel implementations where the cost of extra parallel-to-serial and serial-to-parallel data-format converters is marginal compared to the power savings obtained.

Ki-Wook et al (2000) proposed coupling driven signal encoding scheme for low power interface design. Coupling effects between on-chip interconnects must be addressed in ultra deep submicron VLSI and system-

on-a-chip designs. Here low-power bus coding is introduced to minimize coupled switching which dominate the on-chip bus power dissipation. The coupling-driven bus inverts method use slim encoder and decoder architecture to minimize the hardware overhead.

Jorg & Harish (2001) have analyzed an adaptive address bus coding (A^2BC) for low power deep sub micron designs that take coupling effects in to consideration. The basis is a physical bus model that quantifies coupling capacitances. Due to larger buses and deep sub micron effects where coupling capacitances between bus lines are in the same order of magnitude as base capacitances, power consumption of interconnects starts to have a significant impact on a systems total power consumption. The A^2BC scheme is applied in the two stages ACCS and LSIS. Together eventually lead to power energy saving compared to the gray encoding scheme that is considered the best low transition encoding scheme for address buses.

Madhu et al (2003) designed chips for low power applications is one of the most important challenges faced by the VLSI fabricators. Because the power dissipated by I/O pins of CPU is a significant source of power consumption. Dynamic coding technique for low power data bus encoding scheme developed for reducing switching activity on external buses. This technique considers two logical groupings of bus lines, each being a permutation of the bus and energetically chooses the grouping which yields the minimum number of transitions.

Naveen et al (2004) has implemented a novel deep submicron bus coding for low Energy. In present digital circuits the total amount of power distributed to wires is increasing. Reducing power dissipation in wires plays a major role in low power design. Coupling transitions afford to significant energy loss in deep sub-micron buses. The simulation results show that this technique reduces the coupling transitions for a deep sub-micron bus

compared to the conventional non-coded data transmission. As this method is adaptive, it reduces signal transmission for all sorts of data streams.

Menon et al (2004) introduced switching activity minimization in combinational logic design. The reduction of switching activity in combinational logic design an algorithmic way using karnaugh map has been proposed which modifies the normal optimal solution obtained from k-map to reduce its switching activity. More than 10% reduction in switching activity has been observed using this method. The final solution gives a good tradeoff between cost and power consumption.

Tina et al (2004) have developed deep sub micron bus invert coding presents a deep sub micron bus invert coding for on chip parallel data buses. Similar to bus invert coding technique it is used to realize low complexity encoding and decoding circuitry, and with a complexity that scales linearly with the bus width. By introducing redundancy it is possible to reduce the energy dissipation in on chip parallel data buses.

Muroyama et al (2005) introduced a variation aware low power coding methodology for tightly coupled buses. Variable length coding is proposed to reduce the self capacitance and switching power. Probabilistic information is used to for assigning the code. The smaller length code is assigned for more frequent data, in which the major sources of the power consumption are the activities on the signal lines and the coupling capacitances of the lines.

Avnish et al (2006) proposed an adaptive low power bus encoding based on weighted code mapping. The WCM algorithm transforms an original bus data vector to a low-energy code through 1-to-1 mapping. It is determined by the data probabilistic distribution in the original progression. The Weighted code mapping considers the self and coupling capacitance of

the bus wires. Window-based adaptive coding method is proposed to improve the energy saving by adaptively changing the code mapping for different data probabilistic characteristics. The authors extended their work in another encoding scheme is called as Low power bus encoding using an adaptive hybrid algorithm (2006), in which the WCM algorithm is combined with delayed bus encoding technique will further reduce the bus energy.

Sainarayanan et al (2006) introduced coding for minimizing energy in VLSI interconnects. The main target of VLSI designers is to minimize the switching activity on the on-chip buses. Authors introduced a bus encoding technique which minimizes both self and coupling transition activity to curtail the global power consumption. Simulation results shows that the proposed method is suitable for the continually shrinking technology and low power VLSI applications.

Madhu (2007) introduced CMOS process technology scaling to deep submicron level. Delay in long on-chip buses is becoming one of the main performance limiting factors in high speed designs. Propagation delay is most important when adjacent wires are transitioning in opposite direction as compared to transitioning in the same direction.. This work proposes a technique, namely, selective shielding, to eliminate crosstalk transitions. Selective shielding significantly reduces the number of extra wires which gives a lower bound on the number of wires required to encode n-bit data

Sathish et al (2011) proposed an efficient switching activity reduction technique for on chip data bus. In many digital processors and SoC the switching activity results into dynamic power dissipation on the data buses and interconnects which is a major part of the total chip power dissipation Switching activity is due to coupling transitions and self transitions. Power reduction of the VLSI chip is one of the major challenges in the Deep sub-micron technology. One of the best methods to reduce the

transitions is to encode the data on the data bus lines. Thus an efficient switching transition reduction technique is proposed which can reduce the overall transitions.

Shankaranarayana & Yogitha (2012) introduced universal rotate invert bus encoding for Low power VLSI. Switching activity is one of the factors that affect dynamic power in a chip and several publications have suggested various techniques to reduce the same. Reduction of switching activity in the busses attains significance as bus width; bus capacitance and the clock are recording continuous uptrend. In this paper, a technique for bus encoding has been proposed which reduces the number of transitions on the bus and performs better than the existing methods such as bus invert coding and shift invert coding for random data in terms of switching activity, without the need for extra resources in computation and design the circuit. Though, impartial of the bus width it needs three extra bits and does not assume anything about the nature of the data on the bus.

Verma & Kaushik (2012) developed a bus encoding method for crosstalk and power reduction in RC coupled VLSI interconnects. The crosstalk effect is a consequence of coupling and switching activities that is encountered when there is a transition as compared to previous state of wire and or when there are adjacent transitions. So minimizing switching and coupling activities is crucial in enhancing the performance of System on chip designs. Several methods are followed for power dissipation reduction, delay and crosstalk. Encoding is most effective and popular method for enhancing the behavior of buses on - chip. The transition reduction improves performance in power dissipation reduction, coupling activity and delay in on-chip buses.

Nagendra Babu et al (2012) proposed Bus encoder for crosstalk avoidance in RLC models. In recent years most encoding methods deal with

only RC modeled VLSI interconnects. In deep submicron (DSM), inductive effects have increased due to faster clock, smaller rise times and longer on-chip interconnects. All these raise power dissipation, propagation delay and crosstalk. So, this research introduces an efficient Bus Encoder method using Bus Inverting (BI). This proposal reduces both crosstalk and power dissipation in RLC modeled interconnects which makes it suitable for current high-speed low-power VLSI interconnects.

Padmapriya (2013) proposed for low power bus encoding for deep sub Micron VLSI circuits. In recent year's low power and power awareness has become a major driving force especially due to portable electronics and the growing cost of the power dissipation. DSM bus power dissipation is directly related to the switching activity of the coupling capacitance that exist between the bus lines and also the switching activity of the self capacitance present between the bus interconnect and the ground. The technique used here is to reduce the switching activity of both self and coupling capacitances through encoding the data on buses.

Mullainathan & Ramkumar (2014) proposes switching reduction through data encoding techniques in Network on chip. Here encoding scheme is used to reduce the power dissipation and the energy consumption of the communication system in NoC. On-chip interconnect has more significant fraction of the overall system power/energy budget. So in the definition of new methodologies and techniques aimed at optimizing the on chip communication system not only in terms of performance but also in power. The method followed is, encoding the packets before they are injected into the network in such a way as to minimize both the switching activity and the coupling switching activity in the NoC's links which represent the main factors of power dissipation.

Devendra Kumar et al (2014) have introduced FDTD based transition time dependent crosstalk analysis for coupled RLC interconnects based on FDTD analysis of transition time effects on crosstalk. The investigation carried out is for equal and unequal transition times. The unequal rise time effects are also equally important because, it is common to have mismatch in the rise time of the signals transmitting through different wire length. As an example, two distributed RLC lines coupled inductively and capacitive are considered. The FDTD method is followed because it gives accurate results and carries time domain analysis of coupled lines.

2.4 HAMMING DISTANCE ESTIMATOR

It is necessary, on buses, to calculate how many numbers of transitions had occurred during data transmission. Transition is equivalent to Hamming distance between the data on buses. To estimate transition activity different kind of design methodology is followed. Among different works carried out, few methods are listed here.

Radhakrishnan et al (1984) proposed formal design procedures for pass-transistor switching circuits. Formal design methods are presented to realize pass logic networks in NMOS and CMOS technologies. One is a modified Karnaugh minimization and is effective for design of networks up to five or six variables. For networks involving more than 6 variables, an algorithmic method is proposed by modifying the conventional Quine-McCluskey. Silicon area savings depends on transistor count as well as interconnect. Maximum regularity for pass transistors can be achieved in the intersection of the set of control variables with the set of pass variables in null set and which allows pass and control variables to flow at right angles to each other.

Chandrakasan et al (1992) developed low power CMOS digital design. Motivated by emerging battery-operated applications that demand intensive computation in portable environments, techniques are investigated which reduce power consumption in CMOS digital circuits while maintaining computational throughput. Techniques for low-power operation are shown which use the lowest possible supply voltage coupled with architectural, logic style, circuit, and technology optimizations. An architecturally based scaling strategy is presented which indicates that the optimum voltage is much lower than that determined by other scaling considerations. This optimum is achieved by trading increased silicon area for reduced power consumption

Parameswar et al (1994) proposes a low power, high speed, pass-transistor logic based multiply and accumulate circuit for multimedia. Swing Restored Pass-transistor Logic is a high speed, low power logic circuit technique for VLSI applications. By the using pass-transistor to perform logic estimation, and a latch circuit to drive gate outputs, this method provides very good circuit performance. In double metal 0.4 μm CMOS technology Mac circuit for multimedia applications is implemented based on SRPL. The work is extended in 1996 as swing based restored pass transistor logic based multiply and accumulates circuit for multimedia application.

Uming Ko et al (1995) proposed low-power design techniques for great performance of CMOS adders and is the most critical components of a processor which determines its throughput, since is used in ALU, the floating unit and in generation of address in cache and memory access. Low-power design methods for various digital circuit families are studied for make high-performance adders, an optimization performance per watt or energy and area efficiency. Investigation is performed using 100 MHz, 32 b CLA adders in 0.6 μm CMOS technology. The techniques used here can also be applied to

other parallel adder algorithms such as carry-select adders (CSA) and other energy efficient CMOS circuits.

Kazuo Yano et al (1996) introduced top-down pass-transistor logic design. The cell library and synthesis tool are constructed based on pass-transistor, to clarify potential of the logic. The entire method is known as Lean Integration with Pass-Transistors (LEAP). The feature is its multiplexer function and the open-drain formation. Transistor level design could be achieved in cell and compatibility with conventional cell based design. A simple cell with only seven cells combined with a synthesis tool called "circuit inventor" is compared with the conventional CMOS library that has over 60 cells combined with the state-of-the-art synthesis. The results explain that delay, area and power dissipation are enhanced by LEAP and that the value-cost ratio is improved by a factor of three.

Shams & Bayoumi (1997) introduced structured approach for designing low power adders. Analysis of a 1-bit full adder cell is provided. The cell is anatomized into minor modules using the proposed approach. The modules are studied comprehensively and several designs of each connecting combinations of designs of these modules together construct 24 different 1-bit full adder. Each of the cells shows different area, power consumption, speed and driving capability. Some cells outperform present standard designs of the full adder cell.

Radhakrishnan (2001) developed low voltage low power CMOS full adder. A design procedure for creeating a minimal transistor CMOS pass network XOR-XNOR cell that is fully compensated for threshold voltage drop in MOS transistors is offered. This cell can operate within certain bounds when the power supply voltage is brought down and due consideration provided to the sizing of the MOS transistors during initial design. Low transistor full adder using the XOR-XNOR cell is also presented.

I-Chyn et al (2002) proposed a new low voltage CMOS 1 bit full adder for higher performance. The design consists of combining exclusive OR \ exclusive XNOR gates, used in full adder transmission gates. The proposed adder can provide full voltage swing at a low supply voltage and offers superior performance in both power and speed than the usual, the transmission and low-voltage full adders. Model results taken from HSPICE, the new design consumes less power and has a minimal power-delay product in the TSMC 0.35 μm process.

Kishore Kumar et al (2011) introduced Design of low power full adder using asynchronous adiabatic logic. These circuits are low power circuits and conserve energy. A full adder using asynchronous adiabatic logic with complementary pass transistor, which exhibits low power and reliable logic operations comprising the benefit of both asynchronous systems with adiabatic benefits. Asynchronous adiabatic adder circuits consume less energy than the conventional quasi adiabatic designs. This confirms the possibility of asynchronous adiabatic full adder circuits in low power applications.

Praveer Saxena et al (2011) developed design of 1 bit full adder for low power applications. The full adders designed are compared on the basis of transistor counts to implement the full adders, propagation delay and average power consumed by them for different values of load capacitance and input frequency. The result also compared with full adders designed with static CMOS. It is observed that, full adders designed with adiabatic logic styles consume very low power in comparison to full adder designed with static CMOS logic.

Sunil Gavaskar & Rajendra Prasad (2011) developed Power comparison of CMOS and adiabatic full adder circuits. Apart from basic addition adders also used in performing useful operation such as address

calculation, subtraction, division, multiplication etc. In every such system the adder will be in the critical path that determines the overall performance of this method. Here usual complementary metal oxide semiconductor and adiabatic adder circuits are analyzed in terms of power and transistor count.

Sazzad Hossain et al (2011) developed a new design technique of reversible BCD adder based on NMOS with pass transistor gates. This paper proposes a new design technique of BCD Adder using newly constructed reversible gates are based on NMOS, where conventional one's are based on CMOS. Also evaluating proposed one with conventional CMOS reversible gates which shows the required number of transistors is significantly reduced. The design is very useful for the future computing techniques like low power digital circuits and quantum computers.

Ramkumar & Harish (2012) introduced low power and area efficient carry select adder. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From CSLA structure, it is very clear that there is scope for area reduction and power use in CSLA. This method uses efficient gate-level modification to significantly reduce the area and power. Based on the above provided modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA design. The proposal achieved reduced area and power as compared with the regular SQRT CSLA.

Venkata Siva & Venkataiah (2012) proposed design of adder in multiple logic style for low power VLSI. The main consideration for design and implementation of various logics and Arithmetic operations like adder, are basic pass transistor approach due to their high operating speed and low

power dissipation. The aim of the paper is designing carry skip adder based on different technologies such as CPL (Complementary Pass Transistor Logic), DCVSPG (Differential Cascade Voltage Swing Pass Gate topology), SRPL (Swing Restored Pass Transistor Logic), and EEPL (Energy Economized Pass Transistor Logic). The performance can be compared by considering various parameters such as power consumption, delay, area, transistor count and PDP (Power Delay Product).

Channegowda & Aswatha (2013) developed low power 1 bit full adder cell using modified pass transistor logic. Adders have become one of the important components in the digital world. Adders are mostly used in functions like Dividers, Multipliers and Subtractions etc. In VLSI adders are used as the basic component from processors to ASIC's. Hence a well optimized Adder design is required. Area, Power and Propagation delay are acceptable Quality metrics of the designed products. Recent days has proved that the use of Complementary Pass Transistor Logics (CPL) has provided a drastic reduction in the power compared to CMOS logic.

Neva Agarwala (2014) introduced high speed CPL adder for digital biquad filter design. The paper describes how to minimize the overall delay of a Digital Biquad Filter by comparing the time delay performance analysis among different adders. At last, eight bit adder is used in design methodology of this Biquad Filter for its excellent performance in timing delay computation. Finally, the design was fully functional and the time delay was less compare to others. For full adder cell design, pass-logic circuit is thought to be dissipating minimal power and have smaller area because it uses less number of transistors. Hence, CPL is considered to perform better than CMOS.

Syed Saleem & Maheswara Reddy (2014) introduced a VLSI Implementation of Fast Addition Using an Efficient CSLAs Architecture. Carry Select Adder (CSLA) is a fast adder used in data processing processors for performing fast mathematical functions. From the formation of CSLA, its scope is area reduction and the area of CSLA based on efficient gate-level changes. But, usual CSLA is area-consuming due to the dual Ripple-Carry Adder structure. To decrease area, CSLA could be constructed by using a single RCA and an add-one circuit instead of dual RCA. The customized CSLA architecture was developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using latch-D. Trial outcomes are compared and its analysis shows that the proposed architecture achieves the two folded advantages in terms of area and delay.

Gopala Krishnan & Rachelin (2014) introduced system design for encoding and decoding to minimize the crosstalk in VLSI circuits. Global buses in deep-submicron (DSM) system-on-chip designs consume significant power, have large delays and are liable to errors due to DSM noise. Hence, crosstalk event on long on-chip buses is increasingly becoming a limiting factor in very-speedy designs. Also crosstalk among adjacent wires may create a significant portion of the delay. Keeping shield wire in between each signal wire alleviates the crosstalk problem but doubles the area used, which is undesirable. Instead, employ data encoding and decoding for a special codes called boundary shift codes to minimize crosstalk within a bus has been employed.

Kumar & Prashant (2014) developed a report on low power VLSI circuit design. Low power became a major factor where power dissipation has become as important consideration as performance and their area so there is a

need of low power. A new family of logic styles called preset Skewed Static Logic (PSSL) has been projected. PSSL connects gap between two logic styles, static CMOS and domino, taking place an transitional region in the energy-delay-robustness space among the two. This proposal reviews known strategies and methodologies for designing low power circuits.

Abhijeet & Vishal (2014) developed power reduction in digital VLSI circuits. The main objective is to reduce power dissipation in digital CMOS VLSI circuits. Compare all the optimal methods which can reduce maximum power dissipation among all and with fewer limitations. Using Galaxy Custom Designer a tool of Synopsys and SPICE coding to find out energy, power, delay and leakage charge with various design styles like CMOS, Pass transistor, DCVS (Differential cascade voltage swing logic circuit), Dynamic, DCVS-PG. Computed the delay, power, energy and power leakage and compared amongst these design styles to conclude which design style would work for the specific requirement.

Basant Kumar & Sujit Kumar (2014) introduced area delay power efficient carry select adder. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation sum, different from usual approach. Bit patterns of carry words (corresponding to cin = 0 and 1) and fixed cin bits are used for logic optimization of CS and making units. A competent CSLA design is got by optimized units. This design involves extensively less area and delay than the recently proposed BEC-based CSLA.

2.5 CONCLUSION

In this chapter an overview of data compression, data coding and Hamming distance estimation techniques are discussed. Various lossless data compression techniques like run length encoding, Huffman coding, arithmetic

coding and dictionary based compression principles are analyzed. Apart from all existing techniques, a novel technique named as simple byte compression algorithm for text data is developed for lossless compression. To encode the data several encoding techniques like Bus invert coding, Shift invert method, A^2BC, Beach solution, gray coding, universal rotate, MDSMBC and NBCMEI coding techniques are analyzed and a novel coding method called multi coding technique is used to encode the entire data. During data transmission Hamming distance estimator is used to estimate the transition activity. Several full adders' like logic full adder, CSL, SDSL, DDCVSL, DRDL, DPL and SDCVSL are used to implement the Hamming distance estimator to do the arithmetic functions. Among the full adders mentioned above pass transistor logic (CPL) is used to implement the Hamming distance estimator as it takes less area and low power than other methods.