ABSTRACT

Synthesis of reversible logic has become a very important research area. According to Moore’s law the number of transistors on an Integrated Circuit (IC) doubles every 18 months. Due to this exponential growth physical boundaries will be reached in near future. Furthermore power consumption of the ICs has become a major issue and hence heat dissipation problems emerge. This is due to limited battery life since there is lack of technology advancement in battery. Quantum computers are the suitable alternative to the classical systems. Here information is stored in the form of qubits instead of bits. In addition, the bits of information are lost in irreversible logic which dissipate energy at the rate of kTln2 per bit lost where k is Boltzmann constant and T is the temperature of the system. Quantum computing uses reversible logic which doesn’t lose any information bit and thus allow higher densities and speed with reduced power and energy dissipation. Thus reversible logics find ample applications in design of present day portable systems. Reversible circuits (gates) are logics that have one to one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. Thus, the research orients towards design of arithmetic circuits for binary and Binary Coded Decimal (BCD) addition and subtraction using reversible logic with enhanced performance in terms of reduced gate count, constant input, garbage outputs and delay making it suitable for quantum computing.

The objective of the thesis is to design various architectures for binary and decimal addition and subtraction using novel and efficient
reversible gates. The proposed binary and decimal units are designed using library of reversible gates implemented with structural VHDL code. Experimental evaluation using simulations revealed that the proposed reversible binary and BCD designs perform significantly better with fewer gate counts, constant inputs, garbage outputs and delay compared to similar approaches proposed in literature. The optimization of the proposed BCD adder/subtractor designs using carry skip logic for reversible adder stages reduces delay further compared to the basic version, with little expense in gate count.

Next, the unified architecture proposed for binary/BCD, addition/subtraction though increases complexity it perform well in optimizing the area and delay compared to previous similar approaches. Finally, binary to BCD converter proposed for decimal multiplication performs fine in terms of fewer gate counts, constant input, garbage output and lower delay compared to approaches used for comparison.