CHAPTER 7

CONCLUSION

Synthesis of certain efficient arithmetic circuits for binary and decimal arithmetic suitable for quantum applications have been proposed in this thesis. Reversible logic is used and the designs are realized using simple and efficient reversible logic gates. As more features are integrated within battery powered electronic devices like cell phones, laptops nowadays, it drains the battery quickly. So the need for new technology or circuit technique is necessitated to reduce power dissipation and area of arithmetic units used in processing elements. Various circuit design techniques and algorithms are proposed for arithmetic units using reversible logic.

7.1 DESIGN OF HIGH SPEED REVERSIBLE BCD ADDER

Chapter 2 presents the design of high speed BCD adder using reversible logic. The proposed BCD adder uses reversible full adder for first stage addition and a MPS gate to convert the binary output of first stage adder to equivalent decimal. Evaluation of the proposed BCD adder design is done in terms of number of reversible logic gates, garbage outputs, number of constant inputs and delay. Results demonstrated that the proposed design perform significantly better compared to previous approaches in area and delay reductions with the number of gates and delay reducing by at least 60% compared to the previous best designs used for comparison. The functionality of the proposed reversible BCD design is verified by implementation in two
digit addition. It is seen from the implementation results that the proposed design can be extended for higher digit addition with ease. In addition better performance improvement of the proposed reversible BCD design reveals that it can be used for design of larger computational structures and in quantum computing.

7.2 DESIGN OF HIGH SPEED HARDWARE EFFICIENT CARRY SKIP ADDER AND CARRY SKIP BCD ADDER USING REVERSIBLE LOGIC

Chapter 3 concentrates on efficient design of a carry skip adder using reversible logic. The proposed carry skip adder uses efficient reversible gates viz., MTSG for first stage addition and PG for carry skip logic. To verify the functionality of the proposed reversible CSK adder it is implemented in the BCD adder for first stage addition. MPS gate is used to convert the output of first stage adder to equivalent decimal. The proposed CSK adder and CSK implemented decimal adder are compared with the previous approaches in terms of gate count, number of constant inputs, number of garbage outputs and delay. The evaluation results revealed that both circuits are highly optimized in terms of gate count, constant input and garbage output when compared with the existing designs. For example the gate count, garbage output and constant input of proposed CSK adder show atleast 6 gate, 8 outputs and 8 inputs reductions with the respective percentages to be 42.9%, 42.1% and 53.3% for 4 bit input and its BCD counterpart show the corresponding reductions to be at least 4 gates, 3 outputs and 3 constant inputs with respective percentages to be 30.7%, 21.4% and 30% for 1 digit addition. As a result, the proposed reversible binary and
decimal adders are applicable in portable quantum computing to reduce cost and area.

7.3 AN EFFICIENT REVERSIBLE DESIGN OF BCD ADDER - SUBTRACTOR AND CARRY SKIP BCD ADDER- SUBTRACTOR

Chapter 4 deals with the design of reversible BCD adder/subtractor and its optimization using carry skip adder for binary addition. The proposed BCD adder/subtractor uses NCG and reversible adder for tens complement conversion of subtrahend in case of subtract operation. In addition, reversible adders perform addition of tens complement of subtrahend (in case of subtract operation) or the actual value of the input (in case of addition operation) with the other input. To reduce carry propagation delay in reversible adder stage, an implementation with CSK adder is done. The proposed reversible BCD adder/subtractor and carry skip BCD adder/subtractor are compared with Rajmohan et al (2011) approach in terms of gate count, number of constant inputs, number of garbage outputs and delay. By evaluations of the proposed design, it is shown that the gate count, constant inputs and garbage outputs are significantly reduced compared to Rajmohan et al (2011) design. Also it is shown that the average delay can be reduced upto 0.5 gate delay by CSK adder implementation in the carry propagate additions used, with a little expense in area overhead. Consequently, the proposed decimal adder/subtractor and its delay optimized counterpart can be used in quantum/reversible computing requiring decimal arithmetic units.
7.4 A REVERSIBLE DESIGN OF UNIFIED BINARY AND BINARY CODED DECIMAL ADDER / SUBTRACTOR

Chapter 5 discusses the design of reversible architecture for binary and binary coded decimal addition / subtraction. The proposed approach uses efficient reversible 4 bit adder and BCD detection and correction circuit to realize the logic. Experimental evaluations using simulations revealed that the proposed approach is able to incorporate four different logics within the same circuit and able to operate with minimal delay per total gate count. This in turn reveals the suitability of proposed approach for low power and high speed quantum applications. As a further work the carry look-ahead logic can be implemented in the reversible addition stages to optimize delay further with a little expense in area.

7.5 DESIGN OF REVERSIBLE BINARY TO BINARY CODED DECIMAL CONVERTER FOR BINARY CODED DECIMAL MULTIPLICATION

Chapter 6 discusses the design of reversible binary to binary coded decimal converter suitable for binary coded decimal multiplication. The proposed reversible binary to BCD converter consists of pair of MPS gate to generate decimal equivalent of binary input, BCDH and BCDL gates along with pair of reversible adders are used for generating equivalent decimal values at the corresponding digit position. Performance evaluation is done by comparing the performance parameters with prior design in terms of gate count, number of constant inputs, number of garbage outputs and delay. Since the reversible gates used in the proposed design have tiny count, this tends to reduce the overall area of the converter design. In addition, the
reduced constant inputs and garbage outputs of the reversible gates used in the proposed design lead to considerable cost reduction in the final design. Implementation results revealed that the gate count, constant inputs and garbage outputs show at least 69.3%, 65.6% and 68.8% reductions compared to previous approach. Thus it can be assured that the proposed design is suitable for portable decimal processors and in building more complex computational structures.

7.6 PERFORMANCE ESTIMATES OF PROPOSED REVERSIBLE CIRCuits

The performance metrics viz., gate count, number of constant inputs, number of garbage outputs and delay of the proposed reversible circuits are shown Table 7.1. It is observed from Table 7.1, that the delay efficient reversible BCD adder proposed in chapter 2 perform well in terms of gate count and delay reductions compared to previous approaches with at least 60% area and delay reduction compared to previous best of the approaches. The implementation results of the delay efficient BCD adder in two digit addition demonstrates the functionality of the proposed reversible BCD adder.

The proposed CSK adder discussed in chapter 3 show better performance in terms of gate count, constant inputs, garbage outputs and delay reductions compared to previous approaches mentioned in the literature. An implementation of proposed reversible CSK adder in decimal adder revealed better performance in gate count and average delay reductions compared to the state-of the art BCD designs.
The proposed reversible BCD adder/subtractor discussed in chapter 4 show significantly better performance in terms of gate count and garbage output reductions with the respective percentages to be 30.6% and 45.9% compared to previous novel architecture. However the implementation of CSK adder reduces the delay of the reversible BCD adder/subtractor with little increase in gate count.

**Table 7.1 Gate count, number of constant inputs, number of garbage outputs and delay estimates of proposed reversible circuits**

<table>
<thead>
<tr>
<th>Design</th>
<th>Gate count</th>
<th>No. of constant inputs</th>
<th>No. of garbage outputs</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed reversible BCD adder</td>
<td>5</td>
<td>4</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>Proposed reversible BCD adder( 2 digit addition)</td>
<td>17</td>
<td>14</td>
<td>20</td>
<td>16</td>
</tr>
<tr>
<td>Proposed CSK adder</td>
<td>8</td>
<td>7</td>
<td>11</td>
<td>3.5*</td>
</tr>
<tr>
<td>BCD adder using proposed CSK adder</td>
<td>9</td>
<td>7</td>
<td>11</td>
<td>4.5*</td>
</tr>
<tr>
<td>BCD Adder/- Subtractor</td>
<td>25</td>
<td>18</td>
<td>20</td>
<td>23</td>
</tr>
<tr>
<td>BCD Adder/- Subtractor(CSK optimized)</td>
<td>29</td>
<td>21</td>
<td>25</td>
<td>22.5*</td>
</tr>
<tr>
<td>Unified Binary &amp; BCD adder / subtractor</td>
<td>70</td>
<td>53</td>
<td>55</td>
<td>42</td>
</tr>
<tr>
<td>Binary to BCD converter</td>
<td>15</td>
<td>21</td>
<td>20</td>
<td>11</td>
</tr>
</tbody>
</table>

* - average delay
The proposed unified binary/BCD adder/subtractor proposed in chapter 5 performs better performance in optimizing area and delay compared to other similar approaches used for comparison.

The proposed binary to BCD converter discussed in chapter 6 perform more than 50% reduction in gate count, constant inputs and garbage outputs compared to architecture mentioned in literature.

7.7 FUTURE WORK

The proposed reversible arithmetic designs viz., both for binary and decimal addition and subtraction perform fine in terms of gate count, constant inputs, garbage outputs and delay reductions compared to the architectures proposed in literature. Similarly the binary to BCD converter proposed in the thesis perform extra ordinarily well compared to previous approaches. An implementation of these proposed reversible designs in an Arithmetic and Logic Unit (ALU) can be done to verify their suitability for high speed quantum applications.