CHAPTER 5

A REVERSIBLE DESIGN OF UNIFIED BINARY AND
BINARY CODED DECIMAL ADDER / SUBTRACTOR

5.1 INTRODUCTION

The high growth of integration of present day ICs increases power density enormously. This inturn poses serious threats in terms of heat generation and much care has to be taken to dissipate this heat. As stated earlier the energy dissipation of KTln2 joules occurs for every bit of information where K is Boltzmann’s constant of $1.38 \times 10^{-23}$ J/K and T is the absolute temperature of the environment and this has been proved by Landauer (1961). In this context reversible logics emerge which have almost zero energy dissipation. A reversible circuit is one which does not lose any information when compared with the irreversible logic circuit or conventional combinational logic circuits. In other words irreversible circuit can be converted to reversible by saving all the information which it will discard otherwise. Therefore the attention towards reversible concept has reached greater heights in recent years especially in areas of quantum computing.

In computer systems, the most common numbering system that is followed is binary numbers. However there are computers that use decimal
numbering system rather than binary number system. Such systems have found its importance in commercial, financial and internet based applications. Although binary arithmetic is used in wide variety of applications there is always an assumption that decimal arithmetic is better for the financial applications. Recognizing the decimal arithmetic, the specifications of decimal floating point arithmetic is added in the draft revision of IEEE P754 (http://754 r. Ucbtest.org/drafts/754r.pdf). Moreover floating point numbers are represented with desired precision in decimal format rather than binary representations (Hayes 1998). Inspite of its high level of accuracy the decimal arithmetic is 100 to 1000 times slower than binary arithmetic (Cowlishaw 2010). These advantages and disadvantages have urged the hardware designers to add decimal and binary arithmetic unit in Central Processing Unit (CPU) to perform arithmetic calculations (Wang et al 2010). Analyzing all these aspects, a narrative design for unified binary and BCD addition/ subtraction is proposed in this chapter.

5.2 BACKGROUND OF REVERSIBLE LOGIC GATES USED IN THE PROPOSED DESIGN

The logic representation and operation of the reversible gates used in proposed arithmetic units are briefed as follows.

5.2.1 PTM Gate

The proposed 3x3 reversible PTM gate discussed in section 2.6 of chapter 2 is used for generating carry and sign bit of the output. The third
input (C) of PTM gate is kept constant as 1 and 0. The gate produces 2 garbage outputs along with the result and has a quantum cost of 11.

5.2.2 HNG

The HNG discussed in section 2.2 of chapter 2 is a 4 * 4 reversible gate (Haghparast & Navi 2008a) used to realize three bit addition. The gate width of HNG is found to be 4. The gate requires one constant input, 2 garbage outputs and thus has a quantum cost of 6.

5.2.3 BVF Gate and FG

The 4*4 BVF gate (Bhagyalakshmi & Venkatesha 2010) discussed in section 4.3.5 of chapter 4 is used in the design of 16 * 16 copying circuit to be used in the proposed binary/BCD adder/subtractor.

The architecture of FG is discussed in section 4.3.5. FG does the same function as that of BVF gate except that it has a single XOR gate. Also it is noted that the quantum cost of BVF gate is 2.

5.2.4 R-Comp Gate and R-Op Gate

The logic representation and quantum diagram of R-Comp and R-Op gates are shown in Figure 5.1 and Figure 5.2 respectively. Logic diagram, reversible implementation and quantum representation of TR gate and TG used in R-Comp and R-Op are shown in Figure 5.3 and Figure 5.4 respectively.
Figure 5.1 R-Comp gate (a) Logic diagram (b) Reversible implementation (c) Quantum representation
Figure 5.2 R-Op gate (a) Logic diagram (b) Reversible implementation (c) Quantum representation
Figure 5.3 TR gate (a) Logic diagram (b) Reversible implementation
(c) Quantum representation

Figure 5.4 TG (a) Logic diagram (b) Reversible implementation
(c) Quantum representation
5.2.5 SCL Gate

The SCL gate is used for the detection of overflow of output. SCL gate produces a logic 1 if the output exceeds 9 and vice versa. Quantum representation of SCL gate is shown in Figure 5.5. Note that from Figure 5.5 the quantum cost of SCL gate is 7.
5.3 PROPOSED BINARY/BCD ADDER/SUBTRACTOR ARCHITECTURE

The proposed architecture for binary and BCD addition/subtraction consists of copying circuit, binary comparator, reversible multiplexer, two’s complement circuit, 4 bit reversible adder, BCD detection and correction circuit and FG and PTM gates and is shown in Figure 5.6.

A brief description of the blocks used in the proposed architecture are as follows.

a) Copying Circuit

The proposed binary/decimal adder/subtractor consists of two copying circuits. The copying circuit-1 is designed using 4*4 BVF gate (Bhagyalakshmi & Venkatesha 2010) and consists of 8 BVF gates to produce 3 copies of inputs A and B as shown in Figure 5.7. 2 copies of A and B are
given as input to two multiplexers and third other copy is given as an input to reversible comparator. In the next design i.e. copying circuit-2 shown in Figure 5.8, two BVF gates and one FG gate are used. This circuit is used for duplicating 4 bit adder output and for copying the carry bit of the adder.

Figure 5.6  Proposed binary/BCD adder/subtractor
Figure 5.7 Copying circuit-1

Figure 5.8 Copying circuit-2
b) Binary Comparator

The binary comparator (Thapliyal et al 2010) used in the proposed binary/BCD adder/subtractor for comparing two binary inputs uses three R-Comp gates and one R-op gate and is shown in Figure 5.9. For the case of 4 bit inputs $A (a_3a_2a_1a_0)$ and $B (b_3b_2b_1b_0)$, the first stage comparator does comparison of two consecutive bits using a pair of R-Comp gates. The output of the R-Comp gates is fed to another R-Comp gate at the second stage. The output of the second stage R-comp gate is fed to reversible R-op gate to produce the final result. The output of R-op gate will be 010 for $a>b$, 001 for $a<b$ and 100 for $a=b$. Since the quantum cost of R-comp gate is 18 and reversible output circuitry is 9, the 4 bit binary comparator has a quantum cost of 63 (3*18+9).

![Figure 5.9 Binary comparator](image)

**c) BCD Detection and Correction Circuit**

BCD detection and correction circuit used in the proposed binary/BCD adder/subtractor design consists of SCL gate, FG, Peres gate and HNG (Bhagyalakshmi & Venkatesha 2010) and is shown in Figure 5.10.
SCL gate is used for the detection of overflow and FG, PG and HNG are used to convert the output to equivalent decimal based on the control signal from SCL gate.

\[ \text{Figure 5.10 BCD detection and correction circuit} \]

Since the quantum cost of FG, PG and HNG are 1, 4 and 6 respectively, the quantum cost of BCD detection and correction circuit counts to 18.

d) Two’s Complement Circuit

The two’s complement circuit used in the proposed design for binary and BCD addition/subtraction uses a 4 bit reversible adder, designed using HNG discussed in section 2.2 of chapter 2. The architecture of two’s complement circuit is shown in Figure 5.11. Since subtraction operation is similar to adding two’s complement of subtrahend with the other input, two’s complement circuit is used to convert the binary bits of subtrahend to equivalent 2’s complement form. To achieve this, two’s complement circuit uses a NOT gate and a reversible adder. NOT gate is used to find one’s complement of the input and reversible adder is used to add one to the NOT gate output to generate equivalent two’s complement value. Since the
quantum cost of NOT gate is 1 and HNG is 6, the quantum cost of two’s complement circuit counts to 28 (4*6+4*1).

![Diagram of a 4-bit reversible adder](image)

**Figure 5.11 Two’s complement circuit**

e) Reversible Multiplexer

The proposed design uses four 2:1 reversible multiplexers constructed using FR gate. The operation of the reversible multiplexer is discussed in section 4.3.4 of chapter 4.

5.3.1 Principle of Operation

The design uses two’s complement method (Anshul Singh et al 2009) for both binary and BCD subtraction. The main criterion to be noted is that the magnitude of subtrahend must be always smaller than the minuend. To satisfy this criterion the inputs A and B are passed through a 4 bit binary comparator block (Thapliyal et al 2010) to find whether A> B or A<B or A=B. The comparator output is used as the select signal for the multiplexers. The output of multiplexers will be such that the magnitude of minuend (reversible multiplexer 1 output) is greater than the subtrahend (reversible
Table 5.1 Output of reversible multiplexers

<table>
<thead>
<tr>
<th>Condition</th>
<th>Output of Reversible Multiplexer1</th>
<th>Output of Reversible Multiplexer2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A&gt;B (010)</td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>A&lt;B (001)</td>
<td>B</td>
<td>A</td>
</tr>
<tr>
<td>A=B (100)</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

The output of the reversible multiplexer-2 is passed through a twos complement circuit controlled by Add/Sub output of FG. For addition operation, Add/Sub is equal to zero and the bits at the reversible multiplexer-2 output will be passed as such to the reversible adder. In case of subtraction operation, Add/Sub is equal to one and the bits at the reversible multiplexer-2 output will be two’s complemented and passed to the reversible adder. The other input to the reversible adder is the output from reversible multiplexer-1. The output of the reversible adder is fed to copying circuit-2 to produce two copies. One of the outputs of copying circuit-2 is fed to a BCD detection and correction circuit to produce the decimal equivalent. The output of BCD detection and correction circuit and other output of copying circuit-2 are passed through reversible multiplexer-3. The control signal for the reversible multiplexer-3 is a BIN/BCD input. Based on the BIN/BCD input either the binary or decimal equivalent of reversible adder output will be passed out. PTM gates are used to generate the carry output. The input to one of the PTM gate is the output of BCD detection/correction circuit and Add/Sub control input, and for the second PTM gate the inputs are copying circuit output and Add/Sub control signal. To detect sign bit, a separate PTM gate is used.
whose input is the output of binary comparator and Add/Sub bit. The algorithm for the proposed binary and BCD adder/subtractor for \( n = 4 \) is shown in Figure 5.12

Let \( A = (A_3, A_2, A_1, A_0) \) and \( B = (B_3, B_2, B_1, B_0) \) be the two inputs.

**Control Input bits:** Add/Sub, Bin/BCD

**Carry bits:** \( C, C_{in} \) and \( C_{out} \)

**Output bits:** \( I(I_3, I_2, I_1, I_0) \) – Intermediate output

\[ S(S_3, S_2, S_1, S_0) \text{and } D(D_3, D_2, D_1, D_0) \] – Final outputs

**Step 1:** Compare \( A \) and \( B \). If \( B \) is greater than \( A \) swap \( A \) and \( B \).

**Step 2:** If \( \text{Add/Sub} = 0 \) then

\[ B_4 B_3 B_2 B_1 = B_4 B_3 B_2 B_1 \]

Else

\[ B_4 B_3 B_2 B_1 = (\overline{B_4} \, \overline{B_3} \, \overline{B_2} \, B_1) + 1 \]

**Step 3:** Addition of inputs \( A \) and \( B \)

For \( i = 1 \) to \( 4 \)

\[
\begin{align*}
S_i &= (A_i \text{ XOR } B_i \text{ XOR } C_{i-1}) \\
C_i &= (A_i \text{ XOR } B_i) \, C_{i-1} \text{ XOR } A_i B_i \\
i &= i + 1
\end{align*}
\]

**Step 4:** Carry bit computation using PTM gate

If \( \text{Add/Sub} = 0 \) and \( C_4 = 1 \) then

\[ C_{out} = 1 \]

Else if

Add/Sub = 0 and \( C_4 = 0 \) then \( C_{out} = 0 \)
Elseif
Add/sub = 1 and C₄ = 0 then C₄out = 0
Else
Add/sub = 1 and C₄ = 1 then C₄out = 0

Step 5: BCD overflow detection and correction
If I (I₃, I₂, I₁, I₀) > 1001 then
  S (S₃, S₂, S₁, S₀) = (I₃, I₂, I₁, I₀) + 0110
Else
  S (S₃, S₂, S₁, S₀) = I (I₃, I₂, I₁, I₀)

Step 6: Sign bit computation
If Add/Sub = 0 and R = 0 then S = 0
Else if
  Add/Sub = 0 and R = 1 then S = 0
Else if
  Add/Sub = 1 and R = 0 then S = 0
Else
  Add/Sub = 1 and R = 1 then S = 1

END

Figure 5.12 Algorithm for the proposed binary and BCD adder/subtractor for n = 4

5.4 RESULTS AND DISCUSSION

The proposed reversible binary and BCD adder/subtractor is designed according to the methodology presented in previous section using structural VHDL to produce gate level netlist and synthesized using Xilinx
software. Experimental evaluation of the proposed binary and BCD adder/subtractor design is done in terms of no. of reversible gates, no. of constant inputs, no. of garbage output and quantum cost and are shown in Table 5.2.

Note that, from Table 5.2 that all the blocks used in the proposed design has constant inputs except reversible multiplexers. The total

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Gate count</th>
<th>Constant input</th>
<th>Garbage output</th>
<th>Quantum Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary comparator</td>
<td>23</td>
<td>13</td>
<td>18</td>
<td>63</td>
</tr>
<tr>
<td>Reversible Multiplexer1,2,3</td>
<td>13</td>
<td>-</td>
<td>13</td>
<td>75</td>
</tr>
<tr>
<td>Copying Circuit 1</td>
<td>8</td>
<td>16</td>
<td>-</td>
<td>16</td>
</tr>
<tr>
<td>Copying Circuit 2</td>
<td>3</td>
<td>5</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td>Two’s complement circuit</td>
<td>8</td>
<td>7</td>
<td>8</td>
<td>28</td>
</tr>
<tr>
<td>4-bit reversible adder</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>28</td>
</tr>
<tr>
<td>BCD detection and correction circuit</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>18</td>
</tr>
<tr>
<td>PTM and FG</td>
<td>(3+4)</td>
<td>(3+3)</td>
<td>(6+0)</td>
<td>(33+4)</td>
</tr>
<tr>
<td>Total</td>
<td>70</td>
<td>53</td>
<td>55</td>
<td>270</td>
</tr>
</tbody>
</table>
count of constant inputs of the proposed design is found to be 53 with copying circuit-1 contributing 30%. Also note that the garbage output of the proposed design is 55 with binary comparator contributing a maximum of 32.7%, whereas copying circuit-1, copying circuit-2 and FG do not produce any garbage outputs. Quantum cost defined as the number of primitive reversible gates needed for the reversible circuit design, of the proposed design is found to be 270. The quantum cost of reversible multiplexer is 75 and it is a significant contributor contributing about 30% of the total.

An evaluation of proposed reversible binary and BCD adder/subtractor against several state-of-the-art approaches, whose design structure represent similar topologies and circuits targeted for binary and decimal arithmetic is done. Evaluation results in terms of gate count, number of constant inputs, number of garbage outputs and delay are shown in Table 5.3. In calculating no. of constant inputs and no. of garbage outputs, the constant inputs and garbage outputs of individual gates are found and added to find the garbage outputs and constant inputs of the design. Similarly to calculate delay, the delay of gates in the critical path are estimated and summed to give worst case delay of the entire design. Using the above approach, the delay of the proposed binary/BCD adder/subtractor is calculated as follows. (Symbol $\Delta$ represents unit delay).

\[
\text{Total delay} = 2\Delta_{BVF} + 15\Delta(\text{TR and FG}) + \Delta_{FG} + 4\Delta_{FRG} + 5\Delta(\text{HNG and NOT}) + 4\Delta_{HNG} + \Delta_{BVF} + 4\Delta(\text{SCL,Peres,HNG and FG}) + \Delta_{PTM} + 5\Delta_{FRG} = 42 \text{ gate delays (assuming each gate has equal unit delay).}
\]
Table 5.3 Gate count, garbage output, constant input and delay estimates of proposed binary/BCD adder/subtractor and previous reversible designs

<table>
<thead>
<tr>
<th>Reversible Designs</th>
<th>Gate Count</th>
<th>Garbage Output</th>
<th>Constant Input</th>
<th>Delay</th>
<th>Applicability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rajmohan et al (2011)</td>
<td>36</td>
<td>37</td>
<td>25</td>
<td>26</td>
<td>$n$ bit addition and subtraction</td>
</tr>
<tr>
<td>Rashmi et al (2011)</td>
<td>7</td>
<td>9</td>
<td>5</td>
<td>7</td>
<td>only 4 bit addition and subtraction</td>
</tr>
<tr>
<td>Proposed BCD adder/subtractor</td>
<td>24</td>
<td>28</td>
<td>24</td>
<td>23</td>
<td>$n$ bit addition and subtraction</td>
</tr>
<tr>
<td>Proposed binary and BCD adder/subtractor</td>
<td>70</td>
<td>55</td>
<td>53</td>
<td>42</td>
<td>$n$ bit binary and BCD addition and subtraction</td>
</tr>
</tbody>
</table>

A plot of delay per unit gate count of the proposed and approaches used for comparison is shown in Figure 5.13. It is seen from Figure 5.13 that the delay per unit gate count of the proposed binary/BCD adder/subtractor is significantly low compared to approaches used for comparison. This reveals that the proposed architecture optimizes delay and area significantly better.
5.5 IMPLEMENTATION OF THE PROPOSED BINARY/BCD ADDER/SUBTRACTOR FOR 2 DIGIT/8 BIT ADDITION/SUBTRACTION

To authenticate the functionality of the proposed binary/BCD adder/subtractor an implementation in 8 bit/2 digit addition and subtraction is done as shown in Figure 5.14. The design requires a separate comparator for comparing the most significant 4 bits of inputs A and B apart from the 8bit binary comparator. In case of BCD subtraction, if the 4 MSBs of A is greater than B, then no correction is required else correction factor of 1010 [15] is to be added to the output through the 4 bit reversible adder.
Figure 5.14 Proposed binary/BCD adder/subtractor implemented for 2 digit/8 bit addition/subtraction

The least significant outputs of 8 bit reversible adder \(S_3/D_3 - S_0/D_0\) are passed through the BCD detection and correction circuit which will pass the output without any correction. The carry from least BCD
detection and correction circuitry is added with output of most significant BCD detection and correction circuitry using set of half adders. The outputs of reversible half adders are passed through PTM gate for constant correction. The addition of correction constant by the PTM gate is controlled by the output of Peres gate. The illustration of the above approach is shown through following example.

A (22) : 0010 0010
B(19) : 0001 1001
Output of 8 bit Binary comparator 1 : 010
Output of Reversible Multiplexer 1 : 0010 0010
Output of Reversible Multiplexer 2 : 0001 1001
Add/Sub,Bin/BCD : 1,1
Output of 4 bit Binary comparator 2 : 001
A : 0010 0010
Two’s complement of B : 1110 0111
------------------
: 0000 1001
------------------
Output of BCD detection and correction circuit : 0000 0011
Final output : 0000 0011

The implementation results reveal that the proposed binary/BCD adder/subtractor can be extended for higher bitwidth addition/subtraction with ease.
5.6 Conclusion

In this chapter a novel design for unified binary and BCD adder–subtractor using reversible logic is proposed. The proposed approach uses efficient reversible 4 bit adder, and BCD detection and correction circuit to realize the logic. Experimental evaluations using simulations revealed that the proposed approach is able to incorporate four different logics within the same circuit and able to operate with minimal delay per total gate count. This inturn reveals the suitability of proposed approach for low power high speed quantum applications. As a further work the carry look-ahead logic can be implemented in the reversible addition stages to optimize delay further with a little expense in area.