CHAPTER 2

A NOVEL DESIGN OF HIGH SPEED REVERSIBLE BCD ADDER

2.1 INTRODUCTION

Decimal adders are the crucial elements of processors used for commercial and business applications. Specifications for decimal floating point arithmetic have been added to the draft revision of IEEE-P754 standard for floating point arithmetic, and IEEE 754-2008 (previously known as IEEE 754r) is the ongoing revision to the IEEE 754 floating point standard (http://en.wikipedia.org/wiki/IEEE_754r). The use of decimal arithmetic is most needed for those applications due to the following reasons.

First, most fractional decimal numbers such as 0.1 cannot be exactly represented in binary format and therefore, their approximate representations are used in binary arithmetic operations. This is not tolerable for most financial and commercial applications, which require exact representation in decimal numbers.

Second, the commercial databases contain more decimal data than binary data. Therefore, when the binary hardware is used, the decimal data is converted from decimal to binary and after processing, the binary data
should be converted back to decimal in order to store the result in decimal format. However, the conversion between decimal and binary data causes too much delay and incurs huge power dissipation (Cowlishaw 2003), (Bayrakci & Akkas 2007).

In this context reversible logics emerge as a promising technique for the design of combinational circuits. Reversible circuits (gates) are logics that have one to one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. It has wide application in optical computing, bioinformatics, low power CMOS design, nanotechnology, advanced computing and quantum computation. As per Landauer’s principle, there is an energy dissipation of KTln2 joules for one bit information lost in high technology circuits constructed using irreversible hardware, where K is Boltzmann’s constant (1.38x 10^{-23} J/K) and T is the absolute temperature at which operation is performed (Landauer 1961). Also, in high technology circuits due to high integration the heat that is dissipated is very large when compared to loss of one bit of information at room temperature. In 1973, Bennett demonstrated that the combinational circuits constructed using reversible logic gates can minimize heat dissipation and loss of energy, and also produce zero power dissipation (Bennett 1973).

A novel design of decimal adder with reduced hardware and delay, suitable for portable systems using reversible logic is proposed in this chapter. The proposed area and energy efficient reversible BCD adder uses new reversible logic gate for correction circuitry and equivalent decimal generation, along with an existing reversible gate proposed in literature for first stage binary addition.
2.2 BASIC REVERSIBLE GATES USED IN THE PROPOSED HIGH SPEED DECIMAL ADDER

The basic reversible logic gates that are used in the proposed BCD adder design are FG (Feynman 1985), HNG, TG (Toffoli 1980), FRG (Fredkin & Toffoli 1982), PG (Peres 1985) and a proposed MPS gate.

a) Feynman Gate

A 2* 2 Feynman gate (Feynman 1985) shown in Figure 2.1 can be used to make either a copy of the input or to invert it. For example, if the input vector $I=(1,0)$ then the output vector is $O=(1,1)$ where inversion of second input takes place and if input is $I = (0,1)$ then output is $O=(0,1)$ where copying of input is done.
b) HNG

Figure 2.2 shows the logic diagram of HNG (Haghparast & Navi 2008a) which can work singly as a reversible full adder. To perform its operation it requires only one clock cycle. This gate requires one constant input, but produces two garbage outputs. Thus a 4 bit adder designed for first stage addition using HNG will have 4 constant inputs and 8 garbage outputs as shown in Figure 2.3.
Figure 2.2 HNG (a) Logic diagram (b) Reversible implementation (c) Quantum representation

Figure 2.3 Reversible 4 bit parallel adder using HNG
c) Reversible gate for correction circuit- MPS Gate

In addition to the basic gates the following gate is used for correction circuit in the proposed BCD adder design. In a conventional BCD adder correction circuit is used to detect whether the sum out of first stage binary addition is in excess of 9 and to produce the correction factor 6. The correction factor and the sum outputs of the first stage adder are added by the second stage 4 bit adder to produce equivalent decimal output. To realize the same function a 5*5 reversible MPS gate is designed and is used in the proposed BCD design. The logic diagram of proposed MPS gate is shown in Figure 2.4. The output of the MPS gate will be the equivalent decimal representation of binary sum of the inputs.
Figure 2.4 MPS gate (a) Logic diagram (b) Reversible implementation (c) Quantum representation
The logic function of the MPS gate is as follows.

\[ P = \sum m (10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25) \]
\[ Q = \sum m (8, 9, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31) \]
\[ R = \sum m (4, 5, 6, 7, 14, 15, 16, 17, 22, 23, 24, 25, 28, 29, 30, 31) \]
\[ S = \sum m (2, 3, 6, 7, 12, 13, 16, 17, 20, 21, 24, 25, 26, 27, 30, 31) \]
\[ T = \sum m (1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31) \]

where \( \sum m \) represents the sum of minterms.

**d) New Gate**

The 3 x 3 New Gate (Khan 2002) shown in Figure 2.5 can work singly as a half adder with minimum of one garbage output. This gate is used in the proposed two digit BCD addition.
2.3 PROPOSED 4-BIT BCD ADDER

Figure 2.6 shows the block diagram of the proposed BCD adder for single digit addition. The circuit consists of a 4 bit binary adder constructed using HNGs and correction circuit using MPS gate to adjust binary sum output of stage 1 to equivalent decimal. The digits to be added viz., A (A₃A₂A₁A₀) and B (B₃B₂B₁B₀) are passed through the first stage reversible adder.

The output of the reversible adder is passed through MPS gate to produce the decimal equivalent S(S₃S₂S₁S₀) and carry C₁.

For example consider [9+9]

\[
\begin{align*}
A & = 1001 \\
B & = 1001 \\
\text{Output of adder} & = 10010 \\
\text{Output of MPS} & = 1000
\end{align*}
\]
2.4 EVALUATION OF PROPOSED 4-BIT BCD ADDER

Evaluation of the proposed BCD adder in terms of number of reversible gates, number of constant inputs and number of garbage outputs is given in Table 2.1. It is seen from Table 2.1, that the proposed reversible BCD adder has 5 reversible gates with 4 HNGs gate for first stage addition and 1 MPS gate to convert the first stage output to corresponding decimal equivalent. The number of constant inputs and garbage outputs generated are 4 and 8 respectively. The total delay of the proposed BCD adder is calculated in terms of number of gates in the critical path and their corresponding delay. Let $\Delta$ represents the delay of gate. Then total delay of the proposed BCD adder is calculated as follows.
Total delay = 4ΔHNG+ΔMPS

Where
ΔHNG = delay of HNG, ΔMPS = delay of MPS gate.
Delay of first stage adder= 4ΔHNG
Delay in converting the first stage binary output to equivalent decimal = 1ΔMPS
Total Δ of proposed BCD adder= 5 Gate delays

Table 2.1 Analysis of proposed 4-bit BCD adder

<table>
<thead>
<tr>
<th>Gate</th>
<th>No. of reversible gates</th>
<th>No.of Constant inputs</th>
<th>No.of Garbage Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>HNG</td>
<td>4</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>MPS</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Total</td>
<td>5</td>
<td>4</td>
<td>8</td>
</tr>
</tbody>
</table>

2.5 EXPERIMENTAL RESULTS

To evaluate the functionality and performance of proposed reversible BCD adder, the reversible gates used are designed using structural VHDL and from the submodules the complete design is generated. To ensure fair and accurate comparison, all the reversible BCD adder designs used for comparison viz., Hafiz Md.Hasan Babu & Chowdhury (2005), Biswas et al (2008a), Thapliyal et al (2006), Bhagyalakshmi & Venkatesha (2011), James et al (2007) and Haghparast & Navi (2008a) BCD designs are
<table>
<thead>
<tr>
<th>Reversible BCD Adder Designs</th>
<th>No. of Gates</th>
<th>No. of Constant Inputs</th>
<th>No. of Garbage Outputs</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCD adder (Hafiz Md.Hasan Babu &amp; Chowdhury 2005)</td>
<td>23</td>
<td>17</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>BCD adder (Biswas et al 2008a)</td>
<td>10</td>
<td>7</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>BCD adder (Thapliyal et al 2006)</td>
<td>11</td>
<td>11</td>
<td>22</td>
<td>11</td>
</tr>
<tr>
<td>BCD adder (Bhagyakshmi &amp; Venkatesha 2011)</td>
<td>8</td>
<td>6</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>BCD adder (James et al 2007)</td>
<td>9</td>
<td>7</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>BCD adder (Haghparast &amp; Navi 2008a)</td>
<td>14</td>
<td>17</td>
<td>22</td>
<td>13</td>
</tr>
<tr>
<td>Proposed</td>
<td>5</td>
<td>4</td>
<td>8</td>
<td>5</td>
</tr>
</tbody>
</table>

reproduced in the same design environment. The functionality of the proposed design is verified from simulation outputs using Modelsim. The performance evaluation of proposed BCD design and designs used for comparison in terms of No. of reversible gates, No. of constant inputs, No. of garbage outputs and delay are shown in Table 2.2. The delay values of the
approaches used for comparison are calculated using the similar approach discussed in section 2.4. It is seen from Table 2.2 that the No. of gates in the proposed BCD adder decreases by 78.3%, 50%, 54.5%, 37.5%, 44.4% and 64.3% when compared to designs in (Hafiz Md.Hasan Babu & Chowdhury 2005), (Biswas et al 2008a), (Thapliyal et al 2006), (Bhagyalakshmi & Venkatesha 2011), (James et al 2007) and (Haghparast & Navi 2008a) respectively. This is due to area efficient HNG and MPS gate which realizes first stage addition and its binary output to equivalent decimal conversion respectively with fewer gates. A plot of gate count of proposed BCD adder and previous approaches is shown in Figure 2.7.

Also note that the proposed reversible BCD design demonstrate significant reduction in number of constant inputs and number of garbage outputs when compared to previous approaches used for comparison, with the number of constant inputs and number of garbage outputs decreasing by 33% and 25% respectively compared to the best of the designs used for comparison. In addition, it is noticed that the delay of the proposed design decreases by 3 gate delays with the respective percentage reduction to be 37.5% compared to the best of the approaches used for comparison. This is due to simple MPS gate which realizes decimal equivalent of binary output of first stage adder with a single gate in the critical path. Thus the delay of the proposed BCD adder design depends solely on the first stage adder carry propagation. A plot of delay of proposed BCD adder and previous approaches is shown in Figure 2.8.
Figure 2.7 Gate counts of proposed reversible BCD adder and previous approaches

Figure 2.8 Delays of proposed reversible BCD adder and previous approaches
2.6 IMPLEMENTATION OF PROPOSED BCD ADDER FOR TWO DIGIT ADDITION

To verify the functionality of the proposed BCD adder an implementation in two digit addition is done. The two digit adder is constructed using two 4-bit HNG adder as shown in Figure 2.9. As in the case of single digit BCD adder, MPS gate is used to produce the decimal equivalent of binary output of first stage adder. FG is used to propagate

![Block diagram of proposed BCD adder circuit for two digit addition](image)

Figure 2.9 Block diagram of proposed BCD adder circuit for two digit addition
the carry output from stage 1 of first digit to first stage adder of second digit. PTM gate shown in Figure 2.10 is used to propagate the carry output from MPS gate of first digit to second stage adder of second digit.

PTM gate has one constant input with binary input as 1. The other two inputs are the carry out of adder1 and the carry output of MPS gate. The logic that represents the operation of PTM gate is as follows.

\[ P = \sum m(0,2,3,6) \]
\[ Q = \sum m(3,5,6,7) \]
\[ R = \sum m(0,1,3,7) \]
Figure 2.10 PTM gate (a) Logic diagram (b) Reversible implementation  
(c) Quantum representation

Table 2.3 Implementation results of proposed BCD adder and previous approaches for two digit addition

<table>
<thead>
<tr>
<th>Design</th>
<th>No. of Gates</th>
<th>Constant Input</th>
<th>Garbage Output</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCD adder (Hafiz Md.Hasan Babu &amp; Chowdhury 2005)</td>
<td>47</td>
<td>34</td>
<td>44</td>
<td>38</td>
</tr>
<tr>
<td>BCD adder (Biswas et al 2008a)</td>
<td>22</td>
<td>19</td>
<td>28</td>
<td>19</td>
</tr>
<tr>
<td>BCD adder (Thapliyal et al 2006)</td>
<td>23</td>
<td>28</td>
<td>44</td>
<td>20</td>
</tr>
<tr>
<td>BCD adder (Bhagyalakshmi &amp;Venkatesha 2011)</td>
<td>18</td>
<td>17</td>
<td>26</td>
<td>17</td>
</tr>
<tr>
<td>BCD adder (James et al 2007)</td>
<td>20</td>
<td>18</td>
<td>28</td>
<td>18</td>
</tr>
<tr>
<td>BCD adder (Haghparast &amp; Navi 2008a)</td>
<td>29</td>
<td>36</td>
<td>44</td>
<td>22</td>
</tr>
<tr>
<td>Proposed</td>
<td>17</td>
<td>14</td>
<td>20</td>
<td>16</td>
</tr>
</tbody>
</table>
The implementation results of proposed BCD adder and designs used for comparison for two digit addition are shown in Table 2.3. It is seen from Table 2.3, the number of gates in two digit adder designed using proposed BCD design reduces by 30, 5, 6, 3 and 12 gates with an area reduction of 63.8%, 22.7%, 27.3%, 15% and 41.3% when compared to BCD designs in (Hafiz Md.Hasan Babu & Chowdhury 2005), (Biswas et al 2008a), (Thapliyal et al 2006), (James et al 2007) and (Haghparast & Navi 2008a) respectively, thanks to the MPS gate which realizes correction detection and addition with fewer gates. Also note that the number of constant inputs and garbage outputs in the two digit adder based on the proposed methodology are significantly lower compared to the approaches used for comparison with the number of constant inputs decreasing by 20, 5, 14, 3, 4 and 22 with the corresponding percentage reduction to be 58.8%, 26.3%, 50%, 17.6%, 22.2% and 61.1% and the number of garbage outputs decreasing by 24, 8, 24, 6, 8 and 24 with the corresponding percentages to be 54.5%, 28.6%, 54.5%, 23%, 28.6% and 54.5% compared to two digit designs using (Hafiz Md.Hasan Babu & Chowdhury 2005), (Biswas et al 2008a), (Thapliyal et al 2006), (Bhayyalakshmi & Venkatesha 2011), (James et al 2007) and (Haghparast & Navi 2008a) BCD adders respectively. This is due to significant reduction in number of constant inputs and garbage outputs in the MPS gate used in the detection circuit and PTM gate used in the correction circuitry of the proposed design. A plot of constant inputs and garbage outputs of two digit adder implemented with proposed BCD design and previous designs is shown in Figure 2.11 and Figure 2.12 respectively. From the delay values of the reversible BCD adder shown in Table 2.3 it is seen that the delay of the proposed reversible design decreases by 57.9%, 15.8%, 20%, 5.9%, 11.1% and 27.3% compared to two digit designs using (Hafiz Md.Hasan Babu & Chowdhury 2005), (Biswas et al 2008a),
Figure 2.11 Constant inputs of two digit adder implemented with proposed BCD design and previous approaches.

Figure 2.12 Garbage outputs of two digit adder implemented with proposed BCD design and previous approaches.
(Thapliyal et al 2006), (Bhagyalakshmi & Venkatesha 2011), (James et al 2007) and (Haghparast & Navi 2008a) BCD adders respectively. This reduction in delay is due to use of efficient MPS gate and PTM gate which realizes decimal equivalent of binary output and carry propagation from first digit decimal adder to second digit adder with a single gate delay each.

2.6.1 Illustration of Two Digit Addition Using Proposed BCD Adder

Consider two digit inputs A=99 and B=99. Addition of A and B based on the proposed methodology is as follows.

\[
\begin{array}{cc}
A & 1001 \\
B & 1001 \\
\end{array}
\]

Output of 1st stage adder : 10011 0010 carryout of adder1=> 1
Output of MPS : 11001 11000
Output of PTM : 111
Output of adder3 : 1001 (1001+0000)
**Final Result** : **11001 1000**
2.7 CONCLUSION

In this chapter a novel design of reversible BCD adder is proposed which is highly optimized in terms of number of reversible logic gates, garbage outputs and number of constant inputs. Extensive evaluation of the proposed design demonstrated significantly better performance in area and delay reduction compared to previous approaches. The implementation of the proposed reversible BCD design for two digit addition revealed its functionality. It is seen from the implementation results the proposed design can be extended for higher digit addition with ease. Also the extensive performance of the proposed reversible BCD design reveals that it can be used for building larger computational structures and for quantum computers.