CHAPTER - I

REVIEW OF PHYSICS AND TECHNOLOGY OF OHMIC CONTACTS TO GaAs

INTRODUCTION

Metallization is required for interlinking semiconductor components on an integrated circuit chip as well as to provide communication between the device or circuit and the outside world. Based on current-voltage characteristics, metal-semiconductor interfaces are classified in two ways: Interfaces with linear characteristics called ohmic contacts and those which exhibit rectifying properties named Schottky barriers. In the former, it is necessary to ensure that the resistance presented by the metal-semiconductor junction is very small and can be ignored during the device operation. The Schottky interface, with its associated depletion region possesses a charge dipole and shows rectifying characteristics which in many respects are similar to those of a p-n junction diode.

The purpose of an ohmic contact is to allow electrical current to flow into or out of a semiconductor device. Recent scaling trends and concept of multi-level metallization in a very large scale integration (VLSI) design, have created a genuine demand for dimensionally confined low resistance contacts which also play a key role in efficient operation of microwave power devices. Therefore, the need for extremely low resistance stable contacts has arisen to achieve an optimum performance for the entire family of semiconductor devices.

In the last decade an upsurge in the development of GaAs technology has occurred because this material inherits different and in some respect better electronic properties compared to its counterpart, silicon. The direct band gap and high electron mobility of GaAs have been exten-
sively exploited with the aid of hetero-junction technology. Consequently, GaAs devices enjoy monopoly in the area of opto-electronics and dominate the regime of high speed devices.

One of the most important advantages of devices based on a wide band gap semiconductor like GaAs is that they exhibit low leakage current and therefore, are most suited for applications in hot ambients such as in industries, automobiles, oil, gas & geothermal well logging etc. These devices are also capable of functioning at a high current and power levels which might cause a rise in temperature in the active part of a semiconductor chip. However, there has been insignificant progress in this area, primarily due to two reasons: firstly, a metal on a wide band gap semiconductor usually results in a rectifying junction rather than a low resistance ohmic contact and secondly, contact degradation occurs when the device/circuit encounters a thermal stress.

Eventually, for the development of GaAs circuits with large scale integration and devices for high temperature electronics, thermally stable ohmic contacts with very low resistance are required. Although with the aid of modern spectroscopic techniques like RHEED, LEED, AES, ESCA or XPS, UPS, SIMS, EDAX, EM etc. our knowledge of metal-semiconductor interfaces has substantially enhanced, nevertheless the complete determination of the detailed mechanisms responsible for ohmic behaviour and stability of metal-GaAs contacts has proven quite elusive. Perhaps this is due to complex interactions between the constituents of metal-semiconductor system and concomitant loss of volatile component of the semiconductor when the system is heat treated for contact formation.

In the present work an attempt has been made to provide a systematic understanding of metal-GaAs system. The study deals with the
physics of ohmic interfaces and characterization of metallizations to design a thermally reliable system for ohmic contacts to GaAs. The work concentrates on contact to n-type GaAs since this is of primary interest to current devices and circuits. However, the analysis can as well be applied to metal-p GaAs ohmic contacts.

The ensuing sections review the physics and technology of ohmic contact to GaAs. The published ohmic models are subsequently discussed to reveal their limitations. The objective and plan of the work is outlined in the final section of the chapter.

1.2 THEORETICAL BASIS OF OHMIC CONTACTS

The fundamental theory of metal-semiconductor (M-S) interface is well established and documented in the literature (1-6). This section is concerned with the formation of a M-S barrier and mechanisms of current conduction across it. The dependence of the barrier resistance on mode of current transport is discussed to describe the structure of an ohmic contact.

1.2.1 FORMATION OF METAL-SEMICONDUCTOR BARRIER

When a metal is placed in an intimate contact with a semiconductor, the valence and conduction bands of the semiconductor bend to align its Fermi level ($E_{FS}$) with that of the metal ($E_{FM}$) at thermal equilibrium, as shown in Fig. 1.1. The resultant potential barrier height $\phi_B$ for electrons flow from the metal to the semiconductor of this simple Schottky model (1-6) is given by

$$\phi_B = \phi_m - X$$  \hspace{1cm} (1.1)

Where $\phi_m$ and $\phi_s$ are work function (the energy from the Fermi level to the vacuum level) of metal and semiconductor respectively & $X$ is the semiconductor electron affinity i.e. the energy from the bottom of the conduction band $E_C$ to the vacuum level.
FIG. 1.1 METAL-SEMICONDUCTOR CONTACTS FORMATION ACCORDING TO THE SIMPLE SCHOTTKY MODEL (a) INFINITE SEPARATION BETWEEN THE METAL AND THE SEMICONDUCTOR AND (b) INTIMATE CONTACT.
For a flow of electrons from the semiconductor into the metal, the potential energy barrier is given by

\[ qV_{bi} = \Phi_B - (E_C - E_{FS}) \]  

(1.2)
as can be deduced from band diagram of depletion contact in the Fig. 1.1. The quantity \( V_{bi} \) is known as the built-in or diffusion potential of the metal-semiconductor (M-S) junction.

This simple metal-semiconductor contact model predicts that the appropriate choice of the metal work function results in depletion, neutral or accumulation contacts as illustrated in the Fig. 1.1. While a good rectifier requires a high barrier height, an ohmic contact prefers as small a barrier height as possible, as indicated by the accumulation contact. This allows a free flow of carriers from the semiconductor to the metal or vice versa.

The eqn. (1.1) of the ideal M-S Schottky contact suggests that \( \Phi_B \) varies directly with \( \Phi_m \) and one should be able to obtain a M-S barrier of desired height. However, it has been experimentally observed (7) that the barrier height is relatively independent of the metal work function as seen in Fig. 1.2, for GaAs. This independence is attributed to the interface states originating from surface states (due to dangling or unsatisfied bonds at the surface) (8,9), from metal-induced gap states (10,11), or from chemical reaction between constituents of the metal and semiconductor at the interface (12-14).

If the density of these states is sufficiently large, then upon contact with a metal, the necessary charge transfer will occur only to or from the surface states and thus the interior of the semiconductor remains screened from the metal. Consequently, the position of the Fermi level is fixed at some level inside the forbidden gap of the semiconductor, known as pinning of the Fermi level by the surface states (8). The barrier
FIG. 1.2 MEASURED BARRIER HEIGHTS AS A FUNCTION OF METAL WORK FUNCTION FOR (a) METAL-n GaAs AND (b) METAL-p GaAs (Ref. 7)
height is then given by an expression (6)

$$\phi_B = E_g - E_{FS}$$  \hspace{1cm} (1.3)

Where $E_g$ is energy band gap of the semiconductor. An approximate thumb rule (15,16) is that the barrier height is roughly two third of the band gap for n-type and one third of the gap for p-type materials. Therefore, metals on a semiconductor having high density of surface states, like GaAs, result frequently in depletion type of contacts.

This implies that the attainment of an 'accumulation' barrier (desired for ohmic contacts) is virtually impossible, especially for large band gap & n-type semiconductors, by choice of a metal. Hence, in order to obtain an ohmic conduction i.e. the free flow of carriers across a M-S interface, some alternative means must be implemented. Obviously, there are two ways to accomplish it : (1) by lowering the barrier height using some exotic techniques, so that the carriers can flow over it easily or (2) by diminishing barrier width, so the electrons can tunnel through it unimpeded.

A method to reduce the barrier height is, by introduction of impurities on the semiconductor surface to introduce interface states for Fermi level pinning. Massie et al. (16) could lower Al-GaAs barrier height from 0.8 eV to 0.4 eV by saturating GaAs surface with $H_2S$. The main difficulty with this process is the required perfect control of the semiconductor surface which may not always be reproducible.

Recent hetero-epitaxy is an attractive technique (3,17) to fabricate junctions with low barrier heights. The concept here is to grow, epitaxially, a thin layer of another semiconductor on GaAs and deposit a metal film onto it. The barrier height can be reduced to a negligible value by choosing an appropriate semiconductor material for epitaxial
deposition, such as InAs (18). Although the hetero-ohmic junctions have been demonstrated to yield extremely low resistance contacts (18-21) nevertheless the method suffers from misfit dislocations problem (22) in addition to the requirement of complex epitaxial process which may not be readily acceptable to an integrated circuit technology.

It therefore, appears that the barrier height engineering is not a realistic way of making ohmic contacts. Using conventional metals and introducing damaged surfaces (23) to create high densities of generation recombination (G-R) centers at the interface is also not a promising technique because such damage generated G-R centers can penetrate deep into the semiconductor and may cause reliability problems (24), especially in thin active layers. This leaves as the only practical technique one in which the metal is deposited onto a highly doped semiconductor (25). Although the barrier height can be significant, the narrow depletion width associated with a heavily doped semiconductor allows tunneling of the carriers (26-29) through the M-S interface.

1.2.2. CURRENT TRANSPORT MECHANISMS

The conduction mechanism (5,26,27) for a metal-n semiconductor contact with increasing doping concentration is shown in Fig. 1.3. For a lightly doped substrate \( N_B < 10^{17} \text{ cm}^{-3} \), the current is the result of electron transfer over the top of the barrier as indicated in Fig. 1.3a. Only those electrons which have thermal energy exceeding barrier height \( \Phi_B \) contribute to the current and is given by well known thermionic emission (T.E) theory. This interface represents a Schottky or rectifying contact.

In the intermediate range of dopings \( 10^{17} < N_B < 10^{19} \text{ cm}^{-3} \), the width of the barrier near its top is sufficiently thin for tunneling
FIG. 1.3 BARRIER HEIGHT & WIDTH & CONDUCTION MECHANISM
FOR METAL- n-SEMICONDUCTOR CONTACTS WITH INCREASING DOPING CONCENTRATION.
to occur there (Fig. 1.3b). The electrons which have enough thermal energy to reach the upper narrower portion of the barrier, tunnel through it to give thermally assisted tunneling, often referred to as the thermionic field emission (T.F.E).

For very high dopings \( N_B > 10^{19} \ \text{cm}^{-3} \) the barrier is thin enough at or near the bottom of the conduction band, so that the quantum mechanical tunneling or field emission (F.E.) is the dominant mode of carrier transport through the barrier as depicted in Fig. 1.3c. For brevity, all the three types of conduction mechanisms are summarised in Fig. 1.3d.

As discussed earlier, most of the metal semiconductor combinations form depletion layer contacts, the conduction properties of which are determined by any one of the three processes described above. The prevalence of a particular mechanism depends primarily on temperature, barrier height, carrier effective mass, semiconductor doping and dielectric constant. Besides, several other factors like the presence of interfacial layers, the stoichiometry of the semiconductor surface or the damages at the interface also influence the carrier transport (1,2,13,14,25).

Assuming uniform doping \( N_B \) in the semiconductor bulk, complete depletion of the space charge region and ignoring image force lowering, Padovani and Stratton (26) derived current-voltage (J-V) characteristics for a metal semiconductor depletion contact. Their analytical expression for the three conduction mechanisms can be summarized as follows:

(i) At a very high doping, electrons are field emitted directly from the Fermi level \( E_{FS} \) in semiconductor to the metal and the resulting current density \( J \) is given by

\[
J = J_{OF} \exp \left( \frac{q V}{kT} \right) \quad (1.4)
\]
Where

\[ J_{OF} = \frac{\Pi A^* T}{KC_1 \sin(\Pi KT C_1)} \exp(-\phi_B / E_{oo}) \] (1.5)

\[ C_1 = \frac{1}{2E_{oo}} \ln \left[ -\frac{4(\phi_B - qV)}{\xi} \right] \] (1.6)

\[ \xi = E_C - E_{FS} \] (1.7)

\[ A^* = \frac{4\Pi qm* K^2}{h^3} \] (1.8)

\[ E_{oo} = \frac{h q}{4 \Pi} \left( \frac{N_B}{m* E_s} \right)^{1/2} \] (1.9)

The parameter \( A^* \) is called Richardson's constant. \( K \) is the Boltzmann's constant, \( h \) is the Planck's constant, \( q \) is electronic charge, \( T \) is temperature in \( ^\circ K \), \( E_s \) is semiconductor dielectric constant, \( N_B \) is the carrier concentration in the semiconductor bulk and \( V \) is the bias applied across the M-S junction. The parameter \( E_{oo} \) has dimensions of energy and is very useful in determining the range of doping and temperature for which a particular conduction mechanism is valid. For example, for field emission to dominate, \( E_{oo} \gg KT \), i.e., it is applicable at high dopings or low temperatures. Note that the J-V characteristics of eqn. (1.4) shows only a weak temperature dependence through \( J_{OF} \).

(ii) For moderate doping levels, where \( E_{oo} \approx KT \), electrons travel at an energy \( E_m \) above the conduction band edge in the semiconductor bulk and

\[ J = J_{OF} \exp(qV/E_0) \] (1.10)
Where

\[ J_{OTF} = \frac{A T \sqrt{\frac{\pi}{\hbar^2}} E_0 (e_B - qV - \xi)}{K \cosh (E_0 / KT)} \exp \left[ -\frac{\xi}{KT} - \frac{1}{E_0} (e_B - \xi) \right] \]  

\[ E_o = E_0 \coth (E_0 / KT) \]

For TFE of eqn. (1.10), Padovani and Stratton (26) found the energy at which tunneling occurred to be

\[ E_m = \frac{(e_B - qV - \xi)}{\cosh^2 (E_0 / KT)} \]  

(iii) At low dopings, where \( E_0 \ll KT \), the carriers are thermionically emitted over the barrier and the resulting current is given by

\[ J = J_{OT} \exp (qV / nKT) \]  

where

\[ J_{OT} = A^* T^2 \exp (-e_B / KT) \]

\[ n = (1 - \beta)^{-1} \]

\[ \beta = \frac{\partial \Phi_B}{\partial V} > 0 \]

The parameter \( n \) is called the ideality factor. If \( n = 1.0 \), the \( J-V \) characteristics illustrates behaviour of an ideal Schottky diode. The value of \( n \) increases rapidly with doping, as tunneling (TFE & FE) component takes over the thermionic emission (1,4,5).

For thermionic-emission, it is normally assumed that the barrier height \( e_B \) is independent of the applied bias. However, in presence of an interfacial layer and image force lowering, it becomes a function of field or the bias across the interface and can be approximated as
where $\Phi_{BO}$ is the barrier at zero applied voltage.

From eqn. (1.9) it can be easily inferred that for n-type GaAs, at room temperature, the cross-over from thermionic-emission to thermionic field emission occurs at the relatively low doping of about $10^{17}$ - $10^{18}$ cm$^{-3}$. This is primarily because of the low value of the electron effective mass in GaAs.

In the above discussions, image force lowering, which reduces the intrinsic M-S barrier height (1,4) has not been considered. Calculations (7) suggest that the lowering is not substantial until substrate doping exceeds $10^{19}$ cm$^{-3}$, a value at which tunneling also begins to be effective.

1.2.3 CONTACT RESISTIVITY

The electrical properties of ohmic interfaces are most often characterised by a single parameter called specific contact resistivity $P_c$ (ohm.cm$^2$) defined as

$$P_c = (\partial J/\partial V)^{-1}_{V=0}$$

Applying this definition to the above three cases Yu (28) obtained the following analytical expressions for specific contact resistivity. For field emission with $E_0 \gg KT$,

$$P_c = \left\{ \frac{A^* T \pi q}{K \sin(\pi C_1 KT)} \exp(-\Phi_B/E_0) - \frac{A^* q}{C_1 k^2} \cdot \exp\left[-(\Phi_B/E_0) + C_1 \xi \right] \right\}^{-1}$$
For thermionic-field emission with $E_{oo} \sim KT$,

$$P_c = \frac{K^2 \text{Cosh} (E_{oo}/KT)}{q A^* [\Pi(\Phi_B - \xi) E_{oo}]^{1/2}} \cdot \left[ \text{Coth} \left( \frac{E_{oo}}{KT} \right) \right]^{1/2} \cdot \exp \left\{ \left[ \frac{(\Phi_B - \xi)/E_0}{(\Phi_B/\xi) + (\xi/KT)} \right] \right\} \quad (1.21)$$

and for thermionic emission, with $E_{oo} \ll KT$

$$P_c = \frac{K}{q A^*} \exp \left( \frac{\Phi_B}{KT} \right) \quad (1.22)$$

It is obvious from eqns. (1.20)-(1.22) that the combination of three parameters viz. the barrier height, the temperature and the dopant concentration determine the value of $P_c$ in a given metal-semiconductor system. The relative effect of these parameters in various current transport regimes could be inferred from the exponential terms in these eqns. After substituting the value of $E_{oo}$ from eqn. (1.9) in eqs. (1.20)-(1.22) we obtain

$$P_c \propto \exp \left[ \frac{4\pi \sqrt{(m^*Es)}}{qh} \left( \frac{\Phi_B}{\sqrt{N_B}} \right) \right] \quad (1.23)$$

for the field emission process,

$$P_c \propto \exp \left\{ \frac{4\pi \sqrt{(m^*Es)}}{qh} \left( \frac{\Phi_B}{\sqrt{N_B}} \right) \cdot \text{tanh} \left[ \frac{h \sqrt{N_B}}{4\pi K T \sqrt{m^*Es}} \right] \right\} \quad (1.24)$$
for the thermionic field emission and
\[ P_c \propto \exp(\Phi_B/KT) \]  \hspace{1cm} (1.25)

for the thermionic process. This functional dependence of specific contact resistivity on semiconductor doping and barrier height is depicted in Fig. 1.4. It predicts that in the FE range, \( P_c \) is proportional to \( \exp(1/\sqrt{N_B}) \) and is insensitive to the temperature. For the case involving thermionic field emission, \( \ln P_c \) varies non-linearly with \( N_B^{-1/2} \). It has temperature dependence in this regime as indicated in the eqn. (1.24). In the thermionic emission range eqn. (1.25) exhibits strong dependence of \( P_c \) on barrier height and temperature whereas semiconductor doping has no influence on it.

The current eqns. (1.4), (1.10) and (1.14) denote that all metal-semiconductor contacts have a non-linear \( J-V \) characteristic of the form
\[ J = J_o \left[ \exp \left( \frac{V}{V_o} \right) - 1 \right] \]  \hspace{1cm} (1.26)

where \( J_o \) & \( V_o \) depend on the mechanism of current flow. At small applied voltages (ie. \( V \ll V_o \)) we have
\[ J = J_o \left( \frac{V}{V_o} \right) \]  \hspace{1cm} (1.27)

This suggests that a contact can exhibit a linear \( J-V \) characteristics i.e it is ohmic, if dependence of \( J_o \) on \( V \) is ignored. Therefore, for a practical ohmic contact, \( J_o \) must be large enough so that the resistance of the contact is small, ensuring \( V \ll V_o \) under all operating conditions. From eqns. (1.5), (1.11) & (1.15) it can be shown that the largest value of \( J_o \) occurs in the case of field emission.

1.2.4 METAL-SEMICONDUCTOR OHMIC STRUCTURE

Following the theory of current transport, it can be concluded that to obtain an ohmic interface, a metal is required to be contacted on a highly doped semiconductor. The principal strategy therefore,
FIG. 1.4 THEORETICAL DEPENDENCE OF THE SPECIFIC CONTACT RESISTIVITY ON THE SEMICONDUCTOR DOPING CONCENTRATION. (REF. 28)

\[
\frac{KT}{qA} \exp\left( \frac{\phi_B}{KT} \right)
\]

In \( P_c \)

\[ \frac{1}{\sqrt{NB}} \]

Slope = \[ \frac{2 \sqrt{m^*E_s}}{q \hbar} \phi_B \]
employed, to fabricate an ohmic contact is to dope the surface of the semiconductor sufficiently high to ensure that the dominant conduction mechanism is field emission.

In fact the presence of a highly doped layer between the metallization and the semiconductor bulk, as shown in Fig. 1.5a, seems to be a necessary condition for achieving the best quality ohmic contacts (30, 31). However, the thickness of this intermediate layer has an important implication on electrical properties of the junction. If it is smaller than the metal-semiconductor \((n^+\) depletion width \(w\), the depletion layer edge penetrates into the n-substrate and the contact becomes non-ohmic or injecting (32, 33). The thermionic field emission is the mode of current transport in such a metal-\(n^+\) (thin)-n structure (34), and a barrier of desired height can be obtained by adjusting carrier concentration in the intermediate \(n^+\)-region (32-34).

When the thickness \((t)\) of the intermediate layer is large enough to accommodate M-S depletion barrier well within it, as indicated in conduction band diagram of Fig. 1.5b, the field emission is the dominant mechanism of carrier flow through the interface. Consequently a metal-\(n^+\) (thick)-n structure exhibits ohmic characteristics (34).

1.3 OHMIC CONTACT FABRICATION TECHNOLOGY

In order to realize a metal-\(n^+\) (thick)-n ohmic structure, a number of techniques have evolved over the years (2, 35-38). Much of the impetus for renewed research on contact technology in the last ten years resulted from the application of advanced vacuum preparation and beam processing technique (38-40).

The formation of intermediate impurity enriched region and the enhancement of the carrier concentration in it, form the basis for ohmic
FIG. 1.5  (a) METAL $n^+$ - $n$ GaAs OHMIC STRUCTURE

(b) CONDUCTION BAND DIAGRAM OF M-S OHMIC STRUCTURE
contact technology since higher the doping thinner the barrier which permits excessive tunneling to yield low resistance contacts. The techniques which are used for fabricating ohmic contacts to n-GaAs are described to elucidate their merits & drawbacks.

1.3.1. SINTERING

It is one of the conventional methods of making ohmic contacts to semiconductor. The basic approach in this technique is to deposit a multi-component metallization which incorporates a dopant element (e.g. Ge, Si, Se, S, Sn or Te for n-GaAs and Zn, Cd, Mg & Be for p-GaAs) onto GaAs substrates (6,35,41). The structure is then heated in vacuum or an inert ambient at a temperature below the melting point of the contacting metallization. This sintering temperature, thus depends on reaction temperature between constituents of metals & GaAs and eutectic temperature of the systems (35-38, 42-44).

Ohmic behaviour of sintered contacts is attributed to a combination of doping effect and chemical reactions at the interface (42-45). The diffusion of the dopant element, generates a heavily doped layer in the semiconductor surface just beneath the metallization whereas the thermally induced metal-GaAs interactions produce intermetallic compounds of low barrier height (38, 43). Thus a tunneling junction with reduced barrier height is obtained. Since no melting occurs in this process, the formation of ohmic contact relies on solid phase reaction (16, 36, 44).

Pd/Ge (42, 45), Ni/Ge (46) and AuGe (47-52) have been investigated as metallizations for sintered contacts to GaAs. Even though a good interface uniformity and an excellent surface morphology are the features of these contacts (5, 35-38) the achieved resistance values are rather high 10⁻⁴ ohm-cm². Owing to this, sintering is not a popular
method of making contacts in GaAs but it has become a well established
technique for silicide contacts (6, 38) in silicon technology.

1.3.2. ALLOYING

Alloying is an extensively used conventional technique for form­
ing ohmic contacts (5, 35-38, 43, 53). To fabricate alloyed contacts,
usually a metal-semiconductor system is subjected to a brief heat treat­
ment at a temperature above the melting point of the metal film in
a furnace in flowing gas of H₂ or N₂. The metallization involves
an eutectic metal composition with a suitable dopant element. The contact
resistance is found to depend upon alloying time and temperature and
also upon the heating and cooling rates. In general, the optimum alloy
time and temperature must be determined experimentally for each alloy­
ing system used. Too long an alloy time or too high a temperature
result in a degraded ohmic contact (54, 55).

There are two main schools of thought concerning formation
of the heavily doped intermediate region in case of alloyed ohmic conta­
cts. One suggests that it forms during alloying due to diffusion of the
dopant into the semiconductor (4,6,35-38). The other holds that this
degenerate layer regrows from the molten melt (31, 36-38). It is believed
that during the heating part of the alloying cycle one or several contact
components are molten and some of the semiconductor is dissolved in
the melt. On cooling the dopant segregates from the melt together
with the solidifying semiconductor. Thus the regrown layer constitutes
the heavily doped intermediate region of the alloyed metal-n⁺-n ohmic
structure.

Gold and silver based metallization systems have frequently been
used for ohmic contacts to GaAs (2, 35-38, 43, 44). Gold alloys are
generally preferred because of their low eutectic temperatures (44).
Among the various systems exploited for ohmic contacts to n-GaAs, the alloyed Au:Ge is found most suitable (35,38, 43-45, 53-56) and presently satisfies a wide spectrum of commercial applications. The recent review articles (35-38) evince that the resistance values of the furnace alloyed contacts to n-GaAs are about $10^{-5}$ ohm-cm$^2$ and thus are lower by an order of magnitude compared to that of sintered contacts. However alloying inherits a few technological problems which are important, particularly from reliability view points. Some prominent consequences of a metal alloying to GaAs are:

(i) Poor surface morphology.
(ii) Non-planar interface.
(iii) Dissociation of the semiconductor and
(iv) In-diffusion of elements of metallization.

Despite these issues, alloying is usually used in production of various GaAs devices. It is mainly because of the ease of contact fabrication and compatibility of the technique to the device processings, in addition to the acceptable resistance values of the resultant contacts. Therefore, research efforts are continued to-date to devise some means to abate the magnitude of these problems. The probable aspects of the origin of these problems and some of the ancillary techniques which are incorporated in alloying to control them are discussed in the following paragraphs.

The poor alloyed surface is attributed to the high surface tension in a liquid metal film, which causes the metal to ball up (56). The formation of intermetallics are the sources of excessive strain at the contact region and thus leads to uneven interface (44, 58). The inclusion of wetting agents like Pt or Ni in the metallization (46, 53,59) or covering the metal layer with a dielectric film prior to the heat treatment (61,62) has been found to considerably improve the surface morphology.
Dissociation of semiconductor is the most deleterious effect associated with the alloying technique. It is ascribed to loss of arsenic from the metallized semiconductor surface (62, 63) during heating. To prevent it, Hartnagel and co-workers have used a sealed ampoule to obtain arsenic over pressure during the alloying cycle (64). An encapsulant layer of silicon dioxide has also been found to suppress the arsenic evolution (60).

The deep penetration of constituents of the metallization makes alloyed contacts unsuitable for shallow junctions and large scale integrated circuit (6, 65). The incorporation of a diffusion barrier layer in the metallization scheme is a recent technique to preclude the unwanted interdiffusion (66-68). However, the barrier layer is required to be properly designed for each metal-semiconductor system.

The undesirable features of furnace alloying can be diminished to a great extent by application of laser or pulse electron beams (39, 40, 69, 70). The metallized surface of the semiconductor is heated quickly (< 1/μs) to a high temperature in a beam annealing technique. The reduction in heating time minimises (i) loss of the volatile component (ii) intermixing of the elements of metal & semiconductor and (iii) phase segregation and size of grains. Low resistance contacts (~ 10^{-6} ohm-cm^2) with excellent surface and a small redistribution of contact constituents have been fabricated by these transient techniques (69 - 74).

The use of alloying in which a high frequency spark is employed to heat the surface, has also been demonstrated to give results compa-
rable to that obtained with pulsed beam processing (75).

In conclusion, to obtain reliable low resistance alloyed contacts, some technological artifices are required to be allied to the alloying technique to minimise the problems involved in it.

1.3.3 DIFFUSION, ION-IMPLANTATION & EPITAXY

Diffusion, implantation and epitaxy may be used to form the heavily doped intermediate region of an ohmic structure prior to metal deposition. The alloying is discretionary to accomplish the contact formation.

Diffusion is the most classical way to obtain a highly doped surface layer. Since contact resistance is merely a function of the dopant concentration in the intermediate region, it is limited by solid solubility of the impurity in this case (76). To enhance the doping, laser or pulsed electron beams have been used to assist the thermal diffusion (40, 76-78). The high diffusion temperatures and large diffusion depths are the two specific problems encountered in contact formation in this method which may be incompatible with the layered structures or shallow junctions.

To obtain carrier concentration in excess to the solid solubility limit, a high dose or multiple implantation is used (38, 80-84). However, the annealing of the implanted layer is essential to restore the crystallinity and activate the implant. The electrical activation is the limiting factor for doping by implantation. Recent laser (85-90) &
electron beam (91, 92) annealing gave better results than conventional furnace annealing (93). A further improvement in contact resistance has been observed when implanted surface is coated with a capping layer prior to activation (83, 95-98).

One of the major drawbacks of pulse annealing is introduction of crystallographic & electrically active defects (39, 40, 69, 99, 100), which lead to low mobilities in the layer and subsequent contact degradation during device operation at elevated temperatures. Nevertheless, the implantation followed by transient annealing is regarded as very advantageous in comparison to the conventional techniques (39, 40, 69).

The application of epitaxy is yet another approach to grow a heavily doped layer on semiconductor surfaces. The carrier concentration in the layer grown by liquid phase epitaxy (LPE) or vapor phase epitaxy (VPE) are determined by the solid solubility and thermodynamic considerations during the growth (17). In molecular beam epitaxy (MBE) the surface kinetics governs the dopant incorporation in the deposited film (101). Using these techniques, low resistance ohmic contacts to GaAs have been realized (102-109). The MBE contacts are generally not alloyed and thus the contact surface is smooth & featureless. However, one of the most serious problems of non-alloyed contacts is thermal instability (69, 110). The process complexity and limited throughput restrict the wide applications of the epitaxial techniques for contact fabrications.

1.3.4 ION-BEAM MIXING

Ion-beam mixing has been used to induce silicide reactions in silicon technology (37). Recently, it has been demonstrated as a viable technique to fabricate ohmic contacts to GaAs (111-113). In this technique, the metallized GaAs substrates are irradiated with energetic ions
(Ge⁺, Si⁺ or Ar⁺) and then the samples are heated at a low temperature to obtain a desired doping and alloy composition at the interface by mixing of ions. The ion-beam mixed metallization has shown a remarkable improvement in surface morphology (111) in comparison to alloyed contacts. However, the technique is yet to be fully explored in terms of resistance and performance of the contacts.

1.3.5 HETRO-EPITAXY

Hetro-epitaxy is based on the principle of reduction of barrier height to obtain ohmic conduction across a metal-semiconductor interface unlike the above techniques which generate tunneling junctions. A thin layer of dissimilar semiconductor with a characteristically low barrier height is introduced between the semiconductor substrate and the metal film. The material of the sandwiched semiconductor is chosen with lattice constants nearly equal to that of the host semiconductor and is epitaxially deposited to form an abrupt hetro-interface as shown in (Fig. 1.6a). The epitaxial layer may also be doped heavily to further reduce the contact resistance.

In order to overcome the conduction band discontinuity at the abrupt interface and to improve the lattice matching, the hetro-epitaxial layer is graded as shown in Fig. 1.6b. Low resistance (∼10⁻⁷ ohm-cm⁻²) hetro-junction contacts using MBE grown Ge (22) and InAs (18) films on n-GaAs have been reported. However, in addition to misfit dislocations, the usual problems which are associated with implanted and epitaxial techniques are also encountered in fabrication of hetro-epitaxial contacts.

In summary, on the basis of fabrication methodology, ohmic contacts can broadly be classified in two categories: Alloyed and Non-alloyed contacts. In alloyed contacts, an impurity enriched layer is generated
FIG. 1.6 BAND DIAGRAM FOR InAs-GaAs HETEROJUNCTION
OHMIC CONTACT
(a) InAs-GaAs ABRUPT INTERFACE AND
(b) InAs-GaxIn1-xAs-GaAs GRADED INTERFACE
(Ref.18)
in the semiconductor surface by heating a metal-semiconductor system whereas it is formed by some external means such as implantation or epitaxy in case of non-alloyed contacts.

1.4 EXPERIMENTAL RESULTS AND THEORETICAL MODELS OF OHMIC CONTACT TO GaAs

In this section, the results exhibited by metal- n GaAs ohmic contacts and the theoretical models which have been proposed in the literature are discussed to enumerate the discrepancies observed between the experimental results and the theoretical predictions.

1.4.1 EXPERIMENTAL RESULTS

The recent review studies (5, 35-38) evince that for alloyed contacts to n-GaAs, the contact resistivity lies in the range of $10^{-4}$ to $10^{-6}$ ohm-cm$^{-2}$ and it ameliorates to $10^{-7}$ ohm-cm$^{-2}$ when non-alloying techniques are used. Although with the application of beam processing techniques, it has become feasible to dope heavily the semiconductor surface (105) nevertheless the contact resistance below $10^{-7}$ ohm-cm$^{-2}$ has not yet been achieved in case of metal- n GaAs ohmic contacts (5, 35-38). The major features of ohmic behaviour of the system can qualitatively be described as follows.

A typical alloying characteristics of a metal-GaAs system is represented in Fig. 1.7a. It shows a minimum in the resistance value (Pc.min.) at an optimum alloying temperature, beyond which it rises again. This trend is observed in almost all the cases when a metallization containing a dopant element is alloyed to GaAs and other semiconductors (30, 41, 44, 54, 114-116). The published measured values of Pc.min. is limited to about $10^{-6}$ ohm-cm$^{-2}$ for metal- n GaAs alloyed contacts as documented in the recent review articles (5, 35-38).
FIG. 1.7 (a) A TYPICAL ALLOYING BEHAVIOUR OF A METAL SEMICONDUCTOR SYSTEM
(b) EXPERIMENTAL DEPENDENCE OF CONTACT RESISTIVITY ON n-GaAs DOPING. (REF.58)
Another important feature of the experimental results of the system has been recognised by Braslau (58). To study the dependence of \( P_c \) values on the bulk concentration \( N_B \), Braslau summarized the published measured values of the contact resistance and obtain the behaviour as shown in Fig. 1.7b. It apparently predicts an inverse proportionality between \( P_c \) & \( N_B \) despite a relatively large spread in the experimental data of \( P_c \).

### 1.4.2. OHMIC MODELS

A number of theoretical ohmic models have been hypothesized to interpret the mentioned features. These are briefly reviewed to examine their appropriateness of application to the ohmic structures obtained in practice.

Braslau (58) proposed an ohmic model to explain \( 1/N_B \) dependence of \( P_c \). He assumed that in a non-planar interface of Au:Ge:Ni-n GaAs alloyed system, the most of the current flows through the Ge-rich protrusions of radius 'r', which are connected through the overlying metal, as shown in Fig. 1.8a. In the intermediate Ge-poor regions, the conduction is much less due to the exponential dependence of tunneling on underlying doping. Thus the current is non-uniformly distributed across the contacting surface. His empirical equation that relates the measured specific contact resistivity \( P_c \) (meas.) to its theoretical counterpart \( P_c \) is expressed as

\[
P_c (\text{meas.}) \sim < R >^2 \left[ \frac{P}{\pi < r >} + \frac{P_c}{2\pi f < r >^2} \right] - - - - (1.28)
\]

Where \(< >\) indicates mean values, \( P \) is the resistivity of the semiconductor bulk and \( f \) is a factor to account for field enhancement of the current at the penetrating points (\( f > 1 \)). For \( P > 10^{-3} \) ohm-cm
FIG. 1.8 (a) BRASLAU'S OHMIC MODEL (REF. 58)
(b) SEBESTYEN'S OHMIC MODEL (REF. 117)
(ie \(N_B < 4 \times 10^{18} \text{ cm}^{-3}\)) the contribution of the second term i.e the resistance of the conducting protrusions is negligible compared to the first term which corresponds to the substrate spreading resistance. Consequently, the eqn. (1.28) gives

\[
P_c(\text{meas.}) \propto P
\]

or

\[
P_c(\text{meas.}) \propto \frac{1}{qN_B\mu_n}
\]

where \(\mu_n\) is the electron mobility. Thus the model clearly, describes the inverse dependence of \(P_c\) on \(N_B\).

However, the Braslaus’ model lacks generality as it is not applicable to non-alloyed or beam annealed contacts which are believed to possess planar interfaces.

Sebestyen (23, 117) postulated the formation of an amorphous or disordered layer in the semiconductor surface just beneath the contact metal due to the alloying process. The energy band diagrams of the resulted, abrupt or graded layer junctions are indicated in Fig. 1.8b. In these structures, the conduction is assumed to occur either by electrons hopping between the mobility gap states near the Fermi-level or it can be thought of as multi-step tunneling and trap assisted recombination through the trap states.

Since in this disordered structure, the estimation of number of tunneling steps (18) is incompatible to the thickness of the inter-mediated region(1.17) it is difficult to characterize the relevant properties of such a sandwich structure to define the experimental observations.

Heiblum et al. (119) have hypothesized the generation of thin high resistance layer (HRL) under the \(n^+\)-region of an alloyed Au:Ge:Ni-
n GaAs contact as depicted in Fig. 1.9a. Although the origin of the HRL is unclear, its formation may probably be attributed to thermally induced interactions at the interface or out diffusion of chromium from the substrate or anomalous doping effects of the metal elements.

Perhaps it may be possible to describe the high temperature alloying behaviour by this model but it is difficult to deduce quantitative results as the mechanism of formation of HRL is not known.

Popovics' model (120) appears to be the most plausible one to explain $N_B^{-1}$ dependence. It assumes that the thickness of the undepleted part of $n^+$ region is smaller than the carrier mean free path. Consequently, the hot electrons, tunneling through the metal-semiconductor barrier are transported without collision (i.e. ballistically) across the $n^+$ region if they possess energy larger than the $n^+$-$n$ barrier height. Therefore, the current across the contact is controlled not by the tunneling M-S barrier but by the potential energy barrier at $n^+$-$n$ junction. On the basis of these considerations and assuming a very high doping in the $n^+$ region Popovic obtained an expression for contact resistivity as

$$P_c \approx \frac{K \exp \left( \frac{\phi_B - \Delta \phi}{E_t} \right)}{T q n_m A^*} \frac{N_c}{N_B}$$

where

$$E_t \approx \frac{E_{oo}}{\Pi} \left( \frac{8 q V_{bi}}{\Delta \phi} \right)^{1/2}$$

$$\frac{E_b}{\Delta \phi} \approx \left[ \Pi \left( \frac{q V_{bi}}{E_{11}} \right)^{3/2} \right]^{1/2}$$

$$E_{11} = \frac{q^2}{2} \left( \frac{N_B}{E_s E_d^2} \right)^{1/3}$$
FIG.19 (a) HEIBLUM'S et al. MODEL. (REF.119)
(b) METAL-n GaAs CONTACT. THEORETICAL LINES FROM DINGFEN et al. MODEL (REF.121).
POINTS SHOW PUBLISHED MEASURE Pc VALUES (REF.35-38)
The parameter $\Delta \phi$ is called image force barrier lowering. $E_s$ & $E_d$ are respectively the static & dynamic dielectric constants of the semiconductor, $n_m$ is the equivalent minima number of the conduction band, $N_c$ is the effective density of states in the conduction band. $E_{oo}$ and other parameters are defined in the section 1.2.2. The expression (1.30) clearly shows the inverse relationship between $P_c$ & $N_B$.

The Popovics' model is valid only for the alloyed contacts as the thickness of the $n^+$ layer, resulting due to alloying is generally less than the electron mean free path. However, in case of low resistance contacts formed by implantation or epitaxy, relatively thick layers are involved and therefore the model is not applicable.

Recently, Dingfen & Heime (121) proposed a model based on high-low barrier theory to explain the reciprocal relation of ohmic contacts to $n$-GaAs. They considered the diffusion theory to evaluate the high-low barrier resistance and emphasized that the contact resistance is predominantly determined by it for a degenerate doping in the intermediate $n^+$ region. The resistivity expression of the high-low barrier they deduce is

$$P_{hl} = \frac{L_n}{q \mu_n} \frac{N_c}{N_D N_B}$$

Where $L_n$ is the diffusion length of electrons in $n$-GaAs, $N_D$ is the impurity concentration in $n^+$ region. Thus the model expresses the desired dependence of contact resistance on $N_B$ for negligible contribution of the tunneling (metal - $n^+$) barrier which is in series with the high-low junction in an ohmic structure.

A comparison of the results predicted by eqn. (1.34) and the published measured values of $P_c$ is illustrated in Fig. 1.9b. It is seen
from the figure that a number of experimental values of $P_c$ lies even below the theoretical line corresponding to $N_D = 10^{20}$ cm$^{-3}$ (a doping level which has not been so far possible to achieve in practice in GaAs). This contradicts their own conclusion that the contact resistance is sum of the tunnel and high-low barrier resistance. Therefore, the theory envisaged by Dingfen et al. need to be reconsidered to interpret the resistance of a metal-semiconductor ohmic structure.

Therefore, it can be concluded that none of the published models satisfactorily describes the ohmic properties of metal-GaAs contacts. A comprehensive survey of the literature on ohmic contact to GaAs reveals following discrepancies between the experimental results and the theoretical predictions which require explanations.

(i) The ohmic behaviour of contacts fabricated by alloying techniques is not well understood, specifically (a) the phenomenon limiting the minimum value of the contact resistivity and (b) the reason of increase in resistance for alloying beyond the optimum temperature.

(ii) The tunneling theory, widely applied to ohmic contacts, predicts $\exp (1/ \sqrt{N_B})$ relationship of contact resistivity $P_c$ on the semiconductor bulk doping $N_B$, whereas the contacts in practice show the inverse dependence of $P_c$ on $N_B$.

(iii) The reported measured values of contact resistance are not as low as predicted by the field emission theory. What limits the resistance values is not known.

(iv) The resistivity of implanted & epitaxial contacts is lower by an order of magnitude compared to alloyed contacts but the stability of these non-alloyed contacts is poor and often the resistance value deteriorates under thermal aging or long term operation.
1.5 OUTLINE OF THE PRESENT WORK

The objective of the present study, is to develop ohmic models which are capable of rationalising the features cited above and provide the necessary foundation for an unified understanding of the previous results. It also aims to investigate metallizations for thermally stable contacts to GaAs.

In brief, the research work deals with (i) physics of ohmic contact and (ii) characterization of metallizations to design a high temperature ohmic contact to GaAs. This is documented in six chapters of the thesis, a concise resume of these is as follows:

CHAPTER – II:

ESCA characterisation of metallization systems comprising of layers of Ge, Ga and Au alloyed to GaAs is reported. From these results, the role of gallium in a metallization scheme is investigated and diffusivity data of gallium diffusion in gold are extracted.

CHAPTER – III:

On the basis of findings of the preceding chapter, a new ohmic model, 'Gallium Vacancy Diffusion Model' is developed to rationalize the ohmic behaviour of alloyed contacts to GaAs. Gallium diffusion constants obtained in the chapter II are used in Whipples' expression of grain boundary diffusion to construct the model. The model predicts the theoretical limitations in obtaining minimum values of resistance in case of contacts formed by alloying techniques.

CHAPTER – IV:

The influence of a high-low barrier, which follows the metal-semiconductor tunneling junction in an ohmic structure, on current
transport is elaborated. Thermionic emission (T.E) is hypothesized as a dominant mode of carrier transfer across a high-low barrier. The barrier resistance based on T.E theory is added to the tunneling junction resistance to interpret the published experimental results. The model rationalizes the reciprocal dependence of contact resistivity on bulk doping and predicts theoretical limitations on contact resistance in metal-semiconductor ohmic systems.

CHAPTER V:

The criteria concerning the stability of a metallization on GaAs are discussed. The thermal stability of vacuum deposited metallic layers on GaAs, incorporating, a thin film of W.Si₂ as a diffusion barrier is studied using ESCA and SEM. The elemental interdiffusion and chemical compositions of alloyed regions are studied to assess the reliability of the system. The characterization demonstrates that Ge-W.Si₂-Au combination constitutes a thermally stable ohmic system to GaAs.

CHAPTER VI:

A design criterion to ameliorate ohmic contacts to n-GaAs has been discussed. Carrier energy loss mechanisms are considered to evaluate the structural parameters of a metal-semiconductor ohmic contact. On the basis of the models proposed in this thesis, some guidelines are presented for optimal design of an ohmic structure. The conclusion, assesses the requirements to obtain low resistance contacts & suggests some possible means to achieve them.
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