CHAPTER - V

DESIGN AND CHARACTERIZATION OF A THERMALLY STABLE METALLIZATION ON GaAs

INTRODUCTION

Major impetus for the development of high temperature electronic materials, devices, circuits and systems may be credited to the application of micro-electronics in various areas such as space exploration, nuclear instrumentation, transportation, communication, defence, oil, gas and geothermal well logging etc (1-3). For these applications solid-state devices are required to function reliably in high temperature (>300°C) environments (1-3).

Since high power and current levels also enhance temperature of the device, thermal stability is one of the key criteria to determine the operating power and current densities which interconnect lines in a VLSIC (Very Large Scale Integrated Circuit) can handle (1,2,4-6). Therefore, there is a growing need for thermally reliable devices/circuits for research and operational applications.

From physics point of view, the deleterious effects of high temperature on material parameters are (1) movement of Fermi level towards the band gap center (2) narrowing of the band gap and (3) decrease in carrier mobility. These in general, cause decrease in the built-in potential & transconductance and increase in the intrinsic carrier concentration & leakage current of a device (7-12). However, in case of wide band semiconductors, these parameters are not significantly influenced and thus satisfy the material requirements of high temperature micro-electronics (1-3, 9,10).
The excellent material properties combined with the recent technological advancements have made GaAs a leading contender among the large gap semiconductors (8, 11-16) for high temperature applications. Consequently, a wide range of discrete devices like Gunn diodes, light emitting diodes (LED), hetero & homo junction injection lasers, Schottky diodes, field effect transistors (FET), sensors, detectors, monolithic microwave integrated circuits (MMICs) and VLSI level integrated circuits are now based on GaAs semiconductor (3,13-19).

However, one of the most difficult problems associated with GaAs devices intended for high temperature operation is the failure of interface integrity between the metal and the semiconductor (5, 20-23). Even in room temperature preparation of the metal-semiconductor junctions, interdiffusion and interfacial reactions occur and these get accentuated at elevated temperatures (5, 23-24). These thermally induced interactions alter the interface metallurgy and morphology (28-34) which profoundly influence the electrical behaviour of the junction. Therefore, the ultimate limit in performance, parametric stability and long term reliability of GaAs devices are determined by the properties of metallization systems used for contacts & interconnects.

Typically, the life time limiting factors of device operating in hot ambients are (i) altered electrical characteristics due to interdiffusion of elements at the interface (23-35) (ii) dimensional changes or embrittlement of contacting lines caused by compound formation or grain growth (5, 23, 25-27, 29-33, 36-40) and (iii) electromigration dependent metallization failures (41-44). All these failure modes involve diffusive transport with in and/or among the semiconductor and metal layers whose influence increases roughly exponentially with increase in temperature (5).
Therefore, for high temperature applications and in modern VLSI technology where self-aligned gate process and multi-level metallization schemes are being increasingly adopted, thermal stability and dimensional confinement of metal contacts are of immense importance. Development of a suitable metallization to meet the high temperature requirements is one of the challenging tasks to the contact technology.

An attempt is made in the present work to design and develop a thermally stable metallization for ohmic contact to n-GaAs. The ensuing sections describe the general requirements of a metallization and stability criteria. Based on these a multilayer scheme consisting of Ge-WSi$_2$-Au is designed as a thermally stable system in section 5.5. The subsequent section 5.6 is devoted to characterize the system using ESCA, SEM & electrical measurements to assess its thermal stability. The results are discussed in section 5.7 which follows conclusions in section 5.8 to summarize the suitability of the newly developed metallization as a reliable ohmic contact to n-GaAs.

5.2 GENERIC REQUIREMENTS OF STABLE METALLIZATION SYSTEMS

In general metallization systems can be classified as 'CONTACTS' and 'INTERCONNECTS'. A contact metallization provides the electrical connection (ohmic or rectifying) to the active regions on a semiconductor chip while interconnects furnish the lateral conducting paths to the circuit elements as well as the link to the external world through the bonding pads. Although the present study concentrates only on ohmic contacts to GaAs nevertheless most of the considerations are general and can be applied to Schottky contacts and interconnects as well.

It is important that a good durable ohmic contact with both the right electrical and physical properties be realized in metallization
layers so that the contact characteristics are stable over time and
temperature. To cover the wide range of applications of GaAs devices,
the generic requirements of an ohmic contact metallization on GaAs
can be summarized as follows:

(i) Low contact resistance.

(ii) Good adherence to the GaAs surface.

(iii) Reasonable matching of thermal expansion coefficients with
GaAs and between the adjacent layers in a multilayered structure.

(iv) Stability against high temperature and prolonged exposure to
atmosphere.

(v) Stability against compound formation, in-diffusion of metal
and out-diffusion of gallium and/or arsenic.

(vi) High conductivity.

(vii) Resistance to electromigration.

(viii) Potential for selective etchability between the metal & GaAs.

(ix) Good resistance to metallurgical reactions, oxidation and corro-
sion.

(x) Compatibility with wire bonding.

Contact resistance is one of the important criteria in design
of an ohmic contact metallization. It represents the resistance asso-
ciated with the metal-to-semiconductor interface. For a planar contact
it is defined as the resistance between the metallization and an imagi-
nary plane at the edge of, and perpendicular to, the metallization
(28, 45, 46). Since the contact resistance appears in series with the
semiconductor substrate, the voltage applied across a M–S ohmic junction
gets shared between the contact and the substrate resistance.

The physics of scaling devices and circuits dictates that while
transistor delay times improve as devices are scaled down, the contact
properties degrade. For example, when dimensions are scaled by a
factor $k$, according to standard constant-field scaling laws, although the capacitances are lowered by a factor $k$, the contact resistance increases by the same factor (47).

Therefore, low resistance contacts are of paramount importance for efficient performance of the devices and circuits. A comprehensive review of contact technology in the first chapter suggests that a suitable metallization in conjunction with an optimized fabrication process are needed to realize low resistance contacts.

A high quality adhesion between thin films and substrates is essential for contact reliability. It depends on the nature and strength of the binding force at the interface. The parameters which influence adhesion are: crystal orientation, surface preparation, film deposition technique & vacuum conditions, thickness & composition of films, post evaporation treatments and thermal coefficients of expansions (5, 23, 48, 49). The surface preparation and evaporation conditions decide the contaminant atoms contents at the interface which weakens or strengthens the adhesion depending on whether the binding energy is decreased or increased. Sputtered films usually adhere better than evaporated ones since energetic sputtering atoms create defects & nucleation centers at the surface enhancing the binding energy.

The thermal mis-match between the materials of two adjoining layers result in development of undesirable blisters, cracks or holes and even peeling off of films occurs when the structure undergoes a thermal stress. A post metal deposition treatment like annealing or ion-beam mixing has been found to greatly improve the adhesion (5, 23, 49).

In order to maintain the stoichiometry of the semiconductor, composition and conducting properties of the metal film, the thermally induced interactions like elemental interdiffusion and chemical reactions
at the interface must be controlled or eliminated. The out-diffusion of semiconductor elements is attributed to grain boundaries and defects in the deposited film (23, 50, 51) and in-diffusion of metal atoms to vacancy and defect assisted mechanisms (5, 52, 53). The chemical reactions at the interface produce a variety of intermetallic compounds which alter the M-S barrier height and the electrical characteristics of the junction (5, 23, 31, 54).

Therefore, these physico-chemical effects at the interface should be controlled for the thermal stability of a contact and will be discussed in detail in the subsequent sections to design a stable metallization for ohmic contact to GaAs.

For reliability of high current carrying interconnect lines in a scaled down VLSIC, a high conductivity metal is preferred since line resistance increases by the scaling factor (5, 47).

When a metal film transports a current density is excess of \(10^5\) Amp. cm\(^2\), the electrons impart sufficient momentum to the metal atoms and goad them to move in the direction of current flow (55-57). Consequently, the metal accumulates at the electrical positive end of the conductor and depletes at the negative end. This leads to contact failure known as electromigration induced failure and is a well known phenomenon in silicon VLSICs (5, 28, 59, 60). The activation energy of this process is about 1 eV and is therefore easily accelerated by thermal means (5, 28).

The electromigration originated failure modes are characteristically cracks, voids, hillocks and breaks in the metal lines. The undercuts, sharp bends, constrictions, scratches and smears in the metallization lead to non-uniform distribution and points of excessive current density to evoke electromigration. A proper surface treatment and
dielectric passivation of metal lines have been reported to reduce electromigration (42, 44, 71).

In addition to above, the metal system chosen must be capable of deposition, patterning and replication of ultra-fine micro-structures at high yield. The dry etch compatibility and selective etchability are essential features of a VLSIC metallization. Further for wire bond capability it should be reasonably ductile and for long term reliability good resistance against oxidation and corrosion is desired.

In brief, it can be summarised that electromigration and interfacial interactions cause major concern to reliability of contacts operating at high current levels or at elevated temperatures. Electromigration is of more concern to planar contacts on integrated circuit or FET where a lateral flow of current is involved, while a great variety of device reliability problems is attributed to chemical reactions & material migration across a metal-semiconductor interface.

However, it is difficult to find a metallization that satisfies all the aforementioned criteria and this leads to the development of multi-layer metallization schemes which seek to obtain the optimum metal satisfying the above demands.

5.3 A STABLE METALLIZATION SCHEME

A general approach to design a reliable contact metallization is a three layer structure. The first layer is to produce the correct metal-semiconductor characteristics with good adherence to the semiconductor. A ductile top layer is required to meet the performance needs of the outer surface i.e good resistance against electromigration, corrosion and oxidation. To preclude atomic diffusion and chemical reactions at the interface, a barrier layer is required to be interposed between them. The final choice of a specific system as a whole is
determined on the basis of its compatibility with the device processing techniques.

Many metal and metallic alloys fulfill the requirements of primary contact and top surface layers (5, 23, 28, 45). Therefore, to design a reliable metallization, a proper selection of the intermediate barrier layer is of central importance. Implicit in the design of a thermally stable metallization is the need for creation of a barrier layer, through metal deposition, which will permit, each individual metal film to perform its intended function, while maintaining its integrity during subsequent device processing steps or its operation at high temperatures.

5.4 DESIGN CONSIDERATIONS OF A BARRIER LAYER

Thermodynamically, a multilayer thin film structure, made of different materials, is unstable because it is not in a state of minimum free energy (62). Consequently, atomic migration and chemical reactions take place to establish equilibrium by lowering the total free energy of the assembly (62, 64). The former originates from a concentration gradient and the latter is ascribed to a negative free energy of reaction in the system. Therefore, a barrier layer is designed to limit interdiffusion as well as chemical reactions at the interfaces in a multi-film structure.

5.4.1 BARRIER FOR INTER DIFFUSION

From a large number of experimental data, it has been established that diffusion at the free surface is the fastest, along grain boundaries and dislocations is the intermediate and in the bulk of crystals (lattice diffusion) is the slowest process (5, 23, 53). Each of these processes has different activation energy which results in a different temperature behaviour, predicted by the Arrhenius eqm. (2.1) discussed in the Chapter - II.
The design of diffusion barrier layer is based on the above concept (62-71). Obviously, a single crystal or epitaxial layer forms the first choice because the lattice diffusivity is the lowest. However, the fabrication of such a layer is generally incompatible to a device processing. In polycrystalline diffusion barrier film, although lattice diffusion predominates at high temperature, since the total cross-sectional area of the grain boundaries is small compared to that of the grains, the grain boundary diffusion process takes over at low temperatures (about one half or two third of melting point of the solid in °K, called Tammann temperature) (5,23,72). Hence, the polycrystalline barriers may not always be suitable.

Amorphous films possess no or negligible amount of grain boundaries. Therefore, atomic diffusivity in such films is intermediate between lattice and grain boundaries and thus provides an attractive and viable alternative to diffusion barriers (64-66, 73, 74).

It should be noted that diffusion barriers do not eliminate the driving force for diffusion, namely, the concentration gradient. They merely, reduce the rate of interdiffusion by presenting a region of reduced mobility for atomic migration. The role of a diffusion barrier, therefore, is to extend the life time of a contact to that of the projected use of the device or circuit.

5.4.2 BARRIER FOR CHEMICAL REACTION

The general concept of the 'Valency of chemical elements' is no more relevant when two metallic elements combine to form compounds (75). The heat of reaction i.e. the difference between the heats of formation of the reaction products and reactants determines whether the compounds will be formed or not (76). A thermodynamic criterion for chemical reaction to take place at a temperature (T), is negative Gibbs free energy change (ΔG) for the reaction, given by
\[ \Delta G = \Delta H - T \Delta S \quad (5.1) \]

where \( \Delta H \) is the change in enthalpy and \( \Delta S \) is the change in entropy. For the formation of alloys of two metals, \( \Delta G \sim \Delta H \), since contribution of entropy is very little. However, in case of oxides, \( \Delta S \) does play a part because entropy of oxygen in gas phase is significant (76, 77).

A chemical reaction between two dissimilar material in contact is favoured if the total energy of the system is lowered i.e. heat of reaction is negative. A positive heat of reaction deems the overall reaction thermodynamically unfavourable (76). The data of heat of reaction in combination with the relevant phase diagrams can predict the formation of intermetallic compounds and stable phases (76, 78) and have been reported to resolve many ambiguities involved in metal interaction with GaAs (79-81).

A multilayer thin film system is in stable chemical equilibrium as long as any change in temperature, concentration or pressure does not decrease the total free energy of the system. Since the mass transport across an interface brings the reacting species in contact, the rate of reaction is a matter of kinetics while for nucleation of a new phase the free energy of an atom in the new phase must be lower than that in the initial phase.

Therefore, chemical stability of a metal-semiconductor structure can be due to a kinetic limitation to the interfacial interactions or the absence of a thermodynamic driving force for the reaction i.e. \( \Delta G > 0 \).

Nicolet (67) has classified the barriers as passive, sacrificial and stuffed, according to the role they perform. A passive barrier, considered to be the ideal one, is chemically inert and non-reactive with the two materials which it separates. A sacrificial or reaction
barrier operates by the principle that it may react with the adjoining materials but at a predictable rate, which is sufficiently low, so that the barrier is not fully consumed before the performance life of the device. The stuffed barriers succeed because the fast diffusion paths i.e the grain boundaries are filled with some other material and are thus rendered passive or inert.

5.5 DESIGN OF THERMALLY STABLE METALLIZATION FOR OHMIC CONTACTS TO GaAs.

Gold alloys are extensively used for ohmic contacts to GaAs (5, 23, 29-33, 45) because gold satisfies most of the generic requirements of a metallization, discussed in the section 5.2. However, the deep penetration of gold into GaAs substrate (5,23, 32-34, 70, Fig. 2.5 in chapter II) and dissolution of gallium in the gold film preclude the use of gold based systems as a primary metallization for high temperature applications. The former degrades the contact properties (5, 35, 36, 64-66, 82) whereas the latter deteriorates the electromigration resistance of the gold film (83).

We therefore, developed a new structure as shown in Fig. 5.1, in which the top surface gold film is separated from the primary metal film of Ge by a barrier layer of tungsten silicide. The consideration of each of these layers is based on the criteria discussed in the following sub-sections. Some useful materials data used for the design are compiled in Table 5-1.

5.5.1 GERMANIUM PRIMARY CONTACT LAYER

Germanium is widely used as a dopant element in metal alloys for ohmic contacts to n-GaAs (5, 23, 29-34, 45). The important factors which make it suitable as a primary metallization layer on n-GaAs for high temperature contacts are:
FIG. 5.1. A THERMALLY STABLE METALLIZATION SCHEME FOR OHMIC CONTACT TO $n$-GaAs
### TABLE - 5-I

**Thermal Expansion Coefficient and Lattice Constant Data For GaAs Metallization Systems**

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Expansion Coefficient at 300°K x10⁻⁶°C</th>
<th>Lattice Constant ₀ A</th>
<th>REF.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>6.0</td>
<td>5.6531</td>
<td>(84)</td>
</tr>
<tr>
<td>Ge</td>
<td>5.5</td>
<td>5.6575</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>2.44</td>
<td>5.4307</td>
<td></td>
</tr>
<tr>
<td>VSi₂</td>
<td>11.2, 14.65</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>TaSi₂</td>
<td>8.8, 10.7</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MoSi₂</td>
<td>8.25</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>WSi₂</td>
<td>6.25, 7.90</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CoSi₂</td>
<td>10.14</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>NiSi₂</td>
<td>12.06</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Ta</td>
<td>6.5</td>
<td>-</td>
<td>(90)</td>
</tr>
<tr>
<td>Ti</td>
<td>8.5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Mo</td>
<td>5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Ni</td>
<td>13</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Pt</td>
<td>8</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>4.5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Sn</td>
<td>20</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Zn</td>
<td>35</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>14.2</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Ag</td>
<td>19.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Cu</td>
<td>16.6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Al</td>
<td>25.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Cr</td>
<td>6.0</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>
(i) On alloying, it provides the desired $n^+$-doping in the semiconductor surface, which is essential for an M-S interface to be ohmic.

(ii) The intrinsic barrier height of Ge-metal junction (0.5 eV) is lower than 0.8 eV of GaAs-metal interface (85).

(iii) Germanium has an excellent lattice matching with GaAs as depicted in Table 5-I.

(iv) The thermal coefficient of expansion of Ge matches reasonably well with that of GaAs (Table 5-I). The mismatch is of the order of $5 \times 10^{-7}$ per °C at 300 K.

The extremely low resistance contact on GaAs reported in the literature is attributed to the low barrier height associated with Ge-metal interface (85). The lattice mismatch of 0.08% between Ge and GaAs is lowest of all the heterojunction couples listed by Sharma and Purohit (84). This is primarily responsible for an easy deposition of germanium epitaxial film on GaAs, even by evaporation technique (86, 87). An excellent lattice and thermal match combination of Ge and GaAs, makes germanium an ideal primary contact layer material on n-GaAs, for high temperature stability.

5.5.2 GOLD AS SURFACE LAYER

The widespread use of gold in semiconductor technologies is attributed to its noble character, ease of deposition and patterning, high ductility and conductivity (5, 23, 45). Additionally its stability against exposure to environment (as gold does not form oxides) and excellent electromigration properties (88, 89) strengthens the choice of gold as covering metal layer on a contacting metallization.

5.5.3 TUNGSTEN SILICIDE BARRIER LAYER

Our results in the chapter II, conclude that Ga & As from GaAs, diffuse through the contacting germanium layer, when the system undergoes a heating cycle. Therefore, it is necessary to consider
interactions between Ga, As and WSL in the present structure. The main role of the thin germanium layer in this metallization scheme is to provide Ge atoms to diffuse into the n-GaAs substrate to generate donors.

We considered the appropriateness of tungsten silicide as a barrier for the following reasons.

(i) Phase diagrams in Fig. 5.2 illustrate the stability of $W_5Si_3$ and WSi$_2$ phases with GaAs (78).

(ii) The chemical stability of a few silicides (listed in Table 5-1) has recently been predicted by Lau et al. (92), using thermodynamic data of Miedema (76). Their stability criterion is positive heat of reaction i.e ($\Delta H_{298} > +5$ kcal), and for reactions between the stable phases of tungsten silicides and GaAs are calculated as

\[
W_5Si_3 + 5GaAs \rightarrow 5Ga + 5WAs + 3Si
\]

\[8(-5\text{kcal/g.atom}) \quad 10(-9.8\text{kcal/g.atom}) \quad 5(0) \quad 10(-9.0\text{kcal/g.atom}) \quad 3(0)
\]

\[\Delta H_{298} = +48 \text{kcal}\]

and

\[
WSi_2 + GaAs \rightarrow Ga + WAs + 2Si
\]

\[3(-5\text{kcal/g.atom}) \quad 2(-9.8\text{kcal/g.atom}) \quad 1(0) \quad 2(-9.0\text{kcal/g.atom}) \quad 2(0)
\]

\[\Delta H_{298} = +16.6\text{kcal}\]
FIG. 5.2 (a) PSEUDOTERNARY AND 
(b) QUATERNARY REPRESENTATIONS OF SILICIDE 
EQUILIBRIA WITH GaAs IN W-Si-Ga-As SYSTEM 
(Ref. 78)
In these reactions formation of WGa is not considered since it has positive heat of reaction whereas it is negative for formation of WAs (92, 93). The positive heat of reactions in eqns. (5.2) and (5.3) implies that both the phases of tungsten silicide are in thermodynamical equilibrium on GaAs and hence the resultant contact would be resistant to a high temperature cycles.

(iii) As illustrated in Table 5-1, the thermal matching of WSi₂ with both Ge and GaAs is best among all the silicides

(iv) Tungsten silicide is generally deposited by sputtering technique which often produces an amorphous film. Thus in addition to good adherence, it acts as an amorphous barrier.

(v) The device processing compatibility of silicides is well established as these are extensively being used in the modern silicon VLSICs fabrication (28, 90):

On the basis of these criteria we have chosen WSi₂ to perform role of a barrier layer in the metallization scheme shown in Fig. 5.1. Chemical interaction of Ge with WSi₂ is not discussed, since heat of reaction data for this is not available in Miedema's paper. However, ESCA characterisation, to be described in the next section, clearly establishes that WSi₂ acts as an effective diffusion barrier and does not allow Ge to diffuse into it even at a high temperature anneal.

5.6 CHARACTERISATION OF GaAs-Ge-WSi₂-Au SYSTEM

The experimental details concerning sample preparation and ESCA analysis are same as described in the section 2.2 of chapter II. However, the sandwich layer of tungsten silicide in the present structure as shown in Fig. 5.1, is deposited in a Belzar sputtering system, evacuated to obtain a background pressure of 5x10⁻⁷ Torr. The sputtering is carried out in argon at 3x10⁻⁶ Torr, prior to gold
deposition. Samples are annealed to 460°C, 510°C and 610°C for 60 minutes in nitrogen atmosphere. In order to avoid variations between different wafers and different depositions, samples are derived from the same wafer for direct comparisons between as-deposited and annealed cases.

5.6.1 ESCA ANALYSIS RESULTS

Figs. 5.3 to 5.6 represent ESCA sputter profiles of the as-deposited and annealed specimen as indicated there. The as-deposited sample is not subjected to any intentional heat treatment. Nevertheless, during sputter deposition of WSi₂, the wafer gets heated up approximately upto 250°C owing to ion-bombardment. Therefore, the depth distribution profiles of Ga, As, Ge, W, Si & O for the reference as well as the annealed specimen are likely to be influenced by this heating. Following important results can easily be extracted from these profiles:

(i) The contacting system remains stable upto 460°C anneal since a comparison between profiles of the reference and annealed specimen hardly shows any variation. Thus no measurable interdiffusion of elements is detected for alloying upto 460°C.

(ii) The presence of oxygen is recorded starting from the gold surface to the interface even in the un-annealed case. It is interesting to note that the oxygen peak in the WSi₂ layer of the reference sample (Fig. 5.3) disappears on annealing (Fig. 5.4) and oxygen content builds up on the surface and at the interface on subsequent annealing (Figs. 5.5-5.6) at elevated temperatures.

(iii) Results of 460°C anneal in Fig. 5.4 suggest initiation of silicon diffusion in the overlying gold film. It tends to accumulate on the surface for higher temperature anneals. However, till 510°C no appreciable penetration of silicon into germanium layer is observed.
(iv) A very small amount of tungsten is recorded even at the gold surface and is found to enhance slightly with alloying temperature. Its stability with respect to WSi$_2$-Ge interface is remarkable until the annealing temperature exceeds 510°C.

(v) Germanium penetration into GaAs and to a small extent into WSi$_2$ is detected on annealing. Its indiffusion into semiconductor particularly gets enhanced on alloying at high temperatures (Fig. 5.5 & 5.6).

(vi) A small and constant amount of gallium (about 2-3 %) appears to exist throughout the metal film even in the reference sample. At high temperature anneals, although gallium concentration does not rise much in the alloyed region but its tendency to accumulate on the surface is seen (Fig. 5.5 & 5.6).

(vii) No arsenic signal is detected upto 510°C alloying. Only at 610°C anneal a slight amount of arsenic in the WSi$_2$ layer is measured.

(viii) Gold penetration into WSi$_2$ layer becomes appreciable only at 610°C. But it could hardly reach at the GaAs-Ge interface even at such a high alloying temperature.

It is evident from the above results that the substantial interdiffusion occurs only at 610°C anneal, which appears to get initiated at 510°C only for a few elements of the system. Therefore, the contact system proves to be safely stable upto 460°C for device application. To reaffirm the long term thermal stability of the metallization, a sample is subjected to thermal stress at 350°C for 200 hours in nitrogen ambient. The subsequent ESCA investigation of the sample did not show any interdiffusion or degradation of the contact properties.

In an attempt to reduce the barrier layer thickness, a 500 Å thick WSi$_2$ is used in the above metallization scheme. ESCA analysis
FIG. 5.3 ESCA SPATTER PROFILE OF A SAMPLE AS - DEPOSITED
FIG. 5.4 ESCA SPUTTER PROFILE OF A SAMPLE ANNEALED AT 460°C (1 Hour)
FIG. 5.5 ESCA SPUTTER PROFILE OF A SAMPLE ANNEALED AT 510°C (1 Hour)
FIG. 5.6  ESCA SPATTER PROFILE OF A SAMPLE ANNEALED AT 610°C
(1 Hour)
of the annealed samples showed strong interdiffusion even at a low temperature alloying and intermixing of elements at 610°C.

5.6.2 SEM EXAMINATION

Figs. 5.7(a) to 5.10(a) are SEM pictures showing surface topography of the reference and annealed specimen. It is evident from the figures that voids and cracks exist in the gold film even in case of the reference sample, the density of which progressively increases with alloying temperatures (Figs. 5.8(a) - 5.10(a)). At 610°C anneal the gold film breaks & becomes discontinuous forming globules or balls on the surface (Fig. 10(a)).

Electron micrographs in Figs. 5.7(b) to 5.10(b) are obtained after removing the gold film by chemical etching. It is seen that the underlying WSi₂ surface is almost featureless upto 510°C anneal. However, the leftover gold particles (perhaps due to incomplete etching) or dust particles are visible on the surface images.

5.6.3 ELECTRICAL EVALUATION

For electrical characterization, contact resistance measurements are carried-out using transmission line method. The measured value of contact resistivity is of the order of 10⁻⁵ ohm-cm² (94). The metallization is incorporated as ohmic contacts in the fabrication of power MESFETs. The devices are found to work satisfactorily at the designed power level (95). These results evince that Ge-WSi₂-Au constitutes a thermally stable metallization for ohmic contact to n-GaAs and therefore can be applied for high temperature applications.

5.7 DISCUSSIONS

With the aid of available tables of standard ESCA spectra of the elements and line energy information (96) it can easily be predicted, on the basis of measured energy positions and binding energy shifts of Ga,Ge,Si and O peaks, that the metallic oxides are present on the
FIG. 5.7 SEM MICROGRAPHS OF GaAs-Ge-WSi$_2$-Au SAMPLE SURFACE. THE BARS REPRESENT 1um.
(a) ANNEALED SURFACE. THE BAR REPRESENTS 1 μm

(b) AFTER ETCHING Au-LAYER OF THE ANNEALED SAMPLE. THE BAR REPRESENTS 10 μm.

FIG. 5.8 SEM MICROGRAPHS OF GaAs-Ge-WSi₂-Au SAMPLE ANNEALED AT 460°C FOR 1 HOUR.
FIG. 5.9 SEM MICROGRAPHS OF A GaAs-Ge-WSi₂-Au SAMPLE ANNEALED AT 510°C FOR 1 HOUR.
(a) ANNEALED SURFACE. THE BAR REPRESENTS 1μm

(b) AFTER ETCHING Au-LAYER OF THE ANNEALED SAMPLE. THE BAR REPRESENTS 10 μm.

FIG. 5.10 SEM MICROGRAPHS OF A GaAs-Ge-WSi$_2$-Au SAMPLE ANNEALED AT 610°C. FOR 1 HOUR.
surface. Thus, in general, this explains the accumulation of these elements on the surface when the samples are alloyed, and it is akin to the results described in the chapter II.

Oxygen inclusion in the reference metallization could be from adsorbed oxygen on GaAs substrate and its incorporation during sputtering. A peak in oxygen concentration in WSi₂ layer in the reference sample (Fig. 5.3) strongly favours oxygen inclusion during sputter deposition of WSi₂. The increase in its concentration on the surface and at the interface on annealing (Figs. 5.4-5.6) concurs with the experimental observations of Ohfuji et.al (93), who attributed it to increase in grain size, fast diffusivity of oxygen into GaAs and formation of stable gallium oxide (Ga₂O₃) on the surface. The surface accumulation of silicon (Fig. 5.5 & 5.6) is also ascribed to presence in its oxide form.

The appearance of tungsten signal on the gold surface may be due to thermal mismatch between gold and WSi₂ (Table 5-1). This generates holes & cracks in the gold film when the structure is heat treated (Figs. 5.7(a)-5.10(a)). Therefore, tungsten signal corresponds to contribution from these openings, the area of which increases with alloying temperature to add to the tungsten concentration in the distribution profile.

The presence of gallium all through the metallization could be attributed to gallium out diffusion through grain boundaries of germanium and subsequent incorporation in WSi₂ film during sputter deposition. On annealing, this distributed gallium diffuses out to form metallic phases with gold and accumulates on the surface in the form of its oxides, as it has a great affinity for oxygen (23). As observed in the case of tungsten, discussed in the previous paragraph, the contribution to gallium signal from the voids in the gold film is also quite probable.
The above discussion does not consider the formation of oxides and nitrides of tungsten (as annealing ambient is nitrogen). Although WO$_3$ is volatile above $530^\circ$C thermodynamically it is a stable compound ($\Delta H_{298} = -201$ kcal/mol) (93). It is very likely that the effectiveness of WSi$_2$ as a barrier layer (for gold indiffusion and out migration of Ga & As) is due to formation of tungsten oxide or nitride. Oxygen or nitrogen plugs the grain boundaries of tungsten grains which then acts as a stuffed barrier. Nonetheless, the present investigation establishes WSi$_2$ (1000 Å) as an effective barrier to constitute Ge-WSi$_2$-Au as a thermally stable metallization for ohmic contacts to n-GaAs.

5.8 CONCLUSIONS

The investigation reports that WSi$_2$ represents a stable diffusion barrier in a GaAs-Ge-WSi$_2$-Au system. It completely precludes the penetration of gold into GaAs which is considered to be the main culprit (82) in a metallization from reliability point of view. It is therefore possible to produce thermally stable ohmic contacts for GaAs devices operating at elevated temperatures. The observed indiffusion of Ge into GaAs shows a favourable situation for ohmicity of the junction, since Ge acts a donor in GaAs alloyed system and thus forms the desired degenerate layer at the interface.

The presence of a small and constant quantity of Ga in the metal layer may be accredited to out diffusion of Ga in WSi$_2$ film during its sputter deposition. Since gallium amount does not significantly increase with alloying temperature, it can be presumed that once WSi$_2$ is formed, it does not allow further migration of Ga from GaAs. During sputter deposition the temperature of the wafer rises to about $250^\circ$C, so the possibility of gallium outdiffusion seems to be convincing during deposition.
On the basis of our gallium vacancy diffusion model, described in the chapter III, the limited gallium out diffusion provides required gallium vacancies for substitution by indiffusing germanium to form donors. However, one can still optimize the thickness of germanium layer in the present structure to manoeuvre the gallium out diffusion & germanium indiffusion into GaAs to obtain low resistance contacts.
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