ABSTRACT

The fast developments in the field of wireless communication require more flexible and cost effective radio architecture. This architecture should have the capability to dynamically alter the functional blocks of physical layer to support different wireless communication technology standards. Therefore, there is a demand for the use of a basic architecture that can be reconfigured to support both existing and future wireless communication technology standards. Field Programmable Gate Array architectures (FPGAs) provide a suitable platform to achieve such dynamic reconfigurations. This thesis explores the use of FPGAs in the design of reconfigurable architecture. Using a case study, it is demonstrated that this architecture efficiently configures to support different modulation schemes for Wide-band Code Division Multiple Access (WCDMA) standard and Orthogonal Frequency Division Multiplexing (OFDM) based Wireless Local Area Network (WLAN), a.k.a Wireless Fidelity (WiFi).

The most innovative part of this architecture is that it exploits multiplier-less algorithm and algorithmic strength reduction transformation technique to reduce large number of multipliers to achieve area efficiency. The thesis also proposes a method for mapping applications onto the reconfigurable resource sharing architecture. The similarities in computational processing elements of Fast Fourier Transform (FFT) in OFDM and RAKE

receiver in WCDMA are identified and these elements are effectively reused in the hardware while reconfiguring to different standards.

The area utilized by the proposed reconfigurable resource sharing architecture is compared with the conventional architecture that does not share resources. The comparison results show an area reduction of about 56 to 57 percent in the proposed design compared to the conventional architecture considered in this thesis. It is also proved that the proposed architecture saves about 54% of power by resource sharing method compared with the conventional architecture. The proposed FFT and RAKE receiver implementations are also compared with conventional receiver implementations. An area reduction of about 15-20 percent in the proposed FFT implementation and 90-91 percent in the proposed RAKE receiver is achieved compared to conventional architecture. This thesis demonstrates that the proposed architecture is used to provide flexibility, performance, efficiency and better resource utilization even while meeting the area and power constraints set by a particular design.