

REFERENCES

1. Ada, S. Y. P. "An Energy-Efficient Reconfigurable Baseband Processor for Wireless Communications", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 15, No. 3, pp. 319-327, 2007.
2. Ahmad, M. A. "Dynamically reconfigurable architecture for third generation mobile systems", Ph.D. dissertation Ohio University, 2002.
3. Ahmad Sghaier, Shawki Areibi and Bob Dony, "A Pipelined Implementation of OFDM transmission on Reconfigurable Platforms", *Proceedings of the IEEE Conference on Communication Systems*, 2008.
4. Alsolaim, A., Becker, J., Glesner, M. and Starzyk, J. "Architecture and Application of a dynamically reconfigurable hardware array for future mobile communication systems", in *Proc. of IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 205-214, 2002.
5. Baumgarten, V., May, F., Nuckel, A., Vorbach, M. and Weinhardt, M. "PACT XPP-A selfreconfigurable data processing architecture", in *Proceedings First International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, LasVegas, 2001.
6. Boris, D. A., Edward, L., Titlebaum and Eby G. Friedman, "Low Power Flexible RAKE Receivers For WCDMA", *Proc. International Symposium on Circuits and Systems ISCAS '04*, Vol. 4 pp. 97-100, 2004.
7. Chandrakasan, A., Potkonjak, M., Rabaey, J. and Brodersen, R., "Optimizing Power using Transformations", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.14, No. 1, pp. 12-31, 1995.
8. Chen, D. C. and Rabaey, J. M. "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths", *IEEE J. Solid-State Circuits*, Vol. 27, No. 12, pp. 1895-1904, Dec. 1992.
9. Chin-Teng Lin, Yuan-Chu Yu and Lan-Da Van, "A low power 64-point FFT/IFFT design for IEEE 802.11a WLAN application",

Proceedings of IEEE International symposium on Circuits and Systems, pp.45264529, 2006

10. Christophe Bobda, "Introduction to Reconfigurable Computing Architectures, Algorithms, and Applications", Springer, Netherlands, 2007.
11. Claudio Brunelli, Fabio Garzia, Davide Rossi and Jari Nurmi, "A coarse-grain reconfigurable architecture for multimedia applications supporting subword and floating-point calculations", Journal of Systems Architecture, Elsevier, Vol. 56, pp. 38-47, 2010.
12. Ebeling, C., Fisher, C., Xing, G., Shen, M. and Liu, H. "Implementing an OFDM receiver on the RaPiD reconfigurable architecture", IEEE Trans. Comput., Vol. 53, No. 11, pp. 1436-1448, 2004.
13. Erik Dahlman, Stefan Parkvall, Johan Skold and Per Beming, "3G Evolution HSPA and LTE for Mobile Broadband", Elsevier, London, 2007.
14. Gerard, K. R., Paul M. Heysters and Gerard J. M. Smit, "Towards Software Defined Radios Using Coarse-Grained Reconfigurable Hardware", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 1, pp. 3-13, 2008.
15. Goldstein, S. C., Schmit, H., Budiu, M., Cadambi, S., Moe, M. and Taylor, R. R. "PipeRench: a reconfigurable architecture and compiler", IEEE Computer, Vol. 33(4), pp. 70-77, 2000.
16. Gour Karmakar and Laurence S. Dooley, "Mobile Multimedia Communications: Concepts, Applications, and Challenges", Information Science Reference, Poland, 2008.
17. Hang Liu and Hanho Lee, "High-Speed Four-Parallel 64-Point Radix-2⁴ MDF FFT/IFFT Processor for MIMI-OFDM Systems", Proceedings of the 23rd International Technical Conference on Circuits/Systems, Computers and Communications, pp. 834-837, 2008
18. Hauck, S., Fry, T. W., Hosler, M. M. and Kao, J. P. "The Chimaera Reconfigurable Functional Unit", IEEE Transactions on Very Large Scale Integration (VLSI) systems, Vol. 12, No. 2, pp. 206-217, 2004.
19. Havinga, P. J. M., Smit, L. T., Smit, G. J. M., Bos, M. and Heysters, P. M. "Energy management for dynamically reconfigurable

- heterogeneous mobile systems”, 10th Heterogeneous Computing Workshop, San Francisco, 2001.
20. Heiko Hinkelmann, Peter Zipf, Jia Li, Guifang Liu and Manfred Glesner, “On the design of reconfigurable multipliers for integer and Galois field multiplication”, *Microprocessors and Microsystems*, Elsevier, Vol. 33(1), pp. 2-12, 2009.
 21. Heng, T. and Ronald, F. D. “A Multilayer Framework Supporting Autonomous Run-Time Partial Reconfiguration”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, No. 5, pp. 504-515, 2008.
 22. Hyung-Jin Lee and Dong Sam Ha, “A New Low-Power And Area Efficient Rake Receiver Design Without Incurring Performance Degradation”, in *Proceedings International ASIC/SOC Conference*, pp. 251-255, 2002.
 23. Jina, K. and Dong, S. H. “A New Reconfigurable Modem Architecture for 3G Multi-Standard Wireless Communication Systems”, in *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 1051-1054, 2005.
 24. Jong-Suk Lee and Dong Sam Ha, “FleXilicon Architecture and Its VLSI Implementation”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 8, pp. 1021-1033, 2009.
 25. Joseph Boccuzzi, “Signal Processing for Wireless Communications”, McGraw Hill, New York, 2008.
 26. Jurgen Becker and Manfred Glesner, “A Parallel Dynamically Reconfigurable Architecture Designed for Flexible Application-Tailored Hardware/Software Systems in Future Mobile Communication”, *The Journal of Supercomputing*, Vol. 19(1), pp. 105-127, 2001.
 27. Jurgen Helmschmidt, Eberhard Schuler, Prashant Rao, Sergio Rossi, Serge di Matteo and Rainer Bonitz, “Reconfigurable Signal Processing in Wireless Terminals”, *Proc. of the conference on Design, Automation and Test in Europe: Designers' Forum*, 2, 20244 , 2003.
 28. Keshab K. P. “VLSI Digital Signal Processing Systems : Design and Implementation”, Wiley Interscience Publication, New York, 2003.
 29. Kiat-Seng Yeo and Kaushik Roy, “Low-voltage, Low power VLSI subsystems”, McGraw-Hill, New York, 2005.

30. Lam, S. K. and Srikanthan, T. "Rapid design of area-efficient custom instructions for reconfigurable embedded processing", *Journal of Systems Architecture*, Elsevier, Vol. 55, pp. 1-14, 2009.
31. Lasse Harju and Jari Nurmi, "A Programmable Baseband Receiver Platform for WCDMA/OFDM Mobile Terminals", in *Proceedings IEEE Conference on Wireless Communications and Networking*, pp. 33-38, Vol. 1, 2005.
32. Lu, W., Zhao, S., Lu, C., Zhou, X. and Sobelman, G. E. "A heterogeneous reconfigurable baseband architecture for wireless LAN transceivers", in *Proc. EIT*, pp. 284-288, 2008.
33. Mahesh, R. and Vinod, A. P. "New Reconfigurable Architectures for Implementing FIR Filters with Low Complexity", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 2, pp. 275-288, 2010.
34. Marlene Wan, Hui Zhang, Varghese George, Martin Benes, Arthur Abnous, Vandana Prabhu and Jan Rabaey, "Design Methodology of a Low-Energy Reconfigurable Single-Chip DSP System", *Journal of VLSI Signal Processing*, Vol. 28, pp. 47-61, 2001.
35. Maya Gokhale and Paul, S. G., "Reconfigurable Computing Accelerating Computation with Field-Programmable Gate Arrays", Springer, Netherlands, 2005.
36. Mei, B., Vernalde, S., Verkest, D., De Man, H. and Lauwereins, R. "ADRES: An architecture with tightly coupled VLIW processor and coarse-grained reconfigurable matrix", *Lect. Notes in Comput. Sci.*, pp. 2778, 2010.
37. Michalis, D. G., Gregory Dimitroulakos and Costas E. Goutis, "Partitioning Methodology for Heterogeneous Reconfigurable Functional Units", *The Journal of Supercomputing*, Vol. 38, pp. 17-34, 2006.
38. Michalis D. G., Gregory Dimitroulakos and Costas E. Goutis, "Speedups and Energy Reductions From Mapping DSP Applications on an Embedded Reconfigurable System", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 15, No. 12, pp. 1362-1366, 2007.

39. Mirsky, E. and DeHon, A. "MATRIX: A reconfigurable computing architecture with configurable instruction distribution and deployable resources", in Proc. IEEE Symp. FPGAs Custom Comput. Mach., pp. 157-166, 1996.
40. Morris, G. R. and Prasanna, V. K. "A pipelined-loop-compatible architecture and algorithm to reduce variable-length sets of floating-point data on a reconfigurable computer", J. Parallel Distrib. Comput., Vol. 68, Elsevier, pp. 913-921, 2008.
41. Mustafa Ergen, "Mobile Broadband Including WiMAX and LTE", Springer, New York, 2009.
42. Najam-ul-Islam Muhammad, Karim Khalfallah, Raymond Knopp and Renaud Pacalet, "Reconfigurable DSP Architectures for SDR Applications", in Proceedings, 14th IEEE International Conference on Electronics, Circuits and Systems, pp. 971-974, 2007.
43. Nazish Aslam, Mark John Milward, Ahmet Teyfik Erdogan and Tughrul Arslan, "Code Compression and Decompression for Coarse-Grain Reconfigurable Architectures", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 12, pp. 1596-1608, 2008.
44. Park, J., Jung, H. and Prasanna, V., "Efficient FPGA-based Implementations of the MIMO-OFDM Physical Layer", in Proc. ERSA, 2006.
45. Paul Heysters, Gerard Smit and Egbert Molenkamp, "A Flexible and Energy-Efficient Coarse-Grained Reconfigurable Architecture for Mobile Systems", The Journal of Supercomputing, Kluwer Academic Publishers, Vol. 26, pp. 283-308, 2003.
46. Rajaram Sivasubramanian and Abhaikumar Varadhan, "An Efficient Implementation of IS-95A CDMA Transceivers through FPGA", DSP Journal, ICGST, Vol. 6(1), pp. 23-30, 2006.
47. Ramjee Prasad and Luis Munoz, "WLANs and WPANs towards 4G Wireless", Artech House universal personal communications library, Boston, 2003.
48. Rauwerda, G. K., Smit, G. J. M., Van Hoesel, L. F. W. and Heysters, P. M. "Mapping Wireless Communication Algorithms to a Reconfigurable Architecture", in Proceedings, International

- Conference on Engineering of Reconfigurable Systems and Algorithms, pp. 242-251, 2010.
49. Reiner Hartenstein, "Coarse Grain Reconfigurable Architectures", in Proceedings, Conference on Asia South Pacific Design Automation, pp. 564-570, 2001.
 50. Rudolf Tanner and Jason Woodard, "WCDMA – Requirements and Practical Design", John Wiley & Sons Ltd., England, 2004.
 51. Sebastien Pillement, Olivier Sentieys and Raphael David, "DART: A Functional Level Reconfigurable Architecture for High Energy Efficiency", EURASIP Journal on Embedded Systems, Article ID 562326, Hindawi Publishing Corporation, doi:10.1155/2008/562326, Vol. 2008, 13 pages, 2008.
 52. Sedcole, P., Blodget, B., Becker, T., Anderson, J. and Lysaght, P. "Field Programmable Logic and Applications Modular dynamic reconfiguration in Virtex FPGAs", IEE Proc.Comput. Digit. Tech., Vol. 153, No. 3, 2006.
 53. Shen-Chuan Tai, Chuen-Ching Wang and Chih-Ying Lin, "FFT and IMDCT Circuit Sharing in DAB Receiver", IEEE Transactions on Broadcasting, Vol. 49, No. 2, pp. 124-130, 2003.
 54. Singh, H., Lee, M.H., Lu, G., Kurdahi, F. J., Bagherzadeh, N. and Filho, E. M. C. "Morphosys: An integrated reconfigurable system for data-parallel and computation intensive applications", IEEE Transactions on Computers, Vol. 49, No. 5, pp. 465-481, 2000.
 55. SotirisXydis, George Economakos and Kiamal Pekmestzi, "Designing coarse-grain reconfigurable architectures by inlining flexibility into custom arithmetic data-paths", Integration, the VLSI Journal, Vol. 42, pp. 486-503, 2009.
 56. Speth, M., Fechtel, S., Fock, G. and Meyr, H. "Optimum Receiver Design for OFDM-Based Broadband Transmission-Part II: A Case Study", IEEE Transactions. on Communications, Vol. 49, No. 4, pp. 571-578, 2001.
 57. Spyridon, B., Konstantinos, M., Chrissavgi, D., Christos, D., Fragkiskos, I., Dimitris, M., Thanasis, P., Aristodemos, P., Anna, T., Theodor, T. and Adamandios, V. "Prototyping of a 5 GHz WLAN

- Reconfigurable System-on-Chip”, *IEICE Trans. INF. and SYST.*, Vol. E86-D, No. 5, 2003.
58. Srinivasa Chaitanya, K., Muralidhar, P. and Rama Rao, C. B. “Implementation of CORDIC Based Architecture for WCDMA/OFDM Receiver”, *European Journal of Scientific Research*, Vol. 36, No. 1, pp. 65-78, 2009.
 59. Stamatis Vassiliadis and Dimitrios Soudris, “Fine and Coarse-Grain Reconfigurable Computing”, Springer-Verlag, New York, 2007.
 60. Stephen Craven and Peter Athanas, “Dynamic Hardware Development”, *International Journal of Reconfigurable Computing*, Article ID 901328, doi:10.1155/2008/901328, 10 pages, 2008.
 61. Sudarshan Banerjee, Elaheh Bozorgzadeh and Nikil, D. D. “Integrating Physical Constraints in HW-SW partitioning for Architectures with Partial Dynamic Reconfiguration”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 14, No. 11, pp. 1189-1202, 2006.
 62. Sukhsawas, S., Benkrid, K., “A high-level implementation of a high performance pipeline FFT on Virtex-E FPGAs”, *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI System Design*, Vol. 2, No. 4, pp. 229-232, 2004.
 63. Taylor, M.B., Lee, W., Miller, J., Wentzlaff, D., Bratt, I., Greenwald, B., Hoffman, H., Johnson, P., Kim, J., Psota, J., Saraf, A., Shindman, N., Strumpfen, V., Frank, M., Amarasinghe, S. and Agarwal, A. “Evaluation of the RAW microprocessor: An exposed wire-delay architecture for ILP and streams”, in *Proceedings of 31st International Symposium on Computer Architecture (ISCA)*, 2004.
 64. Thilo Pionteck, Carsten Albrecht, Roman Koch and Erik Maehle, “Adaptive Communication Architectures For Runtime Reconfigurable System-On-Chips”, *Parallel Processing Letters*, World Scientific Publishing Company, Vol. 18, No. 2, pp. 275-289, 2008.
 65. Timo Halonen, Javier Romero and Juan Melero, “GSM, GPRS Performance AND EDGE Evolution Towards 3G/UMTS”, Second Edition, John Wiley & Sons Ltd, England, 2003.
 66. Timo Vogt and Norbert When, “A Reconfigurable ASIP for Convolutional and Turbo Decoding in an SDR Environment”, *IEEE*

- Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 10, pp. 1309-1320, 2008.
67. Todman, T. J., Constantinides, G. A., Wilton, S.J.E., Mencer, O., Luk, W. and Cheung, P. Y. K. "Reconfigurable computing: architectures and design Methods", IEE Proc. Comput. Digit. Tech., Vol. 152, No. 2, 2005.
 68. Tony Wakefield, Dave McNally, David Bowler, Alan Mayne, "Introduction to Mobile Communications Technology, Services, Markets", Auerbach, New York, 2007.
 69. Tze-Yun Sung, Hsi-Chin Hsin and Yi-Peng Cheng, "Low-power and high-speed CORDIC-based split-radix FFT processor for OFDM systems", Digital Signal Processing, Elsevier Vol. 20, No. 2, pp. 511-527, 2010.
 70. Waingold, E., Taylor, M. and Srikrishna, D. "Baring it all to Software: Raw Machines", IEEE Trans. on. Computers, Vol. 53, No. 11, pp. 1436-1448, 2004.
 71. Xilinx Inc. "ISE Design Suite 12: Installation, Licensing and Release Notes", UG 631,V12.2, 2010.
 72. Xilinx Inc. "Virtex-6 FPGA Configuration User Guide", UG 360, V3.2, 2010.
 73. Xilinx Inc. "Virtex-6 FPGA DSP48E1 slice User Guide", UG 369,V1.3, 2011.
 74. Ying-Chang Liang, Sayed Naveen, Santosh K.Pilakkat and Ashok K. Marath, "Reconfigurable Signal Processing and Hardware Architecture for Broadband Wireless Communications", EURASIP Journal on Wireless Communications and Networking, Vol. 3, pp. 323-332, 2005.
 75. Yoonjin Kim, Mary Kiemb, Chulsoo Park, Jinyong Jung and Kiyoun Choi, "Resource Sharing and Pipelining in Coarse-Grained Reconfigurable Architecture for Domain-Specific Optimization", Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE'05), 2005.
 76. Yoonjin Kim, Rabi N. Mahapatra, Ilhyun Park and Kiyoun Choi, "Low Power Reconfiguration Technique for Coarse-Grained

- Reconfigurable Architecture”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 17, No. 5, pp. 593-603, 2009.
77. Zain-ul-Abdin and Bertil Svensson, “Evolution in architectures and programming methodologies of coarse-grained reconfigurable computing”, Microprocessors and Microsystems, Vol. 33, pp. 161-178, 2009.
 78. Zexin Pan and Earl Wells, B. “Hardware Supported Task Scheduling on Dynamically Reconfigurable SoC Architectures”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 11, pp. 1465-1474, 2008.
 79. Zhi Alex Ye, Andreas Moshovos, Scott Hauck and Prithviraj Banerjee, “CHIMAERA: A High-Performance Architecture with a Tightly-Coupled Reconfigurable Functional Unit”, in Proceedings of the 27th Annual International Symposium On Computer Architecture, pp. 225-235, 2000.
 80. Zhuan Ye, Yun Kim and Anthony Schooler, “A Flexible Chip Rate Processor For CDMA RAKE Receiver”, Proceeding of the SDR 03 Technical Conference and Product Exposition, 2003.